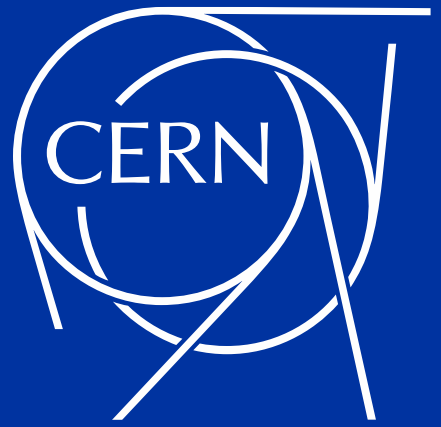


UQDS – a versatile quench detection and measurement system for the HiLumi era

Jens Steckert, Reiner Denz, Tomasz Podzorny, Jelena Spasic
David Bailey, Daniel Blasco Serrano, Magnus Christensen, Adam Hollos, Josef Kopal, Surbhi Mundra, Guzman Martin, Andrzej Skoczen, Dragos Gabriel Vancea & MPE-EP Colleagues

Thanks to SM18 & Test bench crews for their support !

Introduction

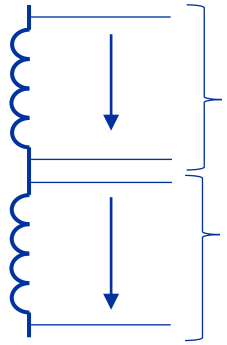
Motivation

- HiLumi comprises of many different new and complex magnets:
  ➔ Big variety but small numbers per item (compared to LHC)
- Design one generic system with enough resources to perform quench detection and monitoring of all HiLumi circuit elements

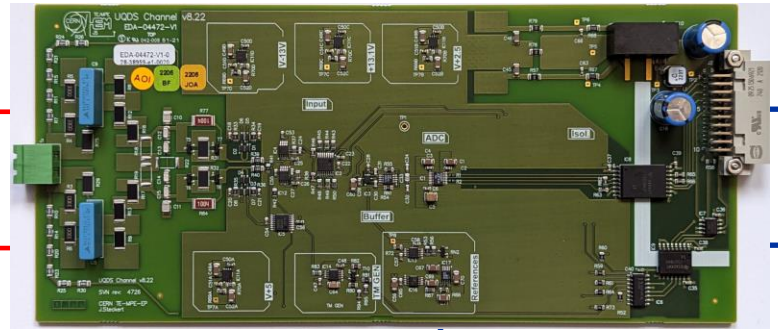
Implementation

- Base new design on programmable Logic (FPGA) in combination with a number of galvanically isolated front-end channels
- Quench detection algorithm defined in Gateware of FPGA
- Design is a quench detection AND measurement system

System overview (UQDSv2)



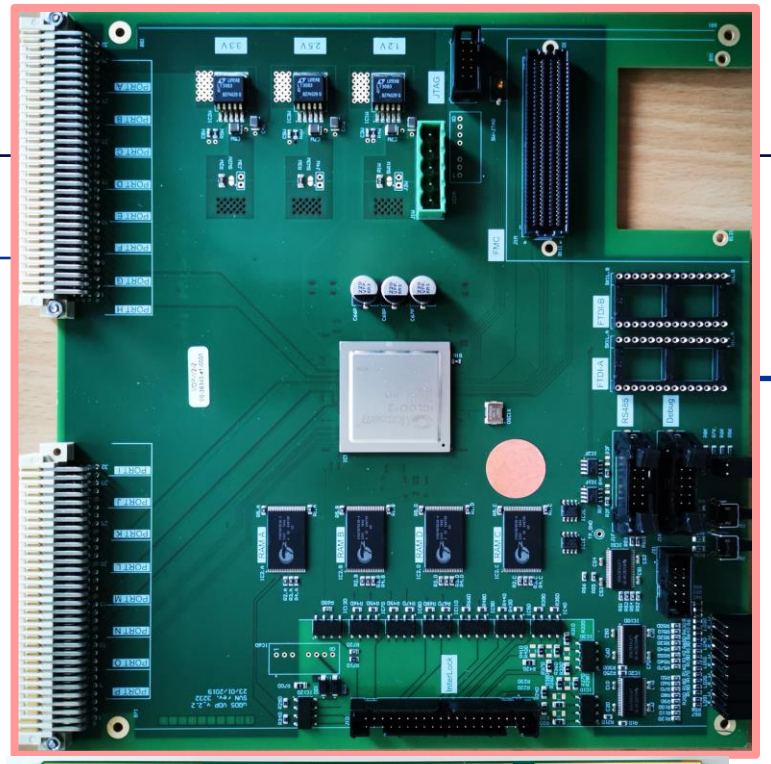
Voltage taps

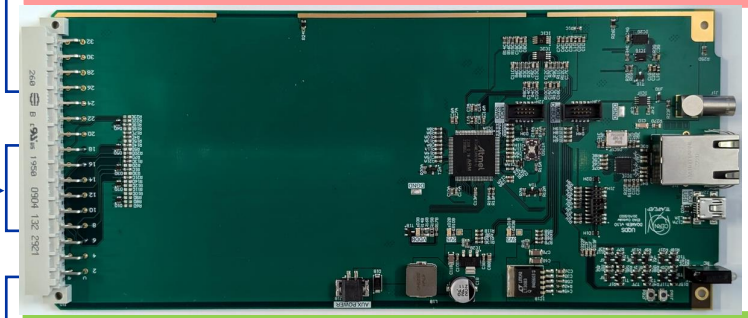


Insulated font-end channel

Up to 16 channels

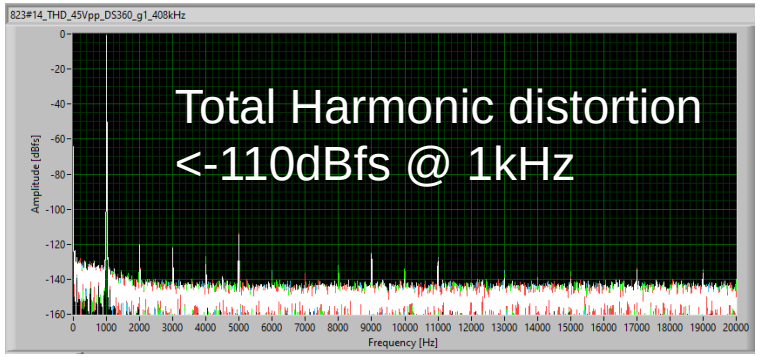
Passive mid-plane

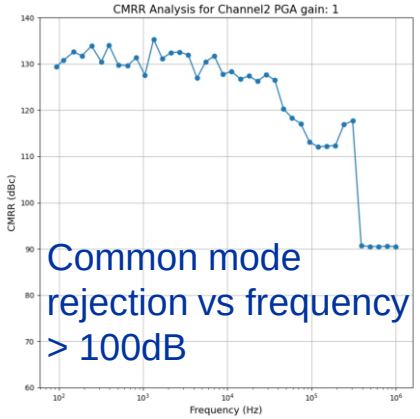


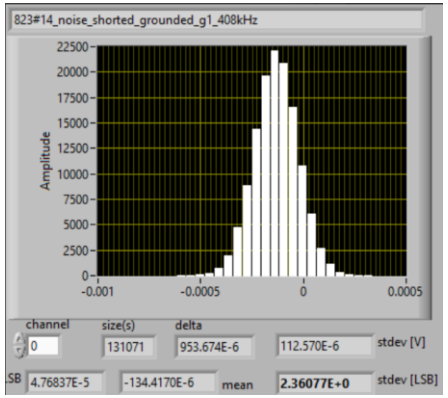


System performance

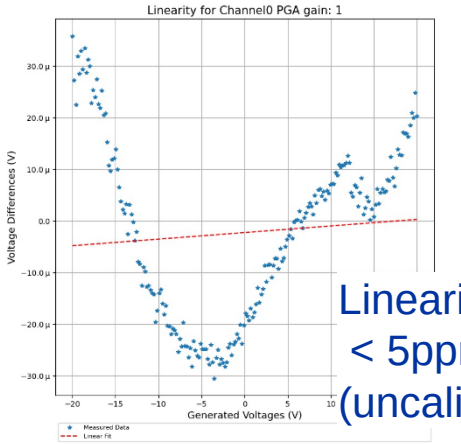
- **Excellent analogue performance both in AC and DC measurements**
- **Real time digital signal processing on FPGA (filters, gain/offset correction)**
- **Quench detection algorithms or other user code in FPGA**
- **Various interlocking options and standards (modular design)**
- **Post Mortem event recording**
- **Absolute time synchronization on microsecond level**
- **Fast logging up to 10kHz via EDAQ**







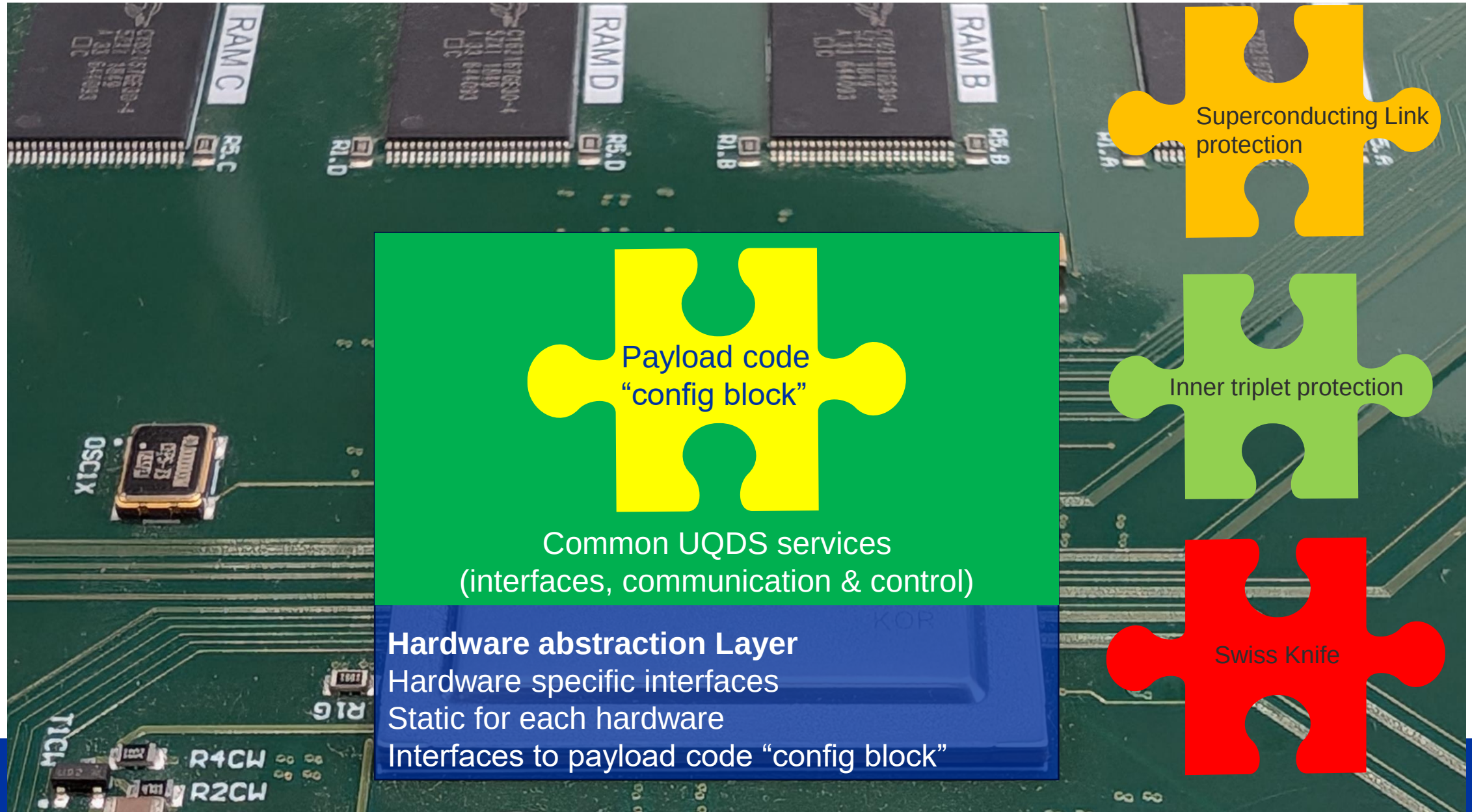
Noise: 2.3ppm
standard deviation



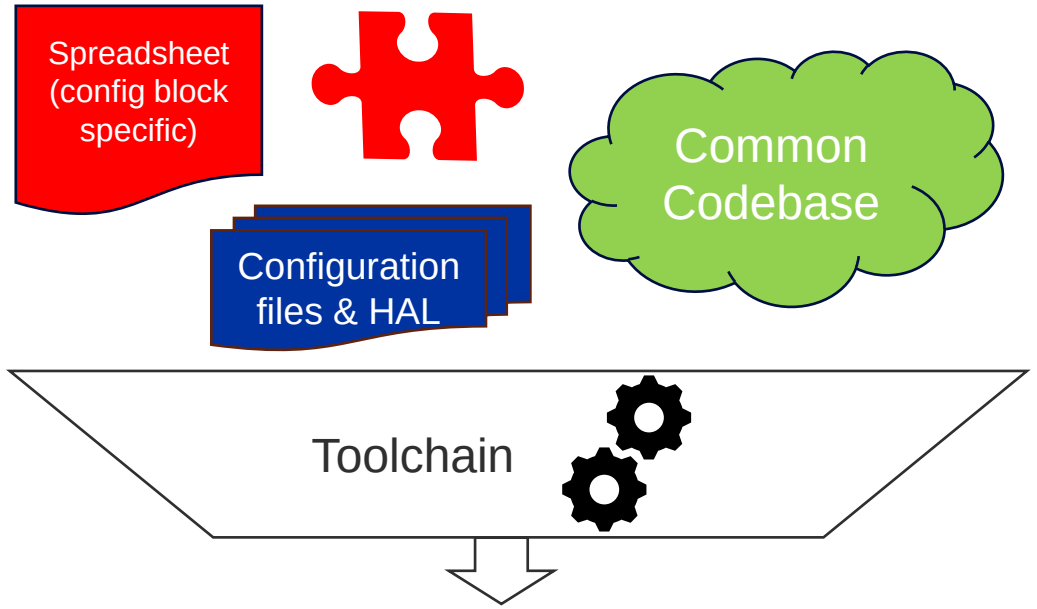
Linearity (calibrated):
< 5ppm
(uncalibrated ~0.1%)

Parameter	Value
Resolution (20-bit ADC)	105 nV/LSB .. 48 uV/LSB
ADC speed	Up to 909 kS/s
Analogue bandwidth	120 kHz @ G=1
Active input voltage range	+/-50 mV (G=450) .. +/-22.5 V (G=1) (1.2kV with divider)
Max differential input voltage	1 kV/1 s
Galvanic insulation	2.5 kV/1h, 5kV/1min

Gateware structure – One platform multi-purpose

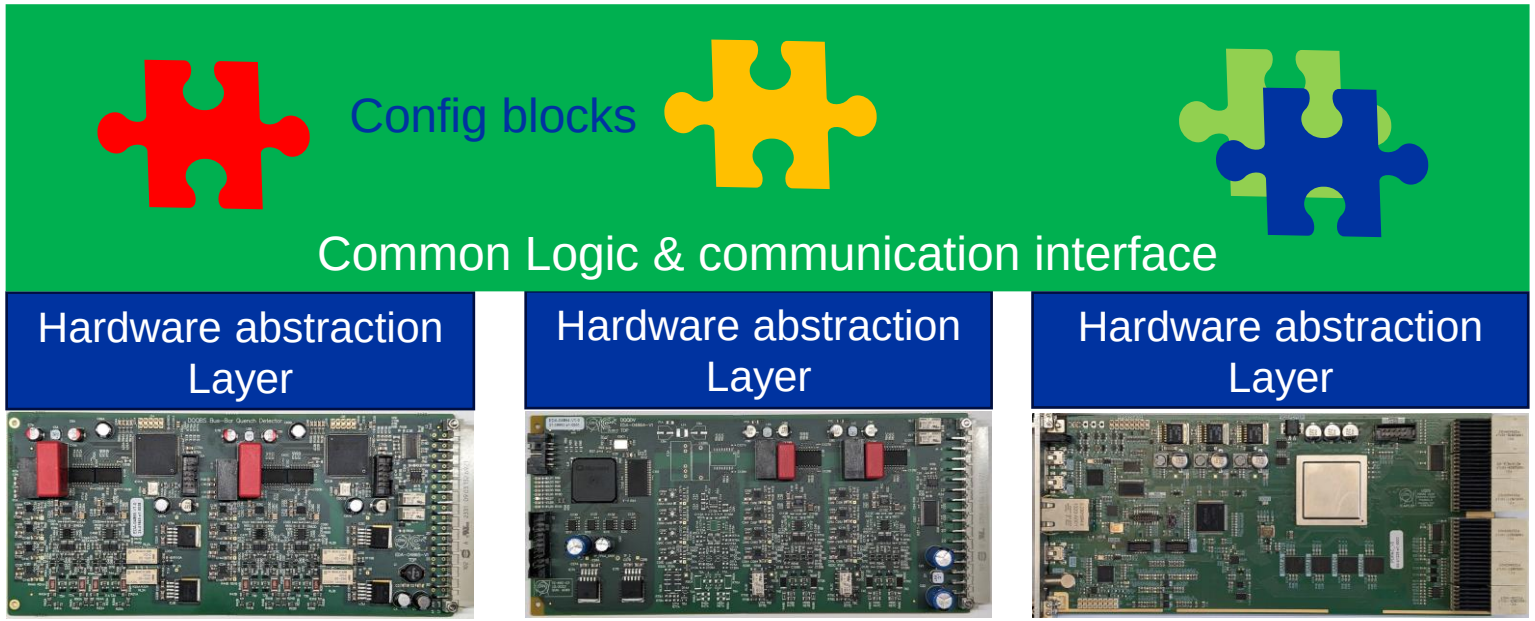


Multi-purpose Gateware on multiple Hardware



➔ Toolchain allows selection of target hardware and config block

- Gateware compiled from common code base
- Common Repository
- Application specific parts defined in HDL and Spreadsheet
- Automatic VHDL code generation for register map and interfaces
- Toolchain heavily scripted (Python & tcl)
- Hardware-in-the loop verification techniques

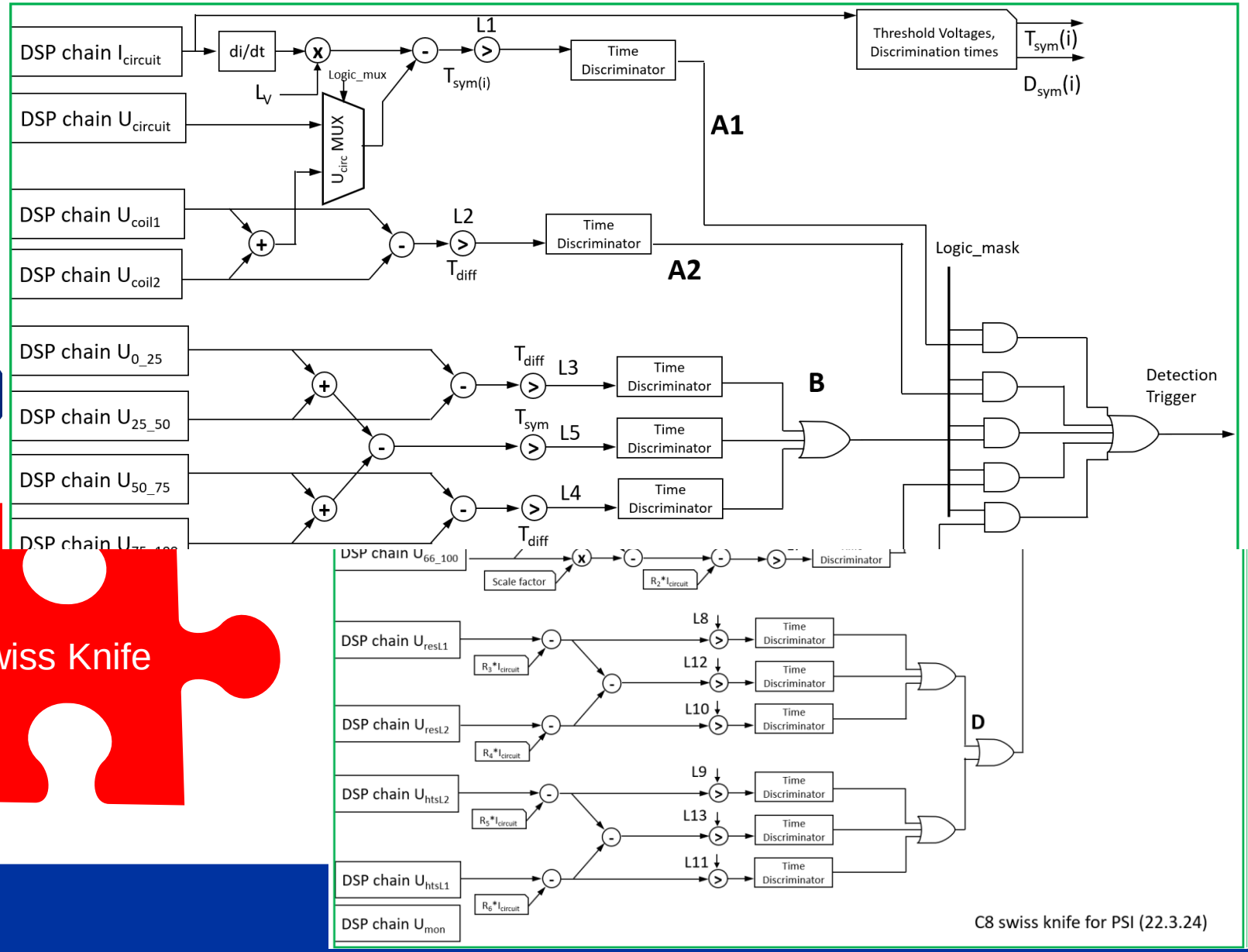


Gateware structure – “config block” examples

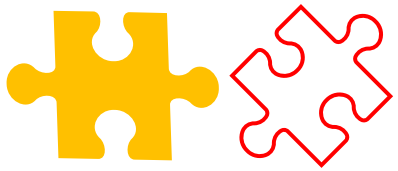
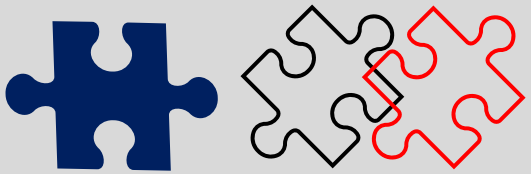
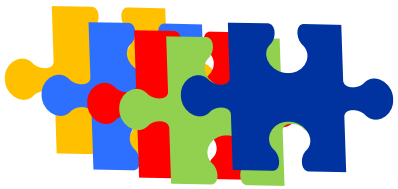
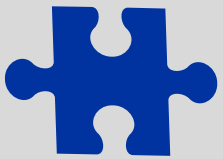
IT corrector Prot.

Q3 protection

Swiss Knife



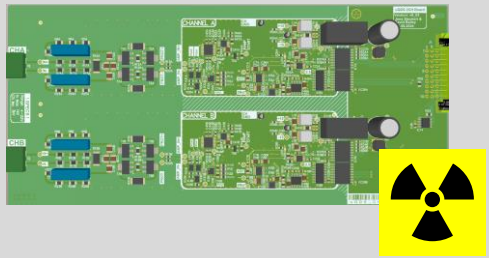
UQDS ecosystem (produced devices)

Image	Description	Configuration	Status
	Bus-bar and current lead monitor	 2 config blocks	120 boards produced Pilot installation in LHC
	Versatile quench detector board for LHC CONS	 3 config blocks planned	60 boards produced production of 630 boards pending
	UQDSv2 16 isolated channels	 27 configurations … and counting	~120 systems produced and in use (usage: see next slides)
	**P**rotection **D**evices **S**upervision **U**nit for HiLumi	 3 configurations planned	10 systems produced for IT STRING

UQDS ecosystem (in development/prototyping)

UQDS v3
Up to 32 isolated channels,
Faster acquisition speed
Optimized mechanics

Evolutionary upgrade of UQDSv2
Baseline for the HiLumi quench detection system
First prototype in final implementation stage



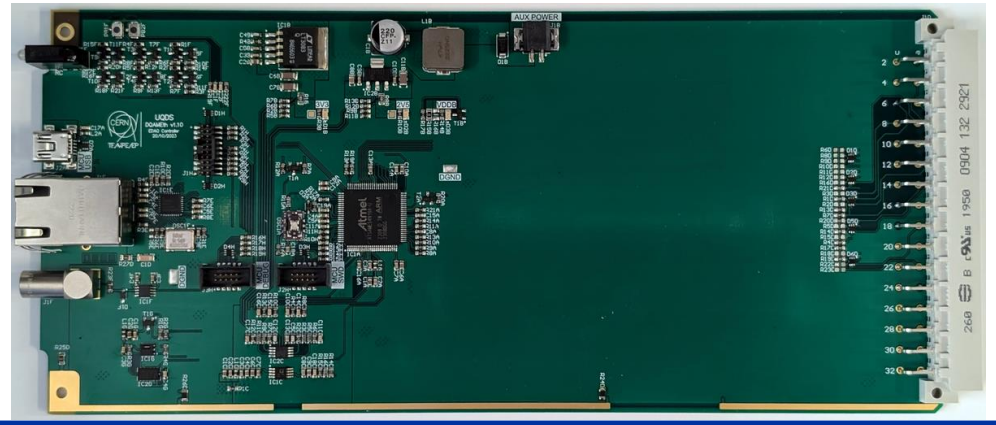
Upgrade of LHC dipole quench detection

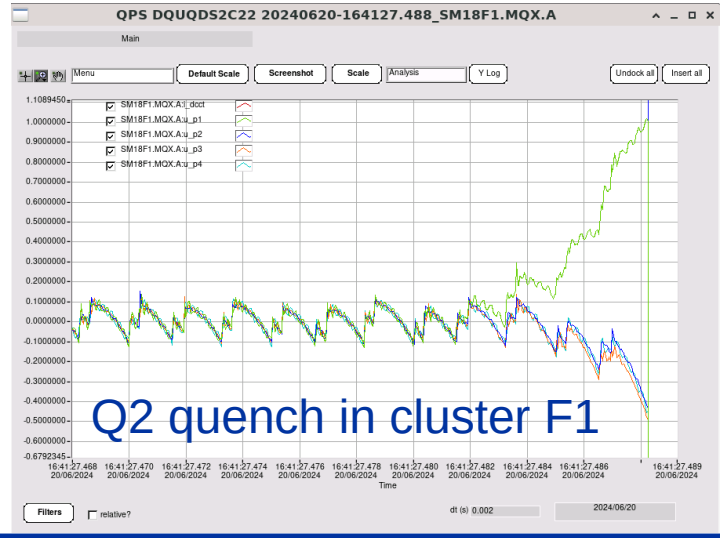
Big production of 2500 pieces to be installed at the end of LS3.
Variable threshold & radiation tolerant

➔ **Evolutionary upgrades and extensions of the ecosystem**

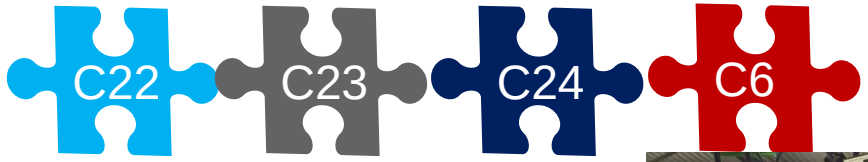
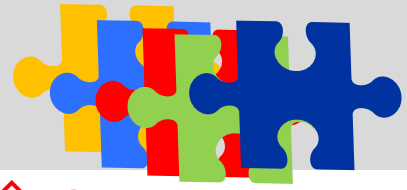
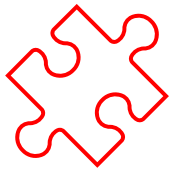
EDAQ – timing and communication for UQDS

- **Ethernet based solution with ~ 1000x the throughput compared to field bus used in LHC (~10Mbit per client)**
- **Timing precision > 1000x better than previous solution using ethernet precision timing protocol ➔ absolute precision better than 1us**
- **Fully integrated in CERN controls infrastructure**
- **Connects to services such as logging and post mortem**

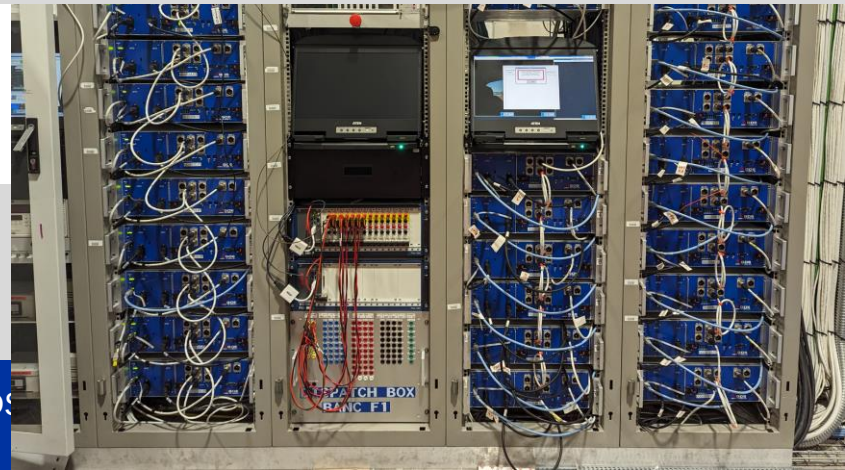




Applications at CERN

FAIR magnet test stand in B180	**18 x UQDSv2**	
FRESCA facility B163	**6 x UQDSv2**	
SM18 cluster F1 & F2 (HiLumi Q2 & SC Link testing)	**30 x UQDSv2**	
SM18 clusters A, B, C, D	**10 x UQDSv2**	
SM18 HiLumi STRING	**35 x UQDSv2**	 6 configurations
LHC tunnel	**8 x Busbar Monitor (more in TS#2)**	

➔ Full exploitation of flexible Gateware to follow the rich test program in SM18



Applications outside CERN

FREIA test facility
Uppsala Sweden

2x UQDSv2
For test of HiLumi magnets

PSI Villingen
Switzerland

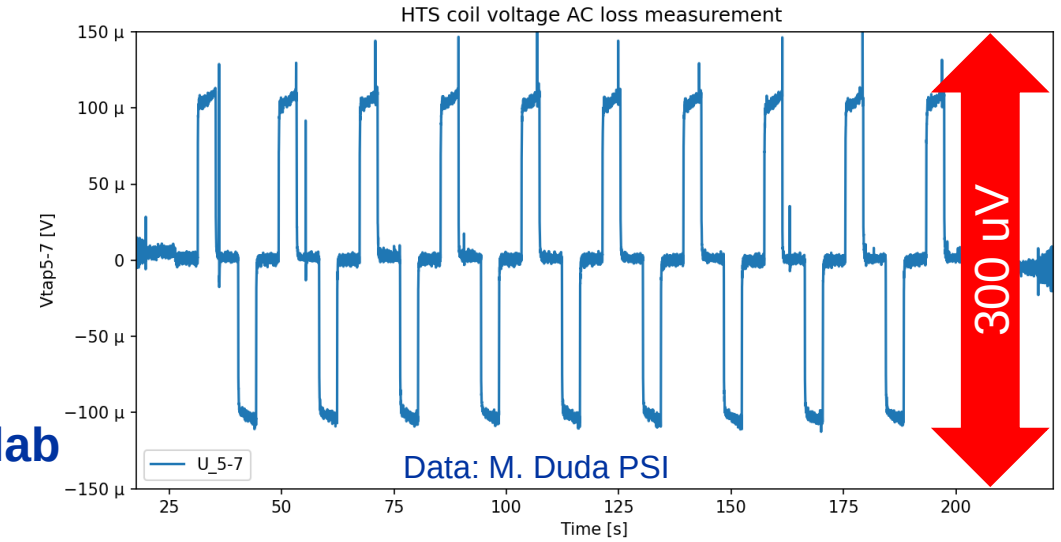
2x UQDSv2 for SC Magnet Lab
7x UQDSv2 quench detection of
SLS2.0 2x super bend magnet

C8

C16

IFJ PAN
Krakow Poland

2 x UQDSv2

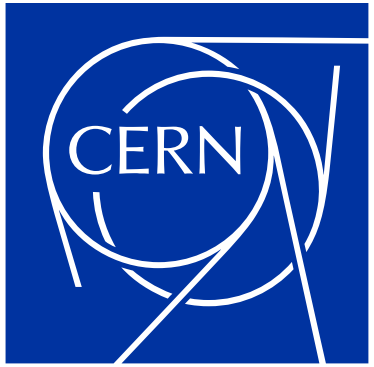


➔ **INFN LASA (Milano) showed interest in UQDS for their test lab**

Summary

- **Established platform with full system integration in CERN controls services**
- **Inhouse solution with full control about all elements**
  → We can cope with obsolescence etc…
- **Quite unique feature set**
  - High performance measurement channels with galvanic insulation of ~5kV peak
  - FPGA for real time processing of data & hardware interlocks
- **Flexible adaptable design which can serve many purposes**
- **Focus now in completion of units for IT STRING**

➔ We’re open for new applications



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