MAPS Simulations with Hexagonal Pixel Designs

The TANGERINE collaboration at DESY

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September 2, 2024

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TANGERINE

TANGERINE (Towards Next Generation Silicon Detectors) Work Package 1 (WP1) aims the development of 65 nm CMOS MAPS (Monolithic Active Pixel Sensor) for future lepton collider and test beam telescopes.

(by simulations and prototype chip tests)

	(HL-) LHC (ATLAS/CMS)	**Future Lepton Colliders**
Material budget	10% X_0	< 1% X_0
Single-point resolution	~ 15 μm	≤ 3 μm
Time resolution	25 ns	~ ps – ns
Granularity	50 μm x 50 μm	≤ 25 μm x 25 μm

S. Spannagel, 93rd PRC

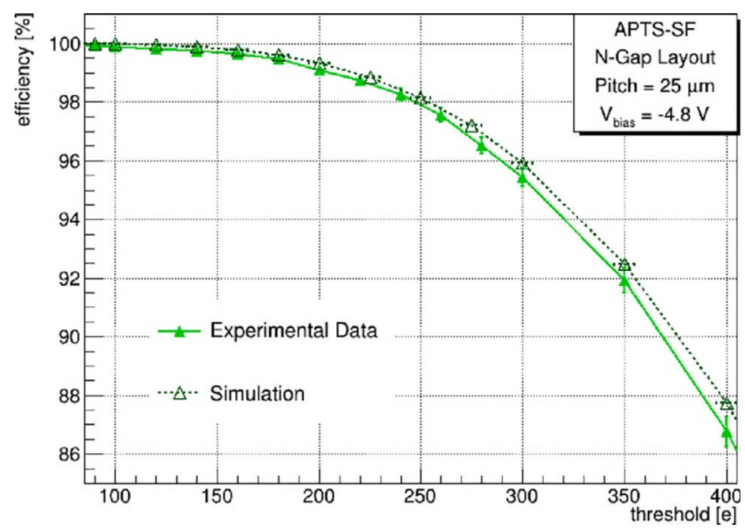
TANGERINE chip requirements

Parameter	Value
Single-point resolution	$< 3\ \mu m$
Time resolution	< 10 ns
Granularity	$< 25\ \mu m \times 25\ \mu m$
Particle rate	1 MHz
Material budget	$< 0.05\%\ X_0$

Main simulation studies

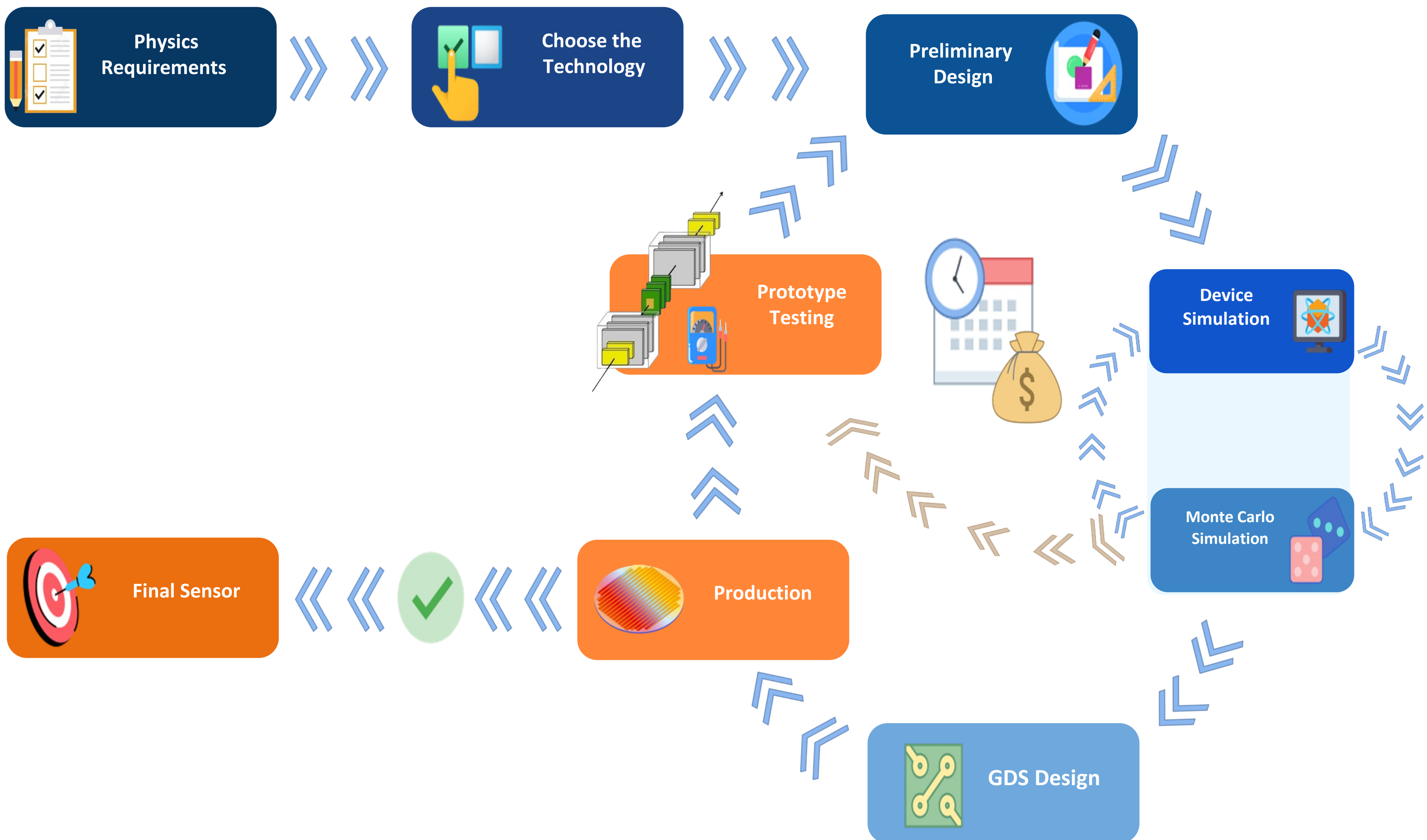
- Simulation of square MAPS in different sizes and layouts
- Simulation of hexagonal MAPS in different sizes and layouts
- Transient simulation for timing performance

Prototype chip measurements are compared to the simulation results.



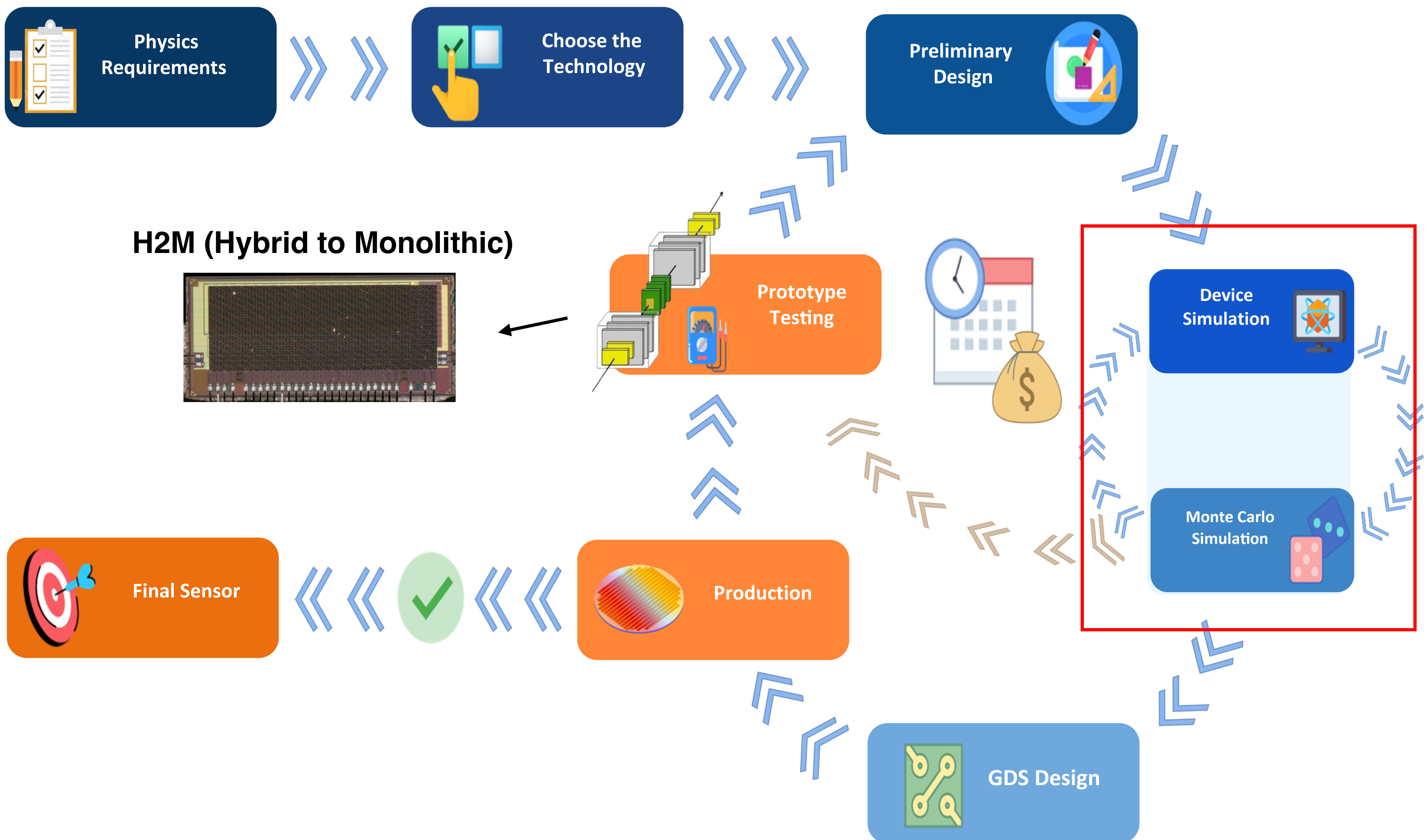
A. Simancas et al., https://doi.org/10.1016/j.nima.2024.169414

Development Flow



L. Mendes

Development Flow



L. Mendes

Because of the limited manufacturing process information,

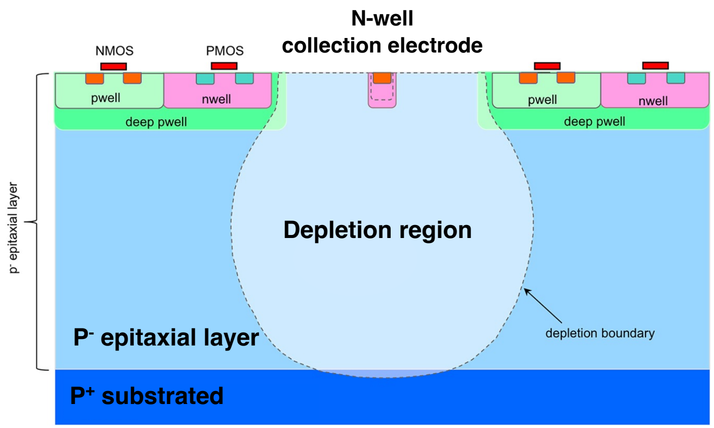
we take a technology-independent simulation approach with generic numbers.

Monolithic Active Pixel Sensor (MAPS)

- P-type substrate
- Reverse bias voltage
- Not fully depleted

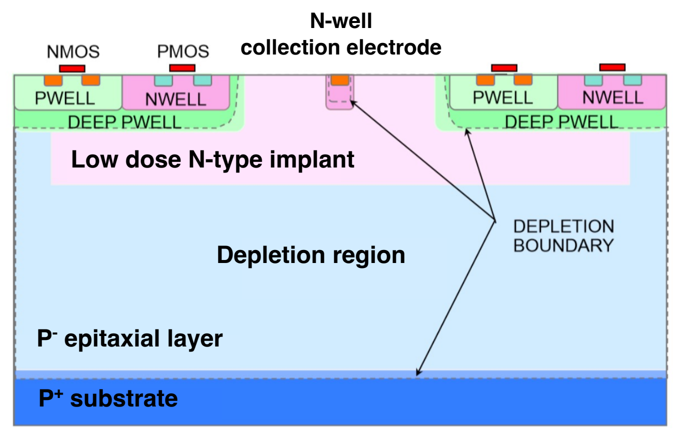
** Not to scale

Standard layout



https://doi.org/10.1016/j.nima.2017.07.046

N-gap layout



https://doi.org/10.3390/instruments6040051

- ❑ P-type epitaxial layer (epi-layer) with lower doping concentration than p-type Si substrate
→ **high-resistivity, depletion region***

- ❑ Small n-well collection electrode

- ❑ Employing commercial CMOS circuitry for readout electronics (NMOS, PMOS)
→ **low material budget, compactness**

- ❑ N-gap: low dose n-type implantation
→ **larger depletion region, higher efficiency**

* Depletion region (backup #31)

Let's think about the PN junction.
We can assume that there're **no mobile charge carriers** in the middle of the n-side and p-side.
Any electron or hole entering this area **will be swept out by the electric field**.
→ In this area, charges **move by drift not by diffusion.**
It attracts charges fast and strongly.
When the **reverse bias** is applied to the PN diode, **depletion region gets wider.**

Doping Concentration and Electric Field

Sentaurus TCAD

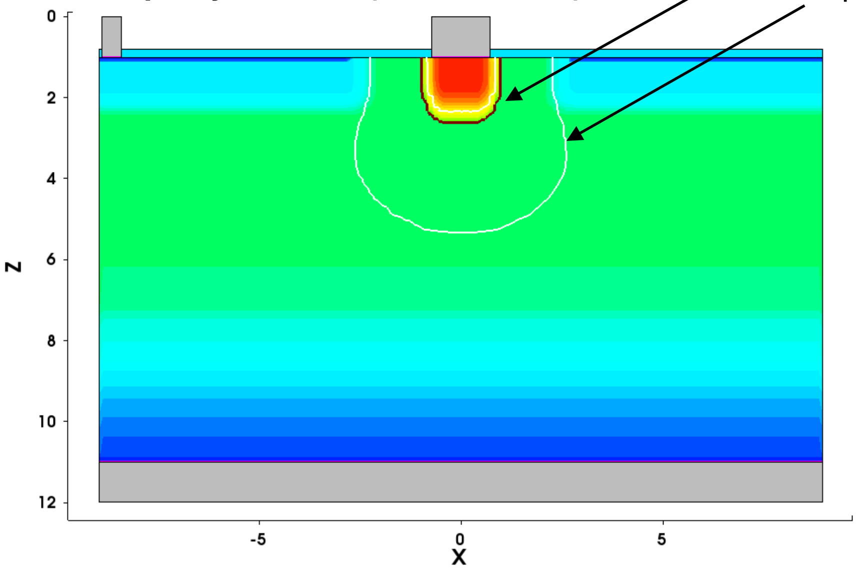
SYNOPSYS

Dopling concentration

Standard, epi-layer 10 μm (axis unit: μm)

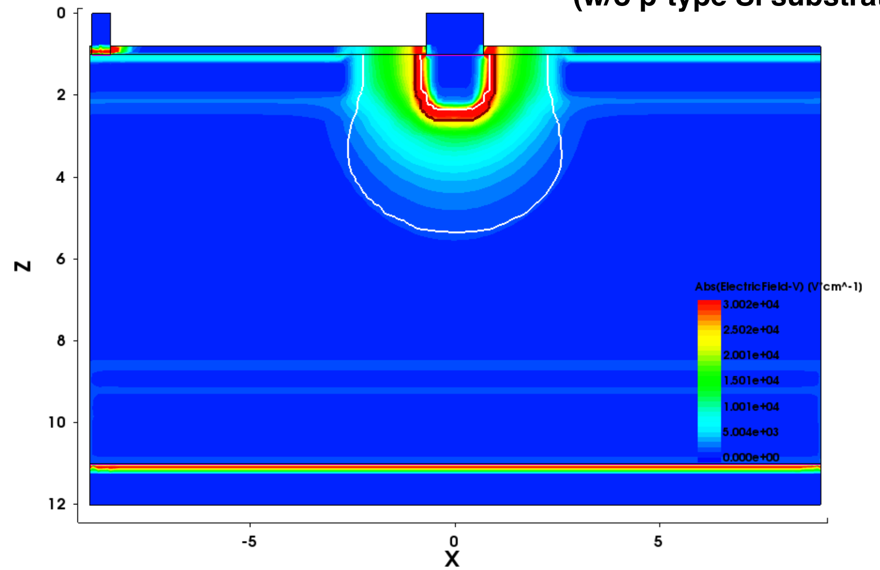
Junction line

Depletion line

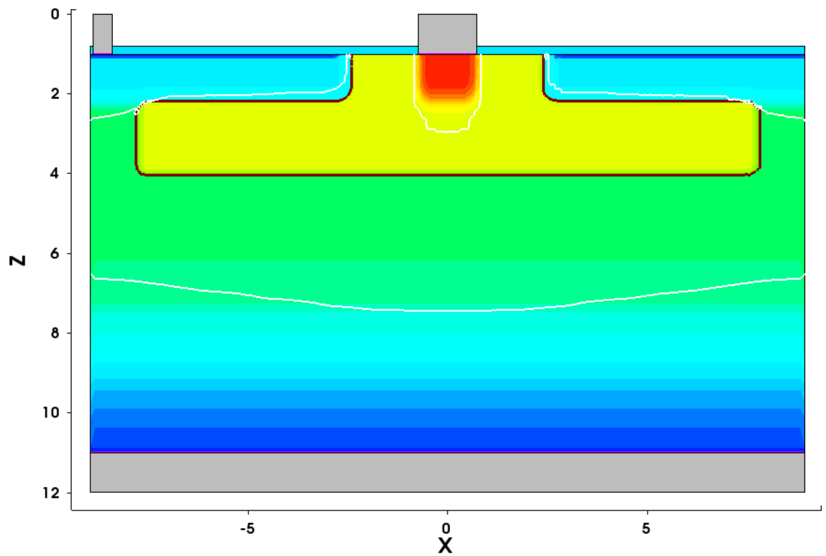


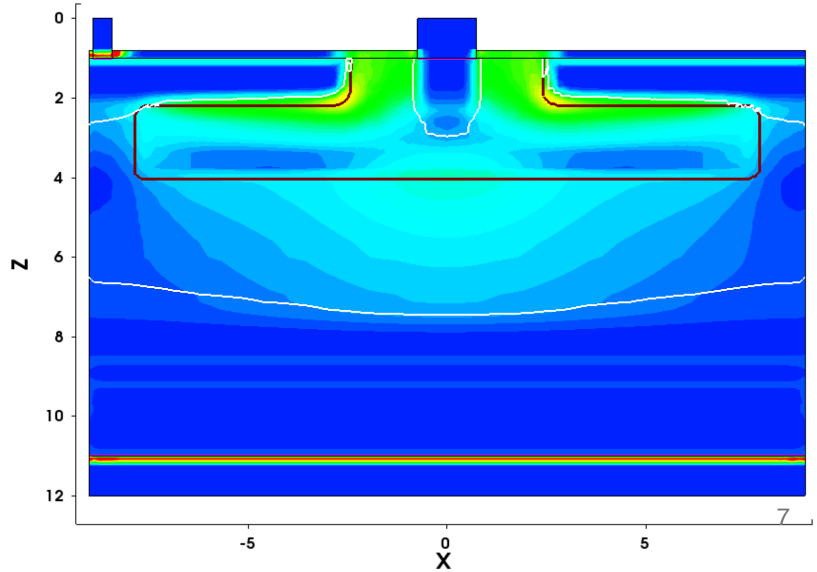
Electric field

Run by L. Mendes (w/o p-type Si substrate)



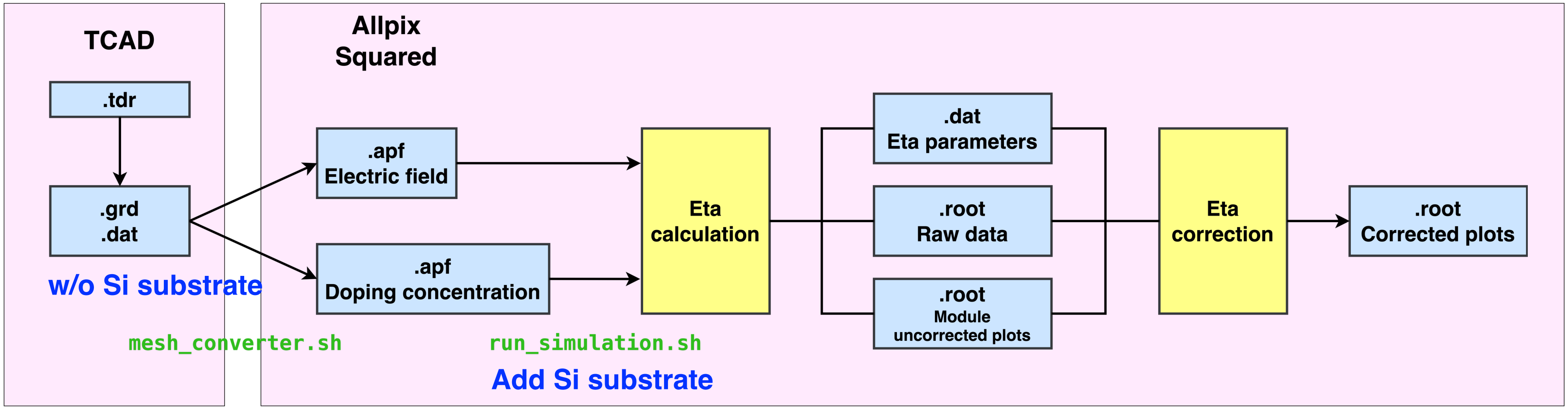
N-gap, epi-layer 10 μm





Simulation

Data flow in Allpix²

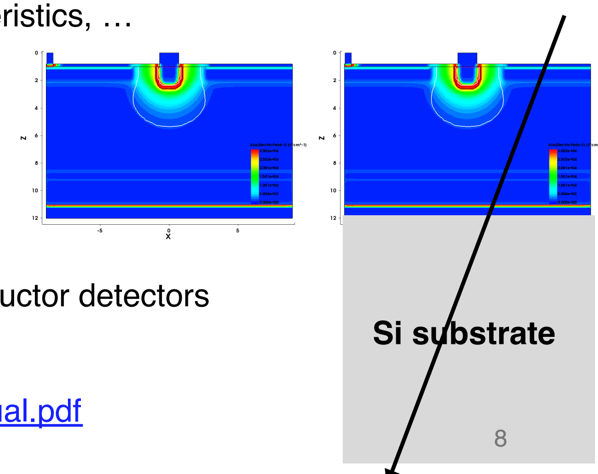


Sentaurus TCAD

SYNOPSYS

- **SProcess**: fabrication process simulation
- **SDevice**: simulates numerically the electrical behaviour of a single semiconductor device
- **SDE**: 2D and 3D device structure editor, geometric operations

→ Doping concentration, electric field, mobility, electrical characteristics, …
https://www.synopsys.com/manufacturing/tcad.html



ap² allpix squared

Monte Carlo simulations
for semiconductor tracker and vertex detectors

- Simulation of **charge deposition and transport** in semiconductor detectors
- **Digitization** to hits in the frontend electronics
- Using **Geant4 and ROOT**

https://project-allpix-squared.web.cern.ch/usermanual/allpix-manual.pdf

Figures of Merit (FOM)

: A quantity to characterize the performance of the MAPS

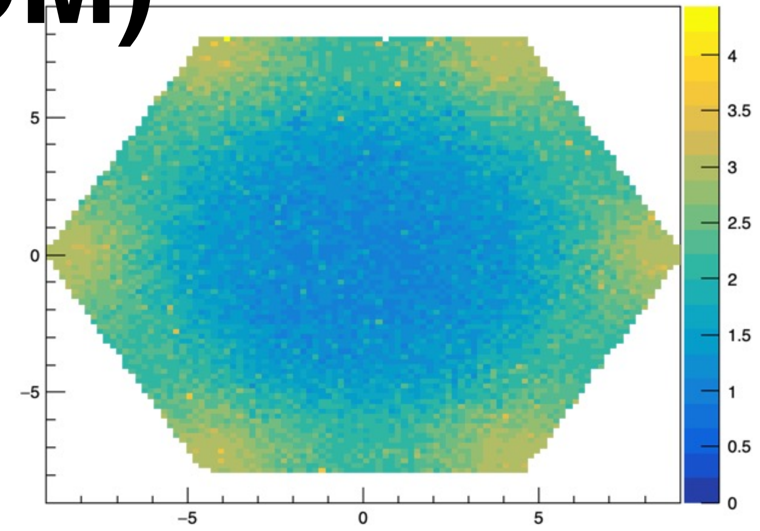
1. Cluster size

- ❑ Number of pixels in each reconstructed cluster (> 1)

- ❑ Shows the degree of charge sharing

→ Larger cluster size means higher charge sharing

- ❑ Mean cluster sizes across the full pixels are in the graphs.



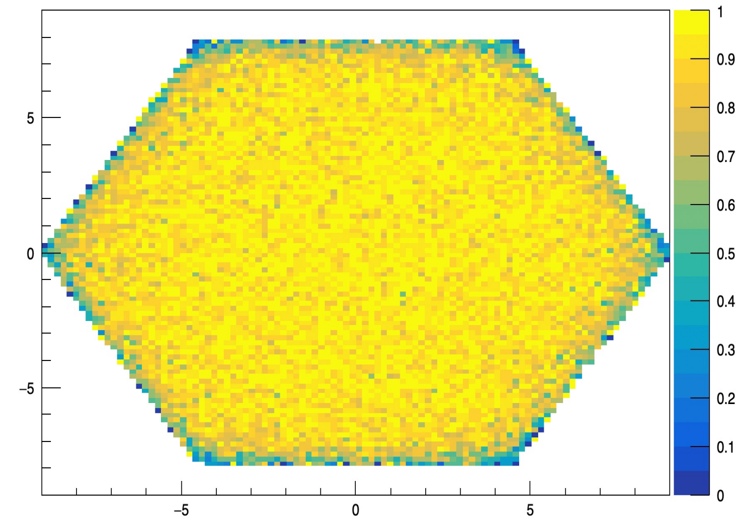
Cluster map

2. Efficiency

- ❑ How many particles generate signals compared to the number of the incident particles.

- ❑ 0 ~ 1 (or 0 ~ 100 %)

- ❑ Mean efficiency across the full pixel are in the graphs.

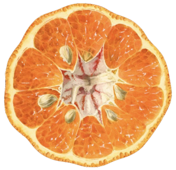


Efficiency map

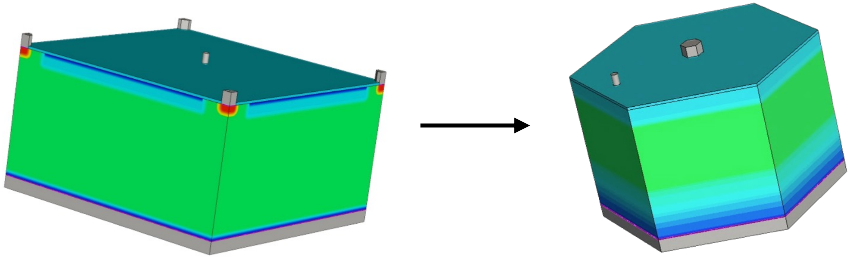
3. Spatial resolution

- ❑ Difference between reconstructed cluster position and real particle position (residual)

Motivation



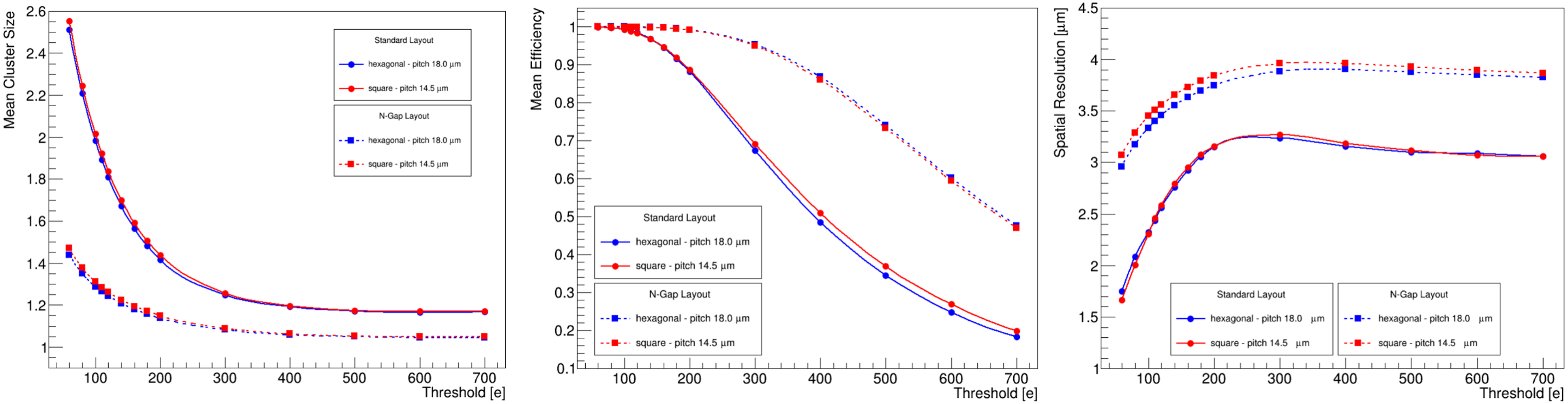
**As a part of the TANGERINE WP1,
we study the possibility of using hexagonal pixels.**



A. Simancas and L. Mendes

Hexagonal pixels

- ❑ Fewer number of neighboring pixels
- ❑ Reduced electric field effects from corners
- ❑ Reduced path between the corner and the electrode in the same area of pixels

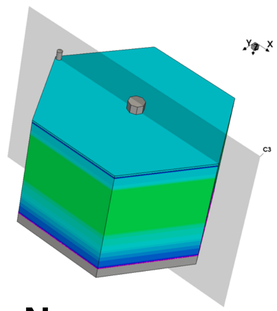


L. Mendes

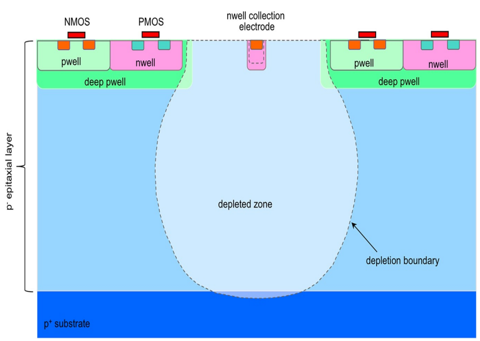
- ❑ The difference between square and hexagonal pixels is not significant because of the thin epi-layer (10 μm).

→ Additional study for comparing the epi-layer thickness with pitch and layout changes

Simulation Setup

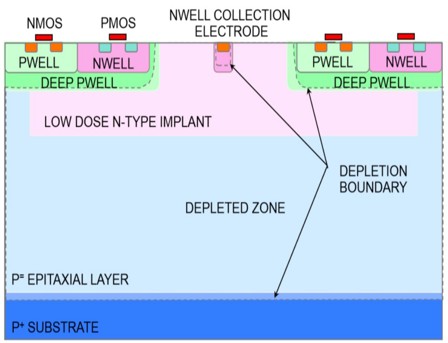


Standard



https://doi.org/10.1016/j.nima.2017.07.046

N-gap



https://doi.org/10.3390/instruments6040051

Simulation type
Electrostatic

Incident particle
5 GeV electron beam

Geometry
Hexagonal

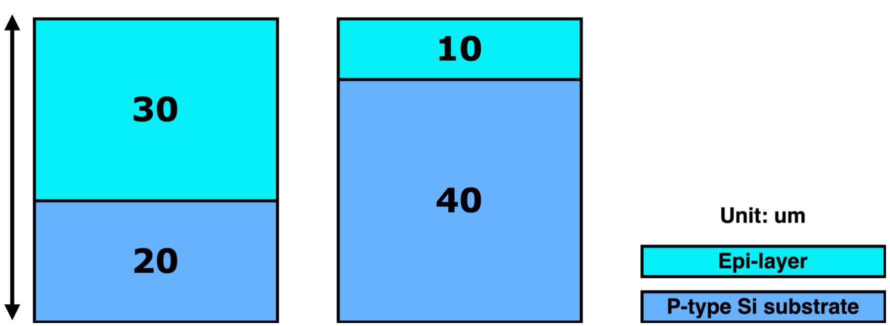
Events
100,000

Voltage supply
Collection electrode 1.2 V
Backside electrode -1.2 V
Contact electrode -1.2 V

Pitch
10.00 μm
18.00 μm
25.00 μm

Layout and epi-layer
Standard, Epi 30 μm
Standard, Epi 10 μm
N-gap, Epi 30 μm
N-gap, Epi 10 μm

Sensor thickness



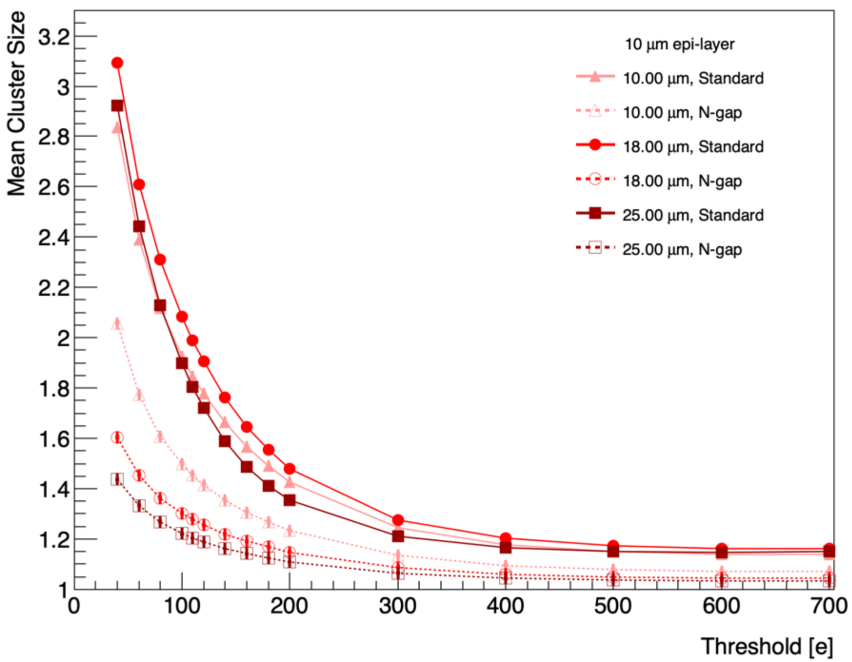
1. Pitch and layout comparison
at 10 μm epi-layer

2. Epi-layer and layout comparison
at 18.00 μm pitch

+ Integration time comparison
25 ns
40 ns
5 μs

Pixel size and Layout Comparison
(10 μm epi-layer)

Cluster Size



25.00 μm pitch has smaller cluster size for both layouts.

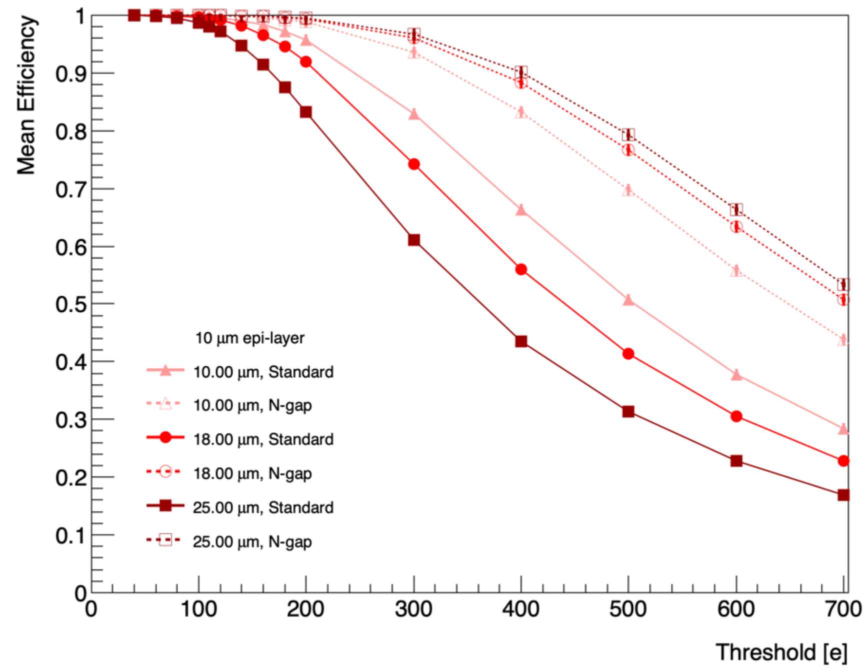
N-gap

- N-gap has smaller cluster size (less charge sharing) *as expected*
- Cluster sizes are inversely proportional to the pitch.

Standard

- Cluster sizes are not proportional to the pitch.

Efficiency

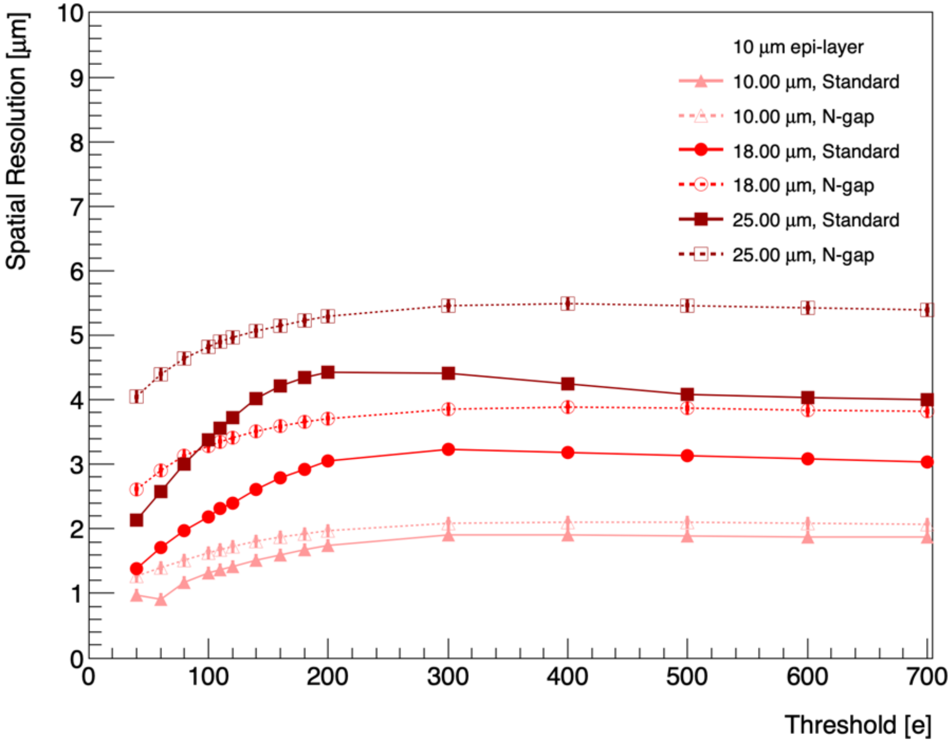


The highest efficiency in 25.00 μm N-gap

- N-gap has higher efficiency than Standard *as expected.*
- N-gap efficiency is proportional to pitch size.
- Standard efficiency is inversely proportional to pitch size.

*** More details are in the slide #23 (backup)*

Residual in X: Spatial Resolution
(10 μm epi, multiple pitch sizes)



No significant differences between X and Y *as expected.*

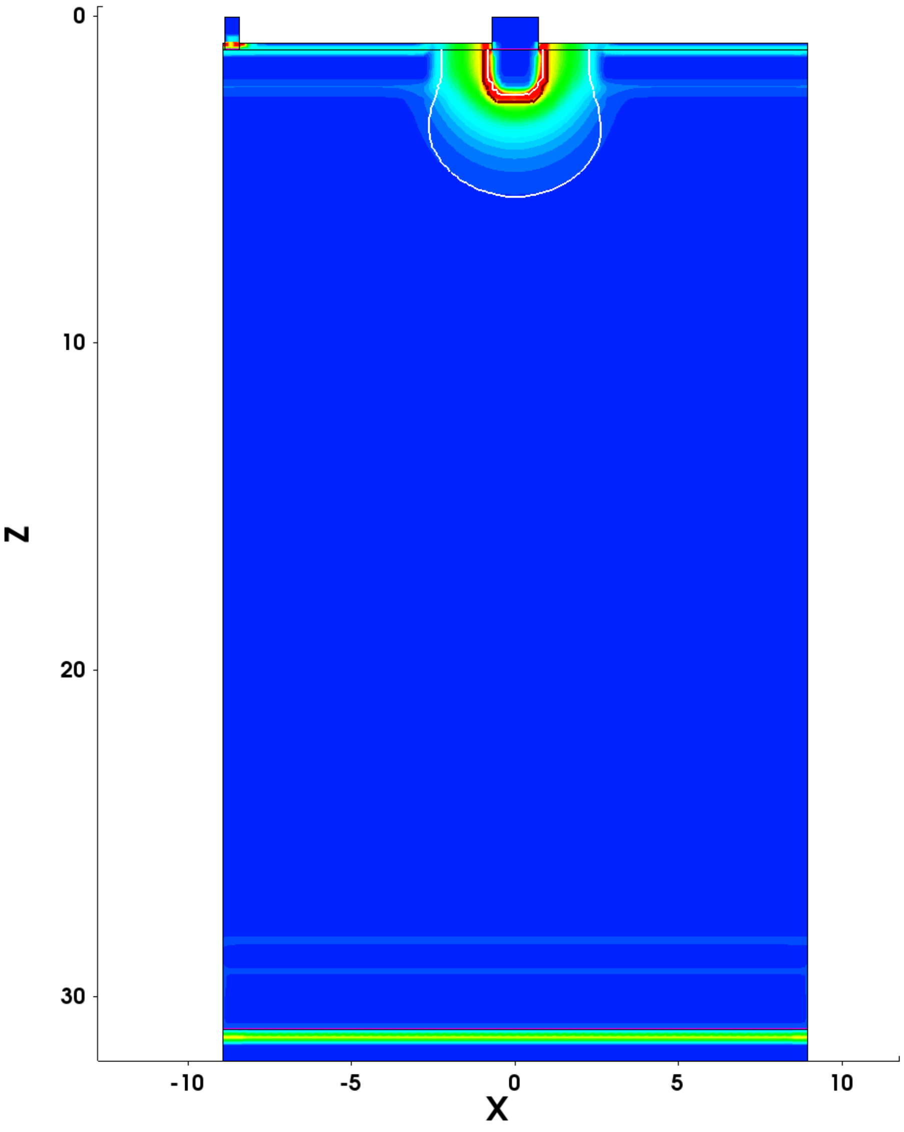
- Standard has higher spatial resolution than N-gap *as expected.*
- If we use the smaller pitch we can overcome the layout differences *as expected*.

N-gap is more stable under 200e threshold.

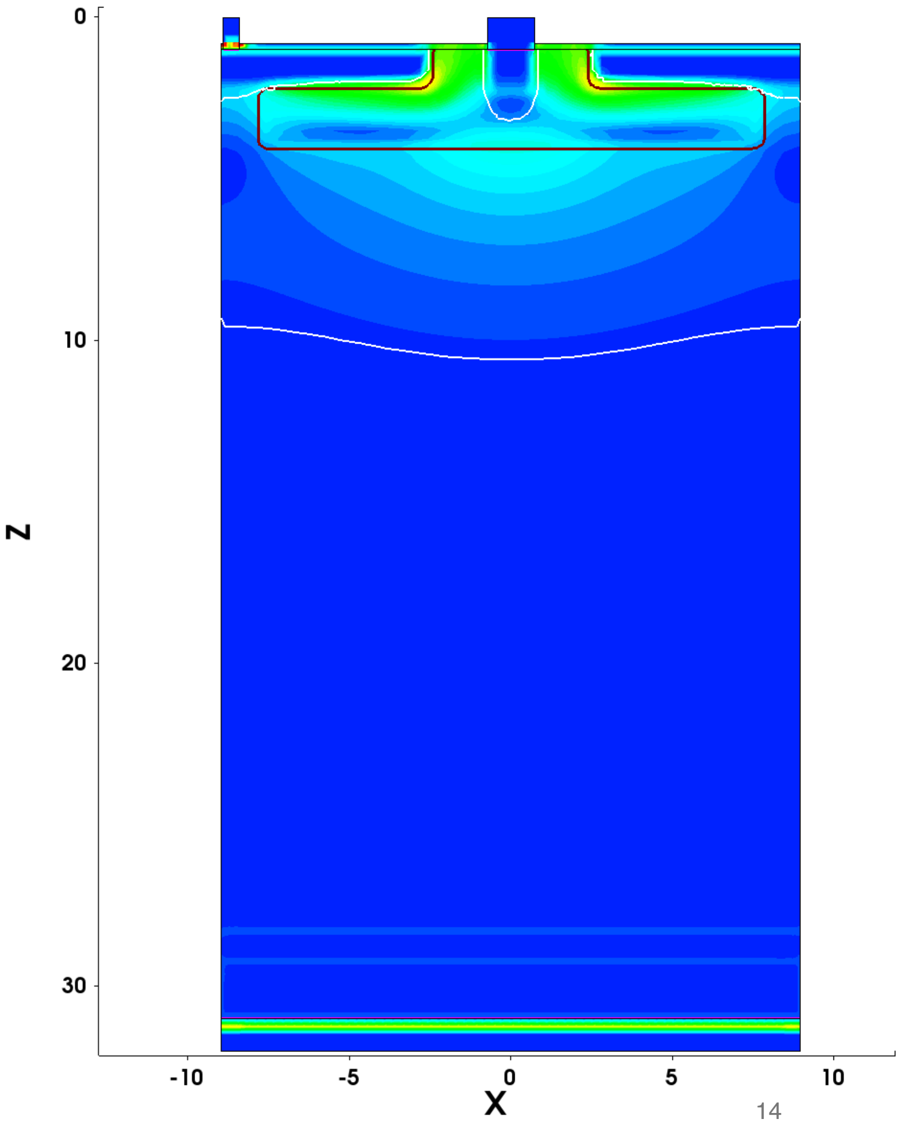
Electric Field in 30 μm Epi-layer

Run by Larissa Mendes
(w/o p-type Si substrate)

Standard (axis unit: μm)



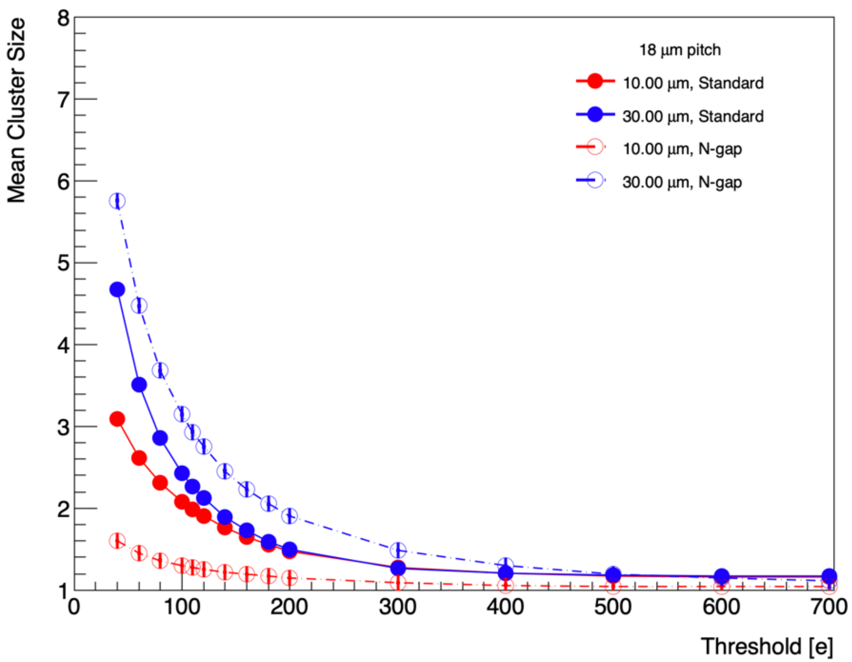
N-gap



Epitaxial Layer and Layout Comparison

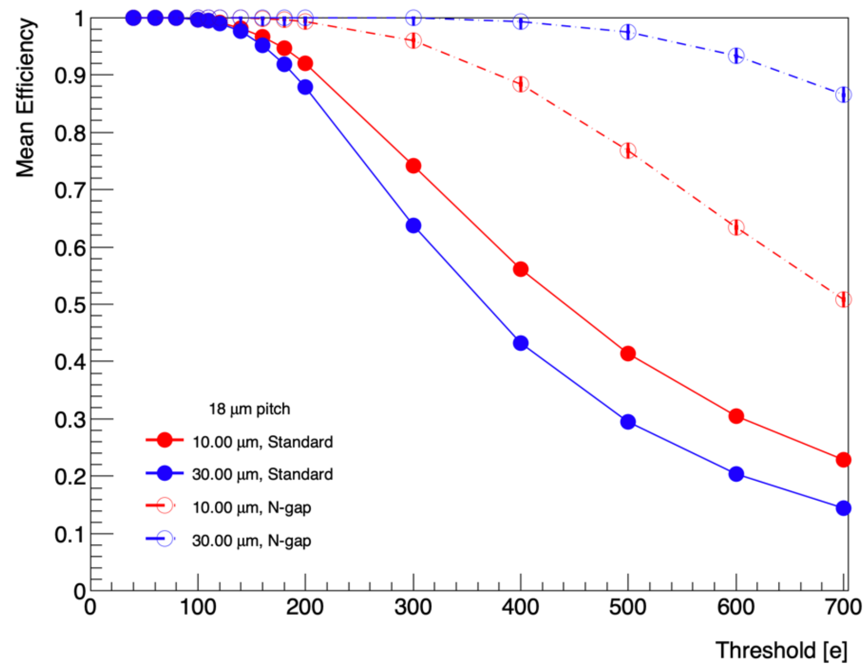
(18 μm pitch, 25 ns integration time)

Cluster Size



○ 10 μm has smaller cluster size than 30 μm.

Efficiency



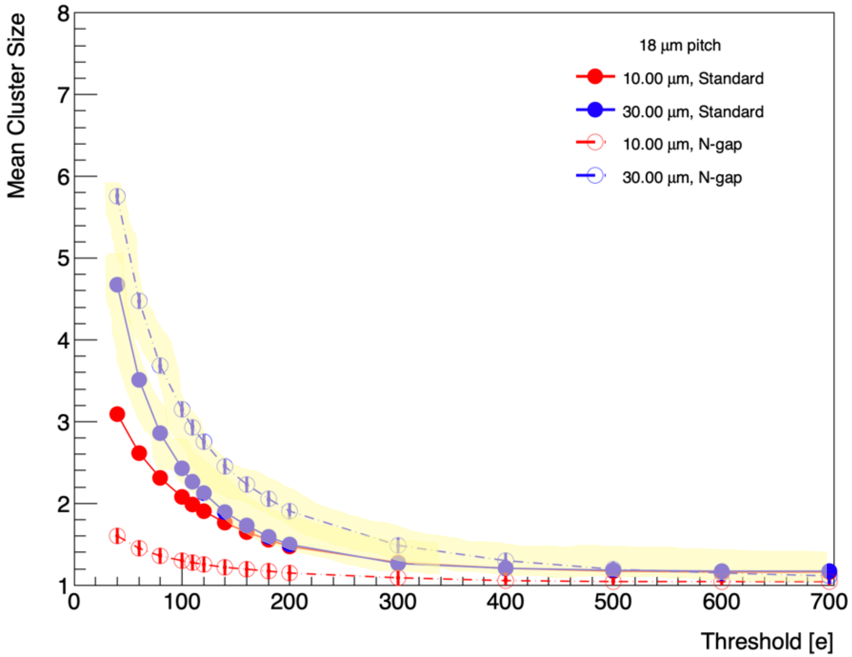
○ The highest efficiency in 30 μm N-gap

○ N-gap has higher efficiency than Standard.

Out of Expectation

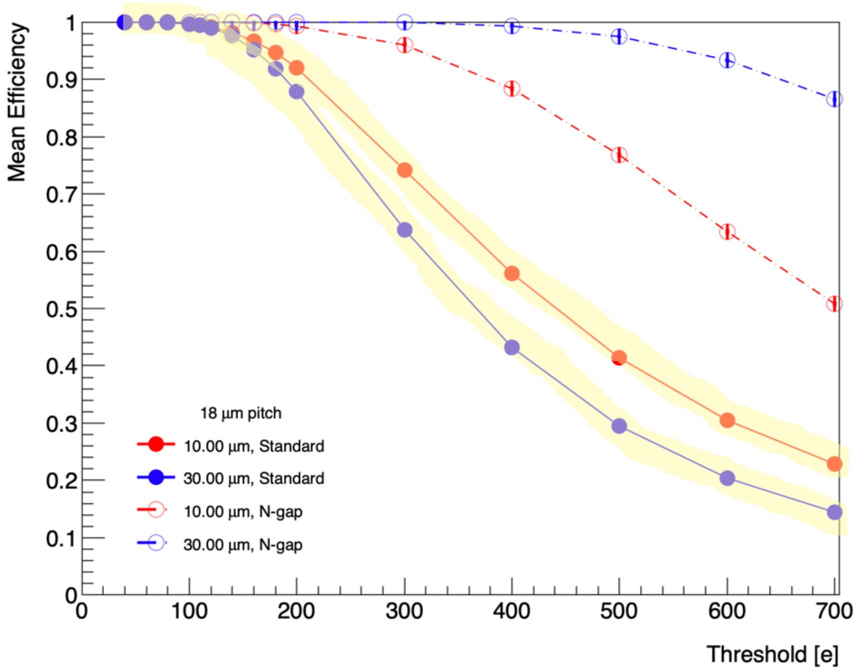
(18 μm pitch, 25 ns integration time)

Cluster Size



- 10 μm has smaller cluster size than 30 μm.
- **In 30 μm, N-gap has bigger cluster size than Standard.**

Efficiency

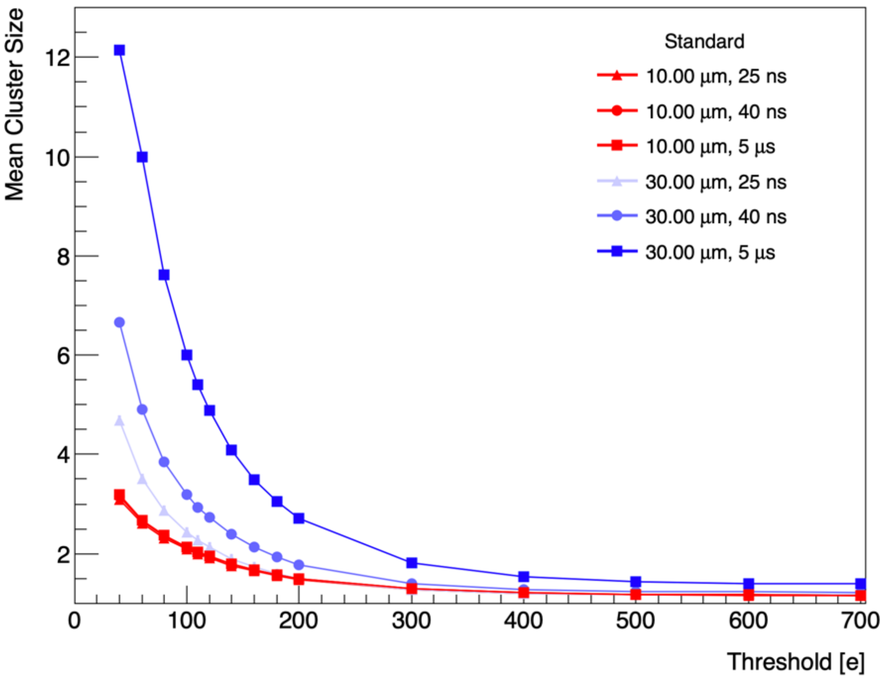


- The highest efficiency in 30 μm N-gap
- N-gap has higher efficiency than Standard.
- **In Standard, 10 μm is more efficient than the 30 μm.**

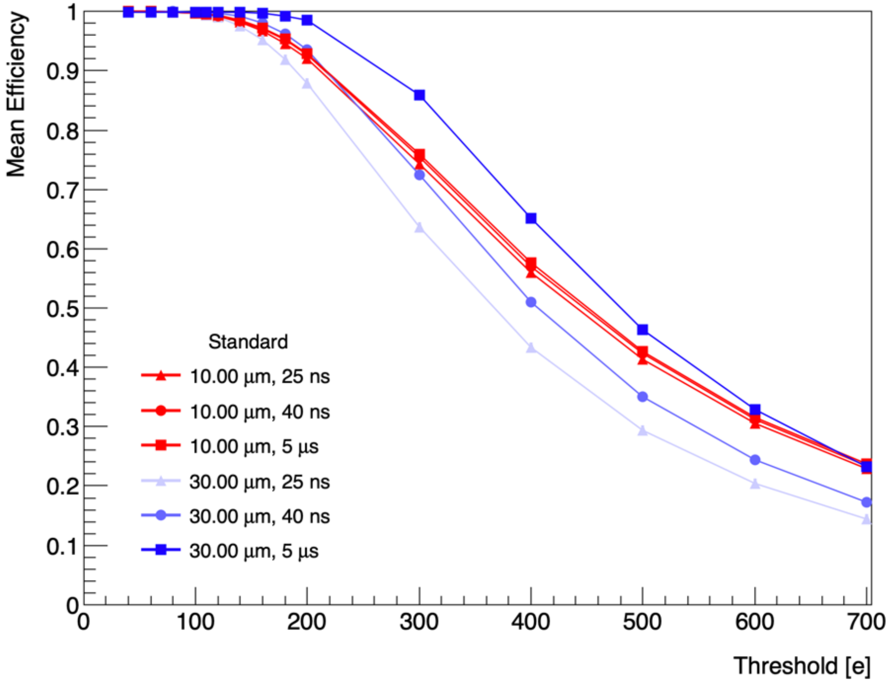
Integration Time Comparison

: 25 ns, 40 ns, 5 μs in both epi-layer (standard, 18 μm pitch)

Cluster Size



Efficiency



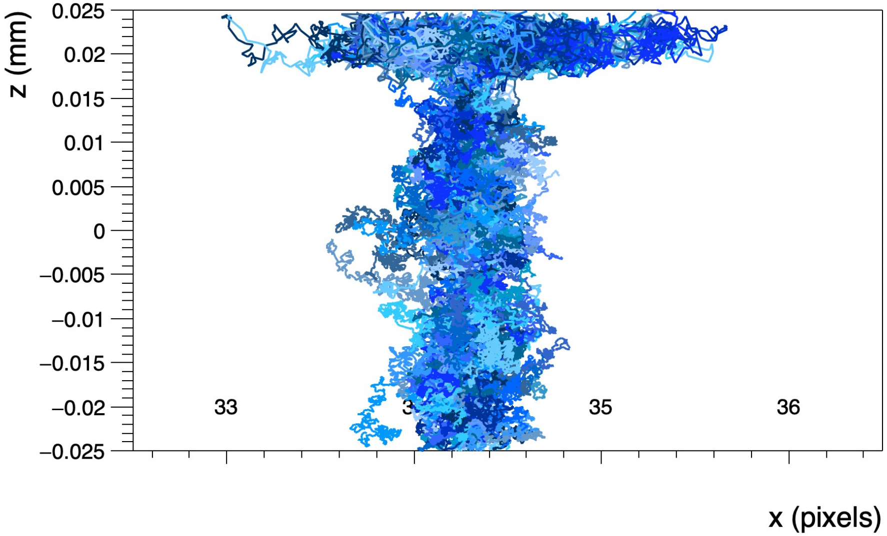
(No significant change in 10 μm epi-layer.)

- **In 30 μm, cluster size and efficiency increases with the integration time.**
- 30 μm exceeds 10 μm in efficiency at 5 μs.

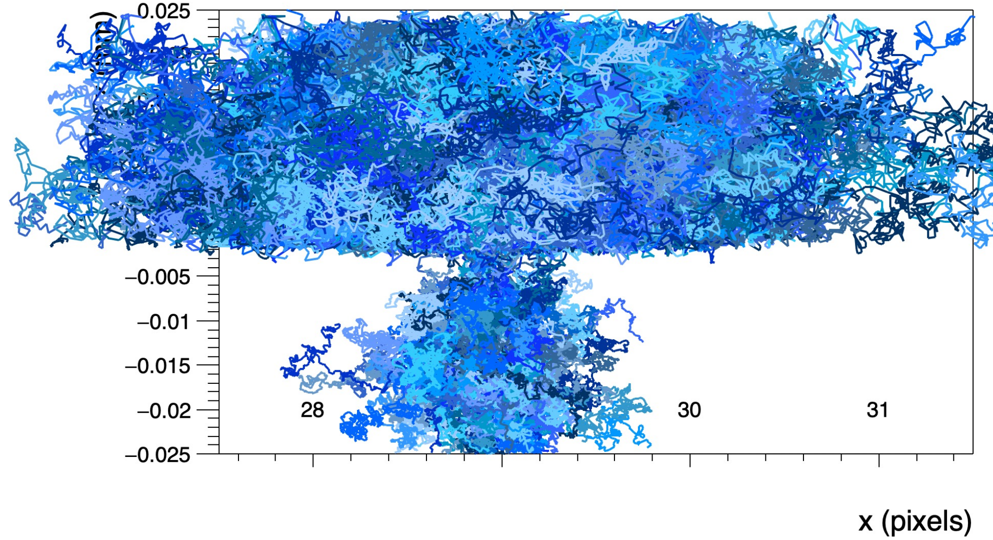
Linegraphs for Standard (40 ns)

Threshold: 60e

10 μm epi-layer

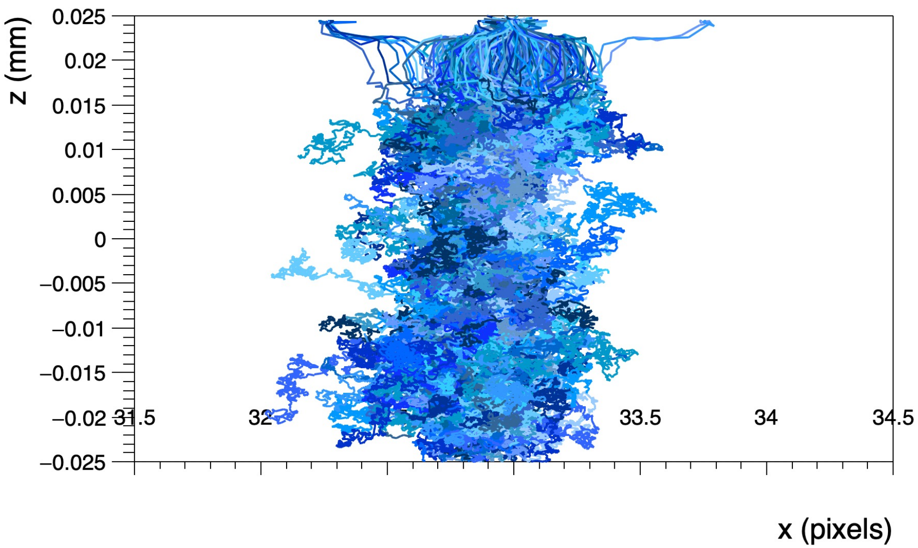


30 μm epi-layer

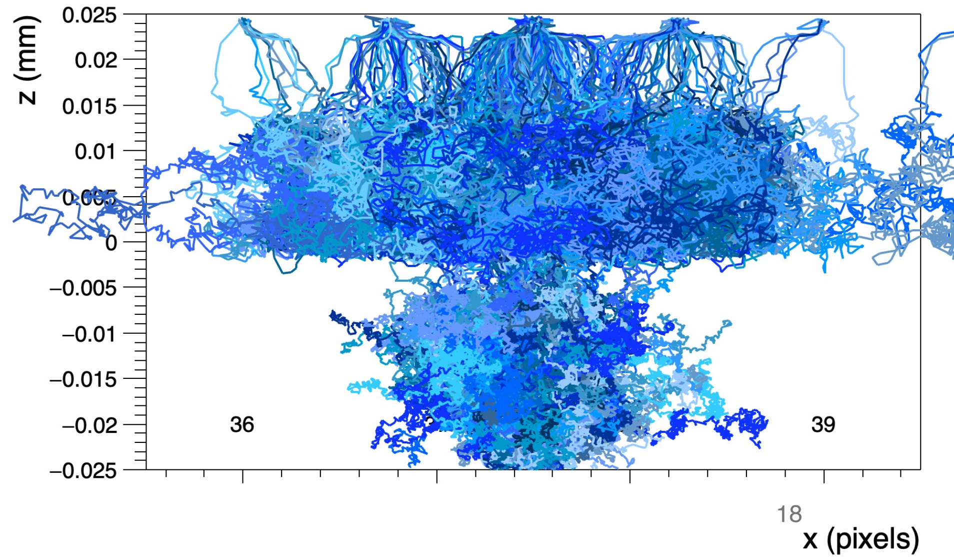


Linegraphs for N-gap (40 ns)

10 μm epi-layer



30 μm epi-layer

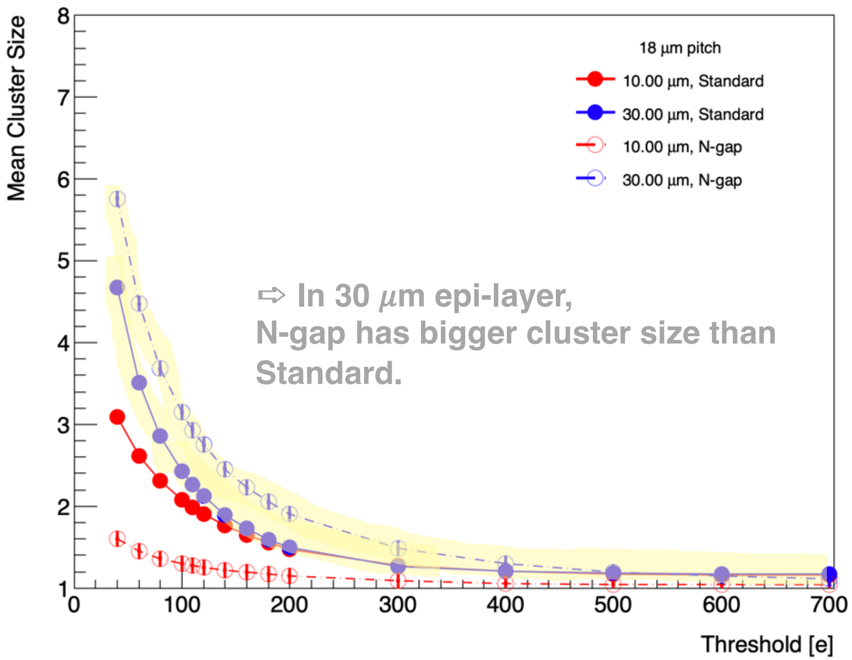


Now We Can Understand ..

(10 and 30 μm epi-layer, 18 μm pitch)

Cluster Size

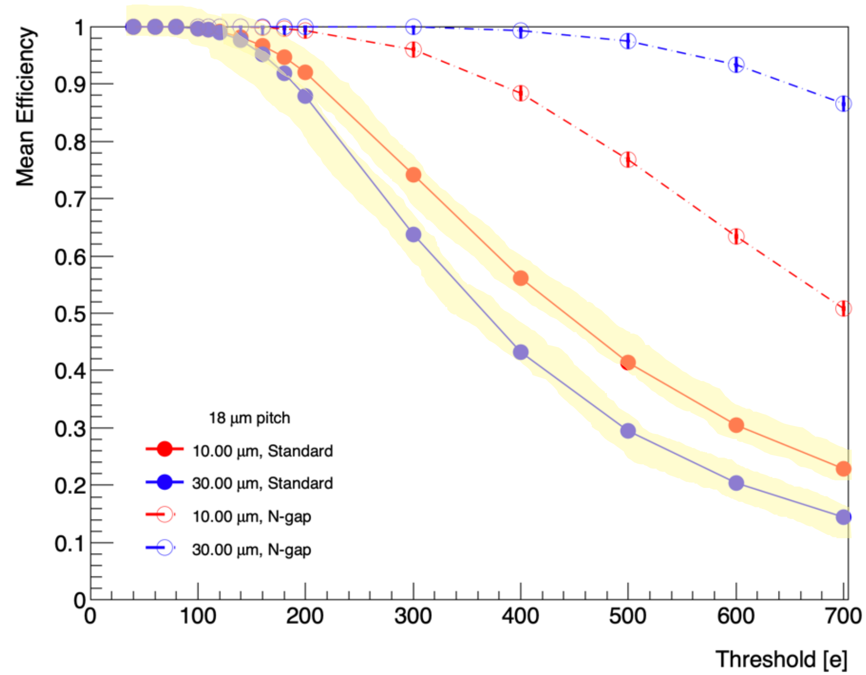
25 ns



Efficiency

⇨ In Standard, 10 μm is more efficient than the 30 μm.

25 ns



Explanation of 30 μm: It makes wide diffusion

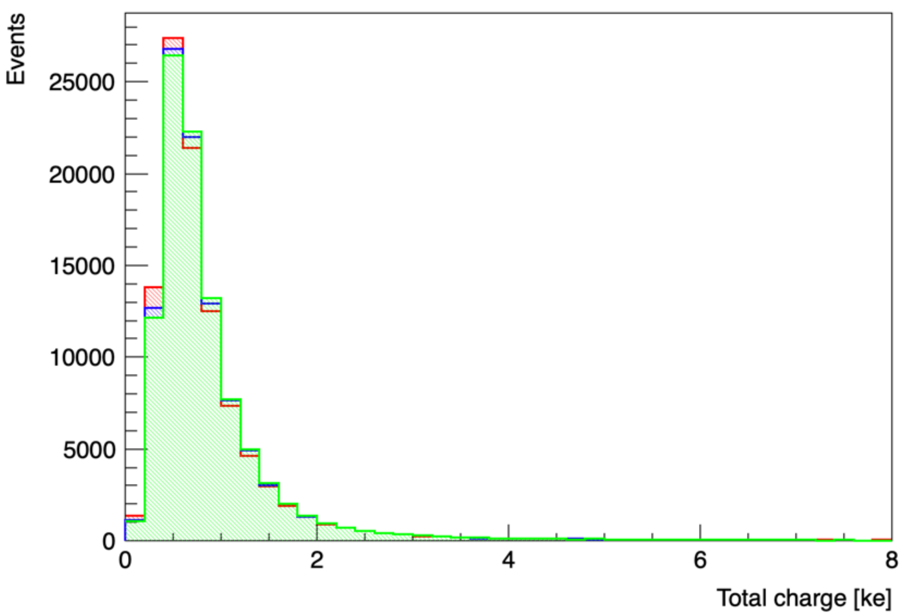
- In Standard, many charge carriers can be recombined before reaching the depletion region of the far pixel. That's why we lose efficiency rapidly as the thresholds increase.
- But in N-gap, it has larger depletion region. Thus, although they can widely move by diffusion, carriers can easily reach the depletion region in far pixels and generate signals.
- We can also explain why only the 30 μm epi-layer is influenced by the integration time.

Total Charge Per Event

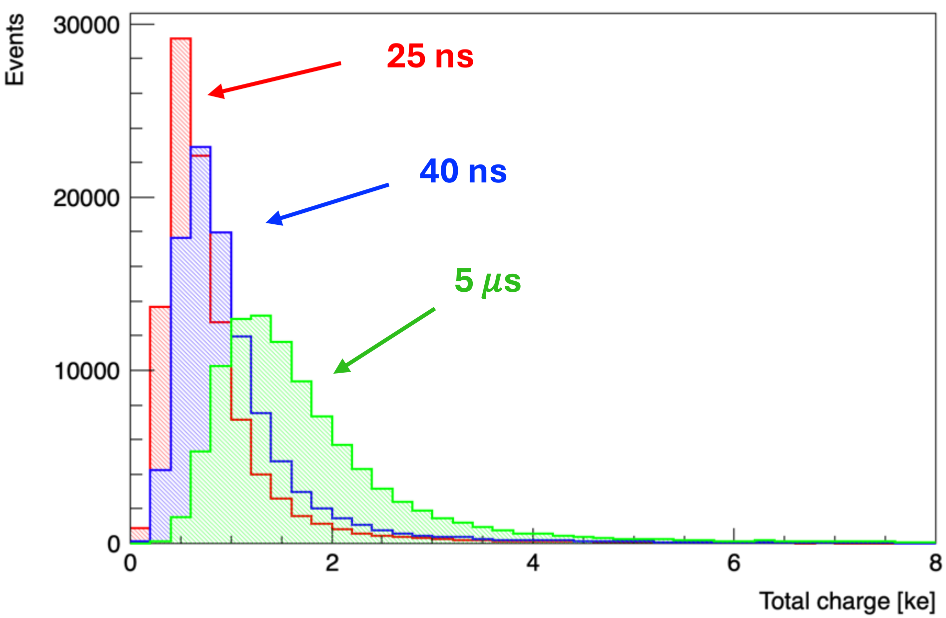
(25 ns, 40 ns, 5 μs for standard in both epi-layer)

* Fit function: Landau distribution

10 μm epi-layer



30 μm epi-layer



Most probable value

10 μm		30 μm	
25 ns	5.00e-1	25 ns	4.96e-1
40 ns	5.10e-1	40 ns	6.45e-1
5 μs	5.15e-1	5 μs	1.16

In 30 μm, charges diffuse for a long time going far pixels, and they couldn't be collected in the integration time.

This also supports our explaination!

Conclusion

1. In 10 μm epi-layer, N-gap has smaller cluster size and higher efficiency.
However, it shows worse spatial resolution compared to the Standard.
(It's because larger cluster size makes reconstruction position more precise)

2. 30 μm epi-layer shows unexpected behaviors in cluster size and efficiency.

- In 30 μm, N-gap has bigger cluster size than Standard.
- In Standard, 10 μm is more efficient than the 30 μm.

➔ To investigate, we changed integration time and checked the charge and linegraphs.
:Only in the 30 μm, cluster size and efficiency increases with the integration time.

➔ It's because 30 μm epi-layer makes carriers diffuse widely and the Standard cannot collect them due to its small depletion region.

Published References

The Tangerine project: Development of high-resolution 65 nm silicon MAPS
https://doi.org/10.1016/j.nima.2022.167025

Towards a new generation of Monolithic Active Pixel Sensors
https://doi.org/10.1016/j.nima.2022.167821

Developing a Monolithic Silicon Sensor in a 65 nm CMOS Imaging Technology for Future Lepton Collider Vertex Detectors
https://arxiv.org/abs/2303.18153

Simulations and performance studies of a MAPS in 65 nm CMOS imaging technology
https://doi.org/10.1016/j.nima.2024.16941

Simulating Monolithic Active Pixel Sensors: A Technology-Independent Approach Using Generic Doping Profiles
https://doi.org/10.48550/arXiv.2408.00027

Thank you

Backup

More Details

10 um epi-layer (slide #12, 13)

Efficiency proportionality

- ❑ N-gap: bigger pitch offers larger space for charge collection (depletion region)
- ❑ Standard: bigger pitch makes larger space out of depletion region. It worsens the efficiency.

This also can explain why the cluster sizes change easily with the pitch in N-gap compared to Standard.

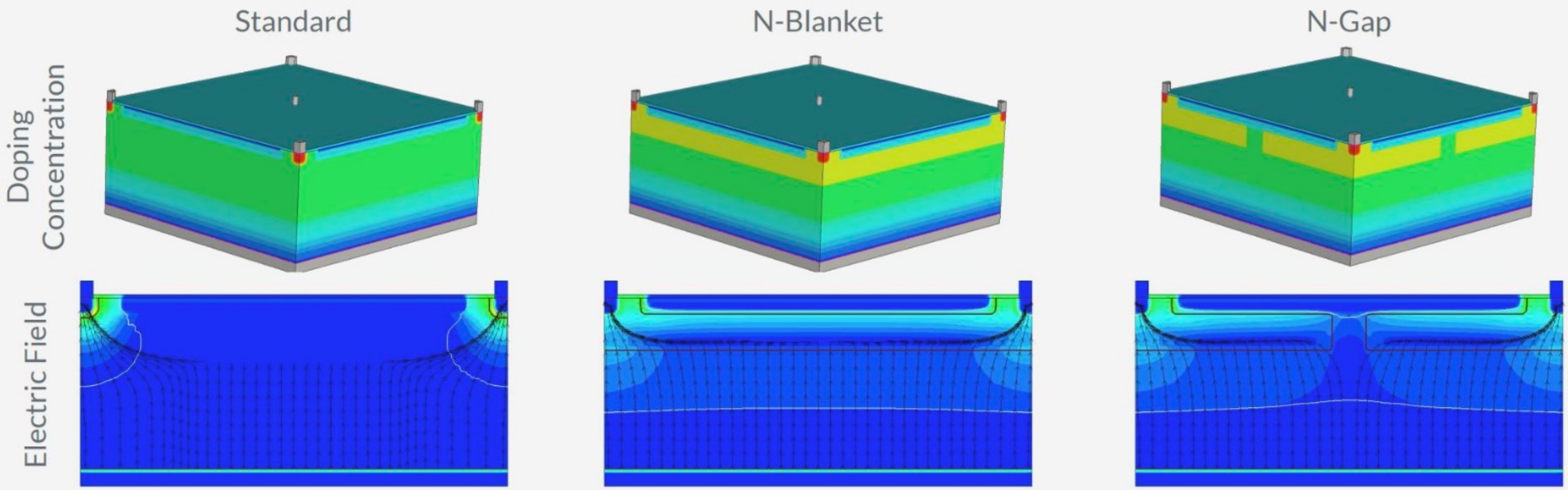
**** Comments from H. Wennlöf**
Cluster size changes with pitches

As the pitch increases, there will be smaller room for charge sharing.

When efficiency gets lower, we also lose cluster size.

Layouts

Performed using **generic doping profiles** for the 3 **Sensor layouts**:



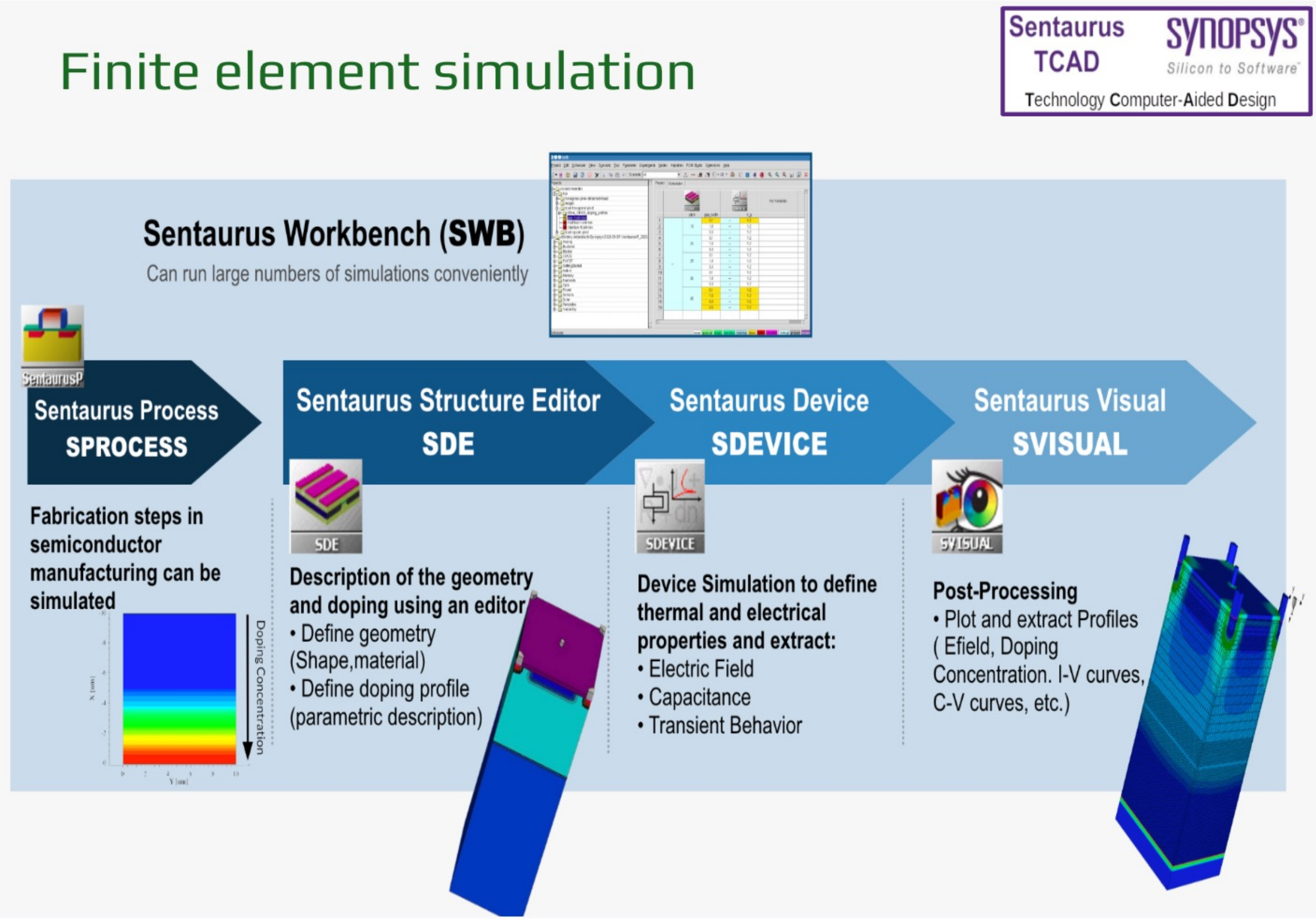
small depleted volume
⇩
- low efficiency
- high charge sharing between pixels

larger depleted volume
⇩
- improvement in efficiency
- impairment of resolution

higher electric field in pixel corners
⇩
- improvement in efficiency and charge collection
- impairment of resolution

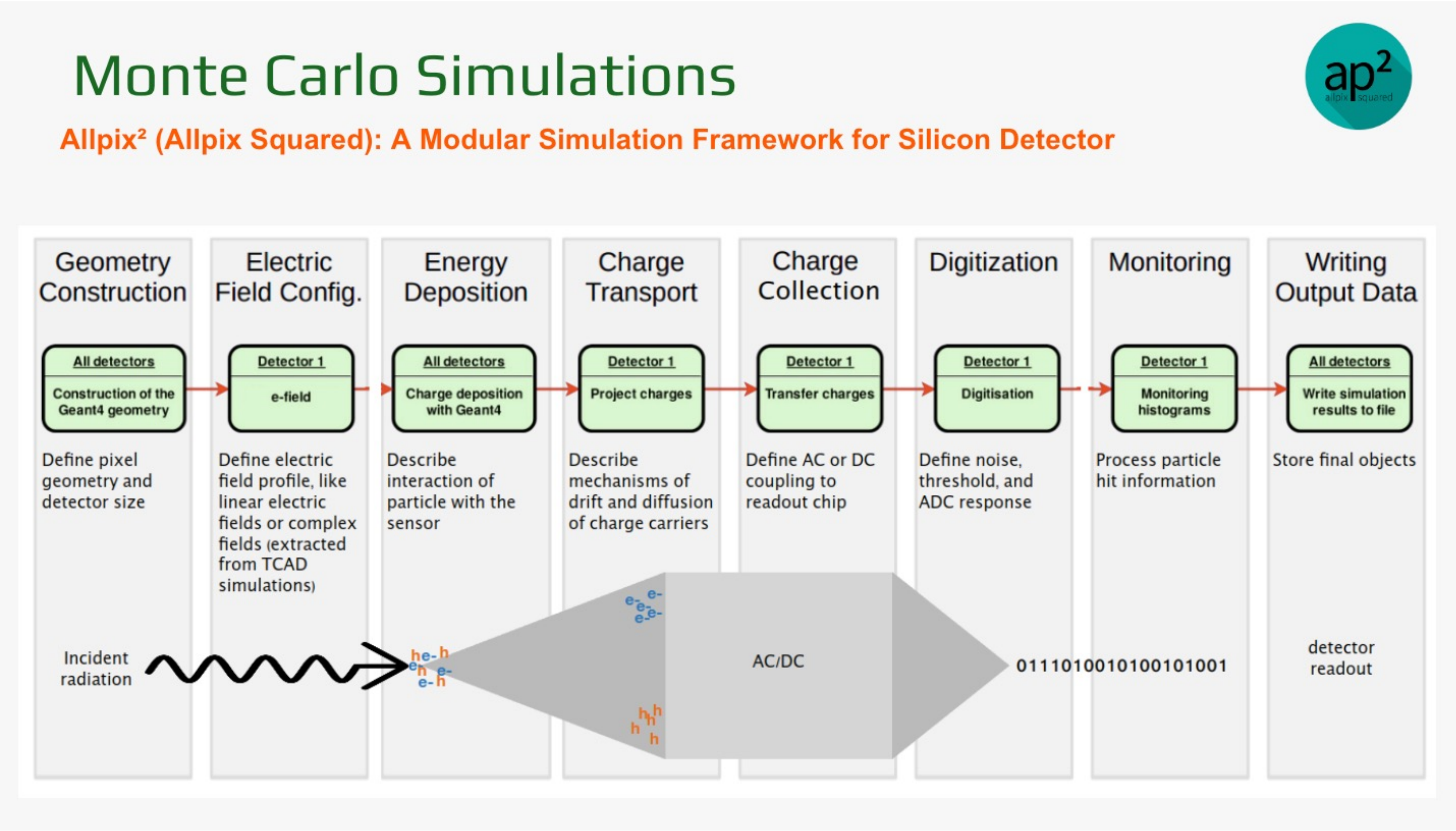
Work by A. Simancas

TCAD



L. Mendes

Allpix²



L. Mendes

Spatial Resolution

- RMS of 3σ (99.7 %) residual distribution

- Residual: difference between reconstructed cluster position and real particle position

In Allpix² simulation,

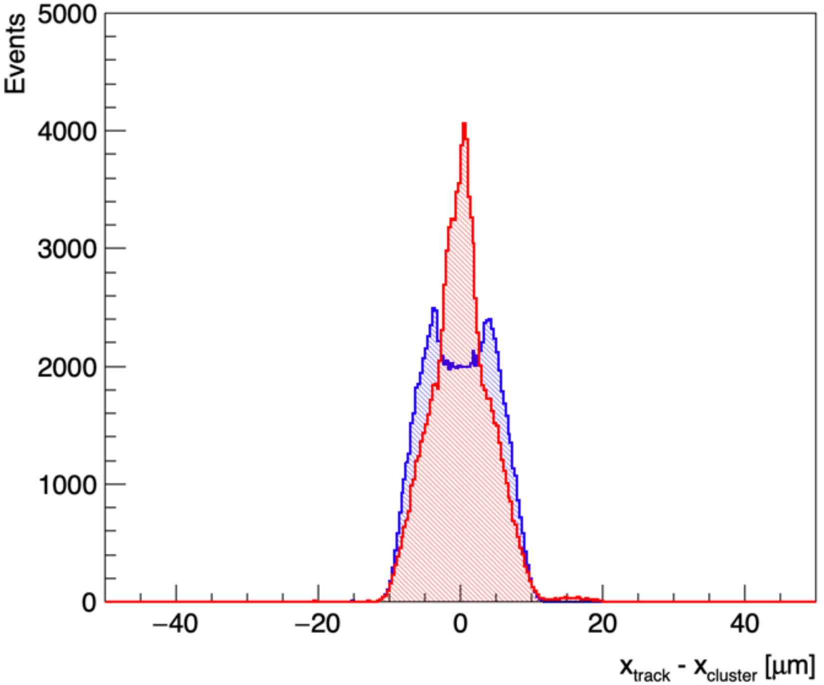
- Reconstructed cluster position: charge-weighted mean of a cluster

$$x = \frac{\sum_i x_i q_i}{\sum_i q_i}$$

- Real particle position: randomly drawn position from a Gaussian distribution

- Bigger cluster size leads to the smaller spatial resolution because it makes more precise reconstructed position

- We use an η-correction



Residual distribution
: Before (blue) and after (red) η-correction

Deep P-well

NMOS, PMOS → p-well → deep p-well structure.
(In TCAD simulation, we use it without CMOS.)
P-well is bigger than deep p-well for more space for charge collection.

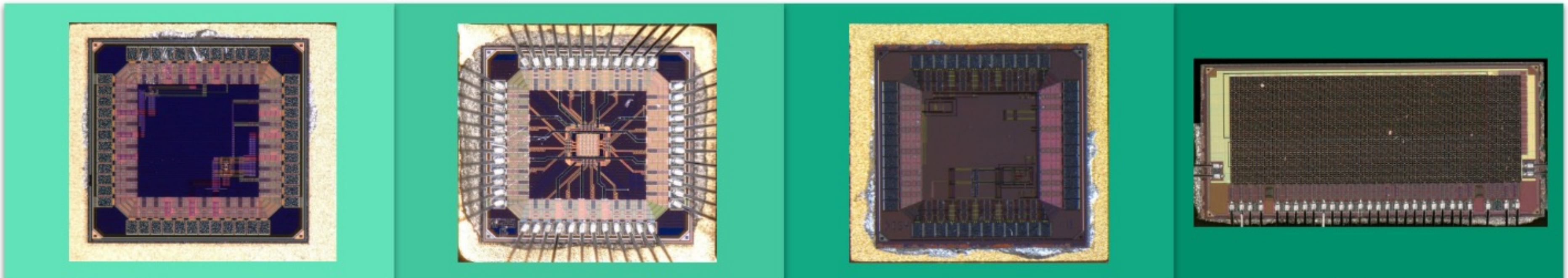
TCAD Files

*.grd: grid file. Structure of mesh.

*.dat: contain variables such as e-field potential and carrier concentrations at every mesh point in the device.

Prototype Chips

MLR1 (2021) ER1 (2023)



DESY Chip V1
OR **DESY MLR1**

APTS
W. Deng et al.

ALICE EP R&D

DESY Chip V2
OR **DESY ER1**

H2M

CERN IFAE

DESY MLR1: fully characterized

- Entirely developed at DESY
- Test structures for **CSA characterisation** developed at DESY
- Block of 2x2 16 µm pixels with an analogue readout for **pixel characterisation**

Analogue Pixel Test Structures (APTS): fully characterized

- Designed at CERN (DESY involved in the lab and TB characterisation)
- **4x4 pixels structure** with analogue output
- Different sensor **pitches and layouts**

DESY Chip V2 in preparation

- 2x2 pixel (35x25 μm^2) with **all-in-pixel functionality**
- External access to **CSA** and **discriminator** output
- N-gap layout with **2.5 µm** and **4 µm** gap
- Single **Front-End** with charge Injection

H2M (Hybrid-To-Monolithic) on going characterization

- Collaboration of DESY, CERN and IFAE
- **3 x 1.5 mm^2** , 64 x 16 square pixel, 35 µm pitch
- **8-bit** counter per pixel
- **4 acquisition modes** (ToA, ToT, counting, binary RO)

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Depletion Region

With the reverse bias voltage (ref. G. Lutz, Semiconductor Radiation Detectors)

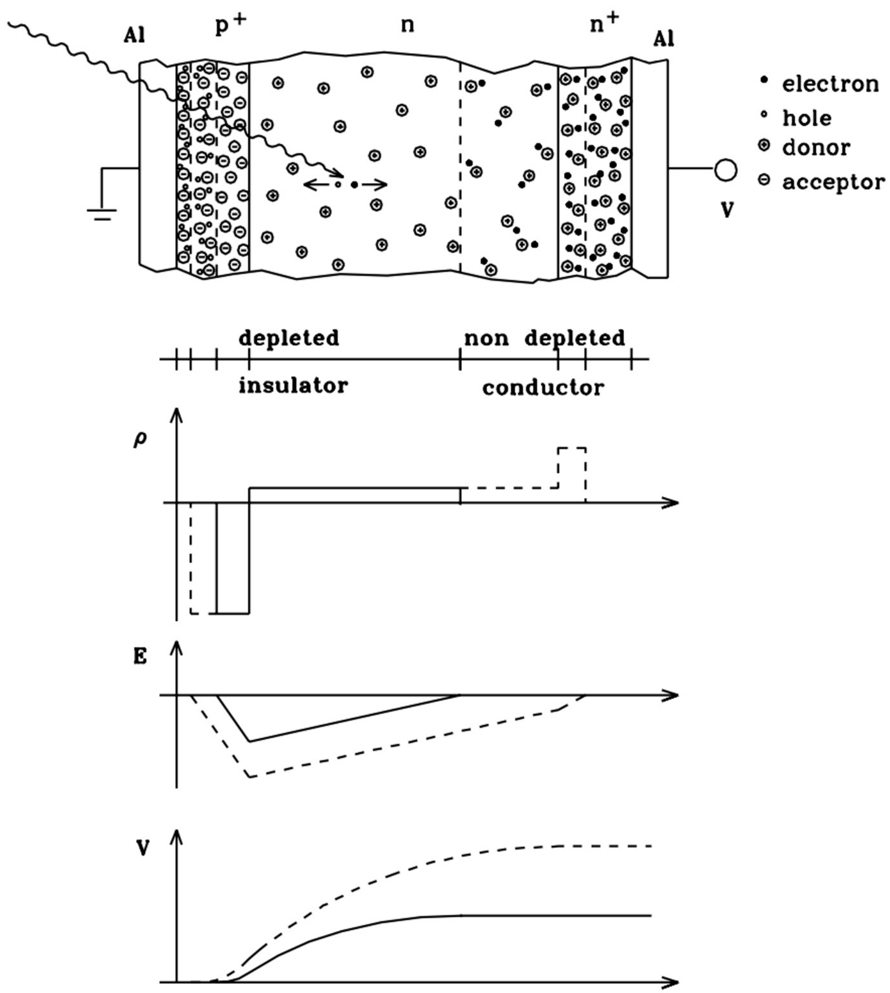

Fig. 5.2. A p–n diode junction detector: charge density, electric field and potential for partial (*continuous line*) and full (*dashed line*) depletion