Silicon Calibration

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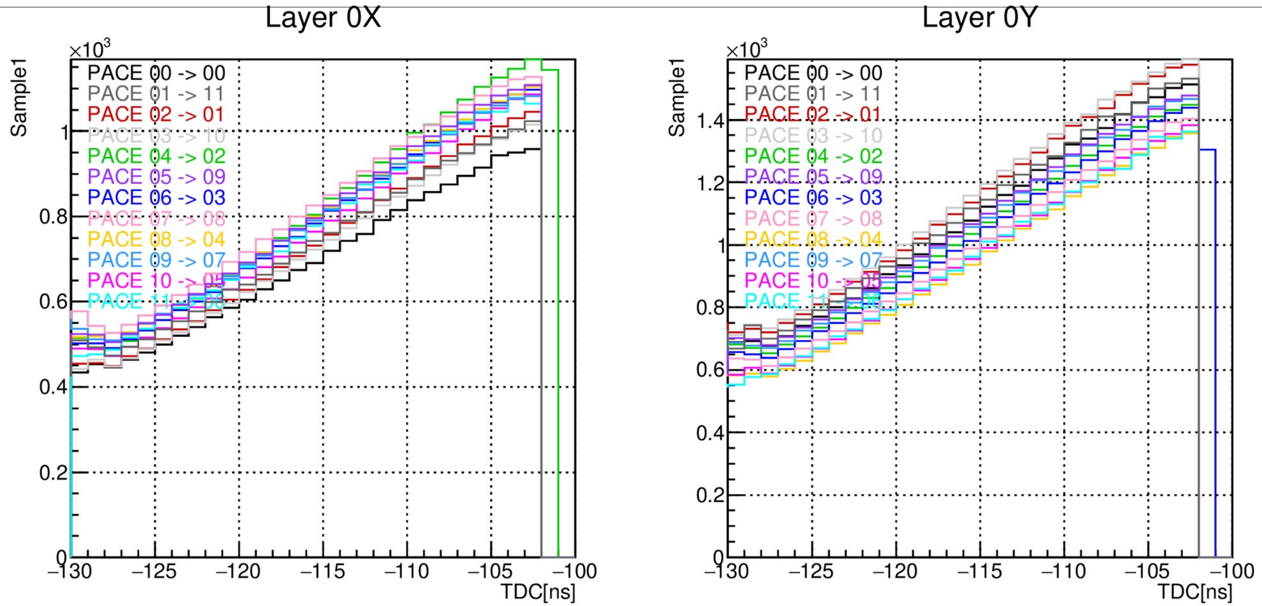
TDC-Signal correction

Signal dependence(s)

Using 200 GeV electron

<u>Selecting only the **strip** *hit* by the track on the **maximum** layer</u>
(so that we can expect always the same signal everywhere)
we can see a signal dependence on two factors:

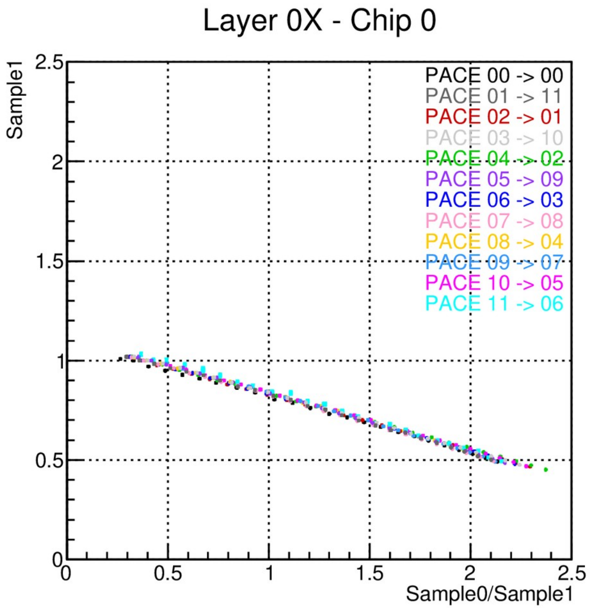
- TDC time (i.e. latency fluctuations) as expected
- Chip/Channel as shown by Elena's study

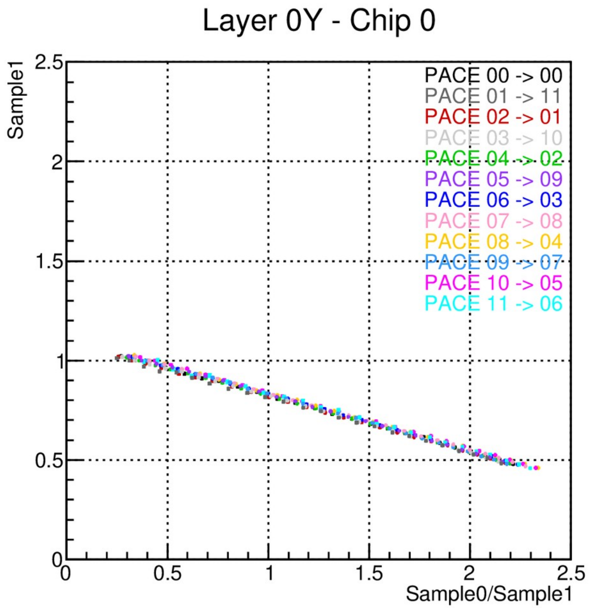


Sample1 vs Sample0/Sample1

Using 200 GeV electron

Latency dependence is clearly evident if we report the signal as a function of Sample0/Sample1 which depends directly on latency (here we normalized considering Sample1=1 for TDC=-104.5 ns)

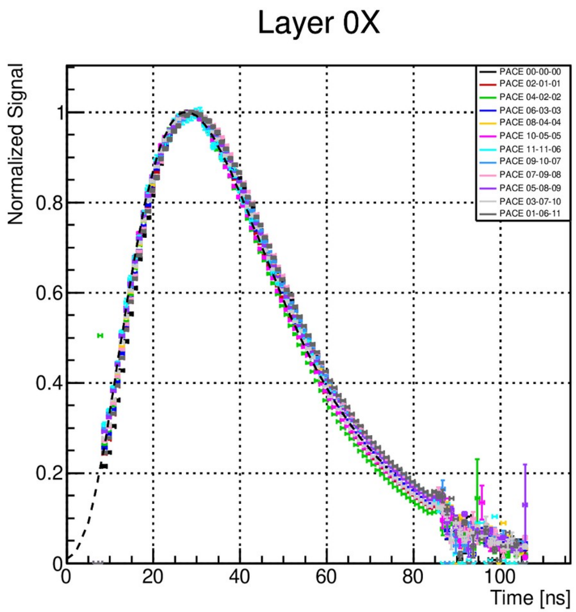


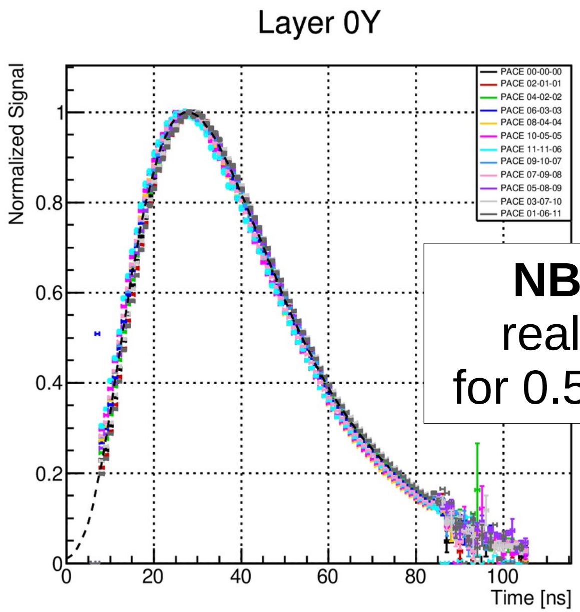


Time profile

Using 200 GeV electron

Using Sample 0, 1 and 2 it is possible to reconstruct the time profile of the signal which, despite chip/channel dependence, is in good agreement with the laboratory measurements by Elena





NB Time scales are realigned using Time for 0.5 Normalized Signal

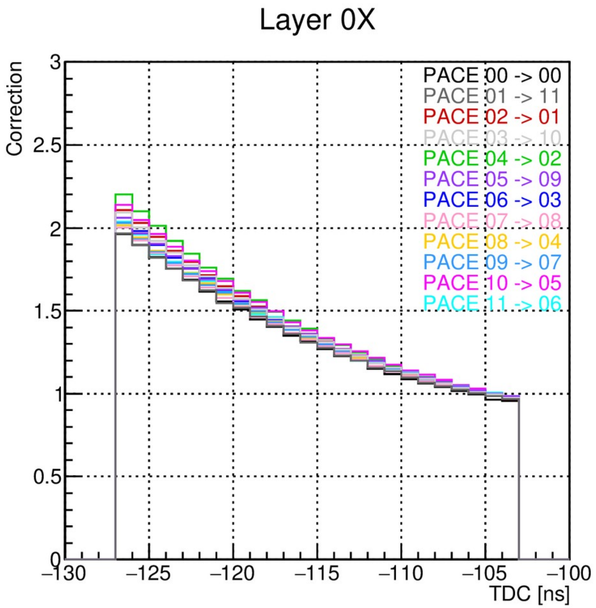
Implementing correction
Method A

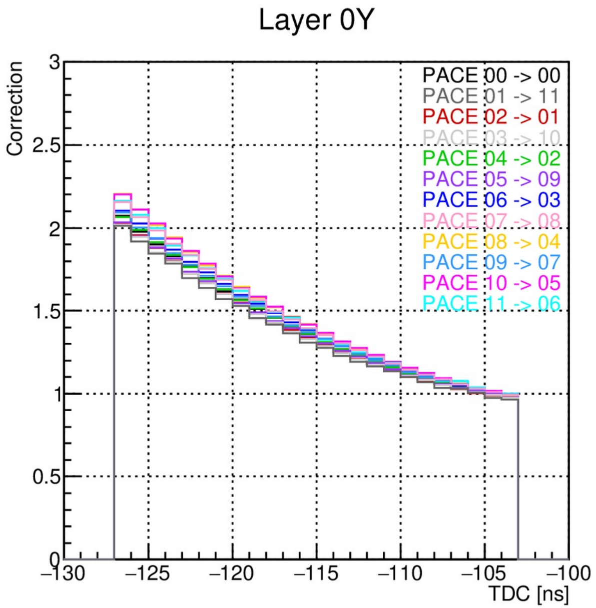
Using 200 GeV electron

Considering as reference TDC Time=-104.5 ns and S0/S1 from CHIP 9 at that TDC Time, for each layer we computed a correction (for both effects):

C = S(chip, S0/S1, TDC) / S(chip, S0/S1, TDC)

i.e. after rescaling to TDC time, we use S1 vs S0/S1 to correct for the fact that at this time the chip has S0/S1 different from S0/S1 of CHIP 9



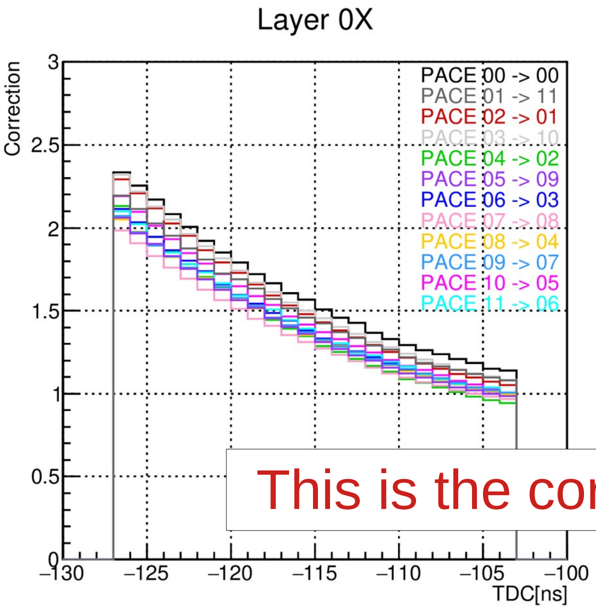


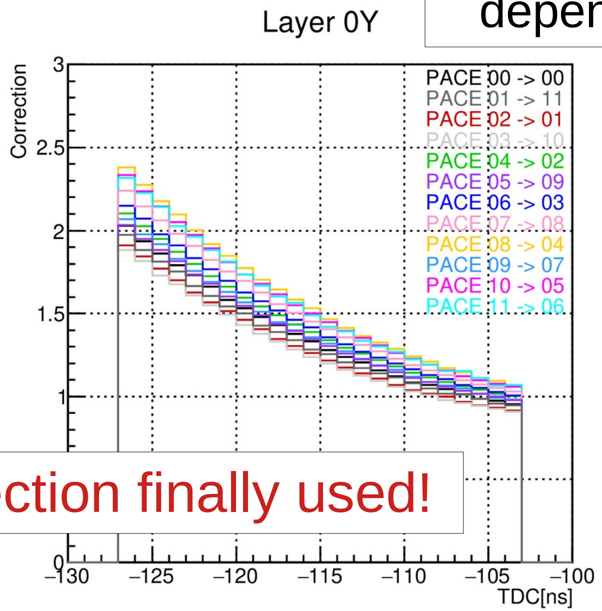
Implementing correction
Method B

Using 200 GeV electron

Considering as reference CHIP 9 and TDC Time=-104.5 ns,
for each layer we computed a correction (for both effects):
C = S(CHIP, TDC) / S(chip, TDC)

NB This method implicitly assumes no position dependence of release



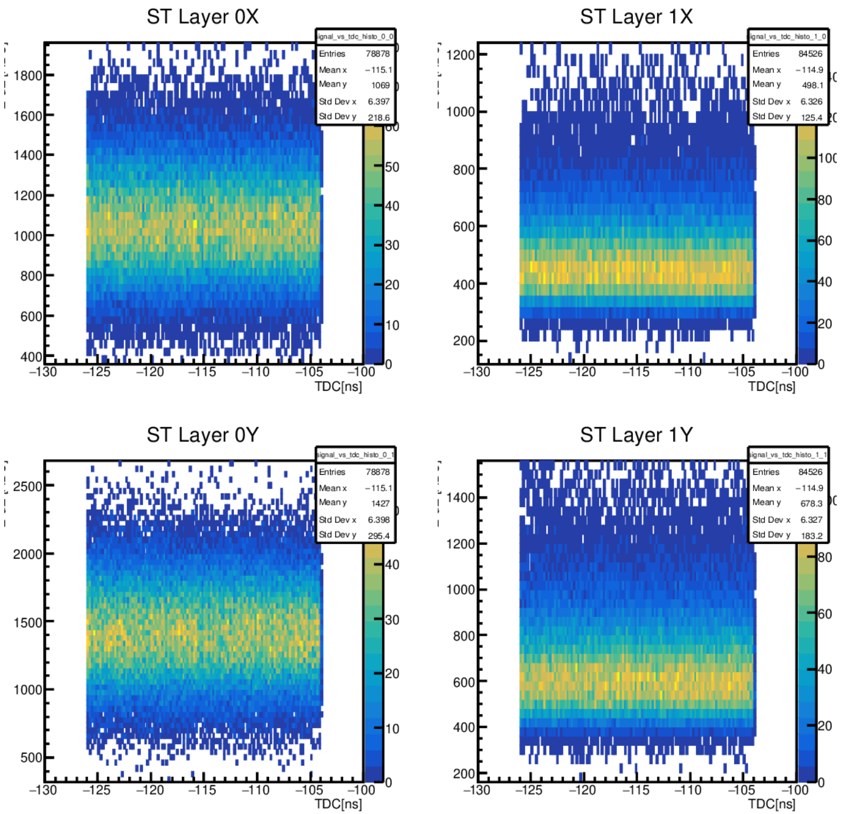


This is the correction finally used!

Gain Calibration

Signal dependence after correction

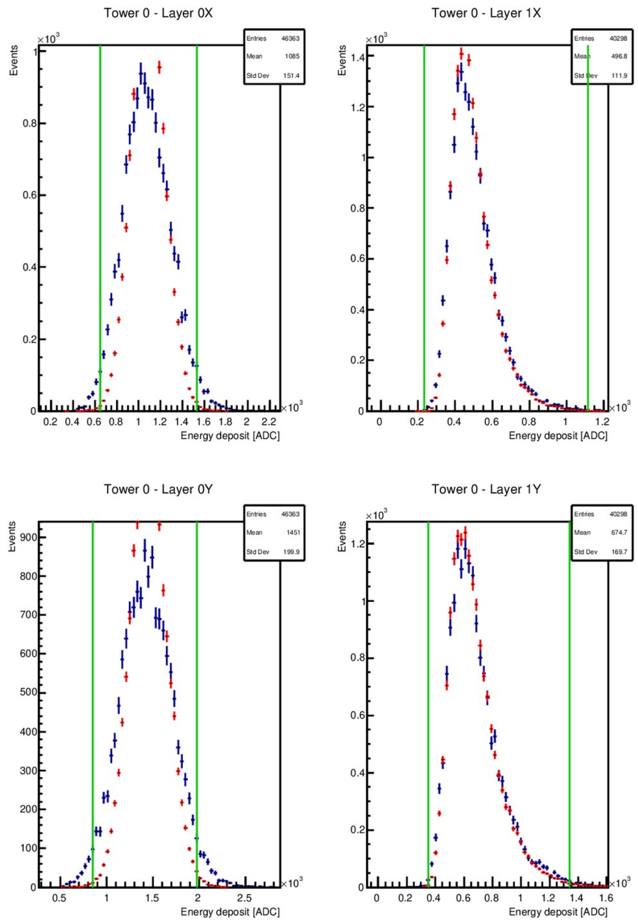
Using 200 GeV electron



Correction (at least for TDC) seems to work well

Problem with minimization

Using 200 GeV electron



Even after correction, and considering just the strip *hit* on the maximum layer, DATA are considerably larger than MC on Layer 0 and slightly larger than it also on Layer 1

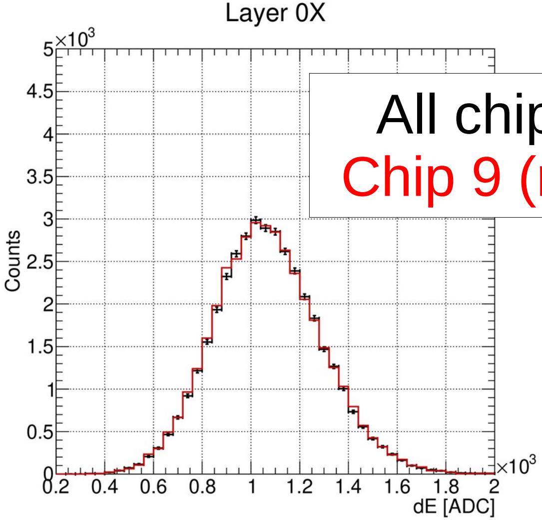
Possible reasons for this discrepancy:

- Residual chip dependence
- Effect of chip edge channels
- Different position resolution

All investigations exclude these effects

Solving the problem...

Using 200 GeV electron



No residual chip dependence!

Since there is no clear explanation, I barbarously solved the problem by adding an additional gaussian smearing to MC

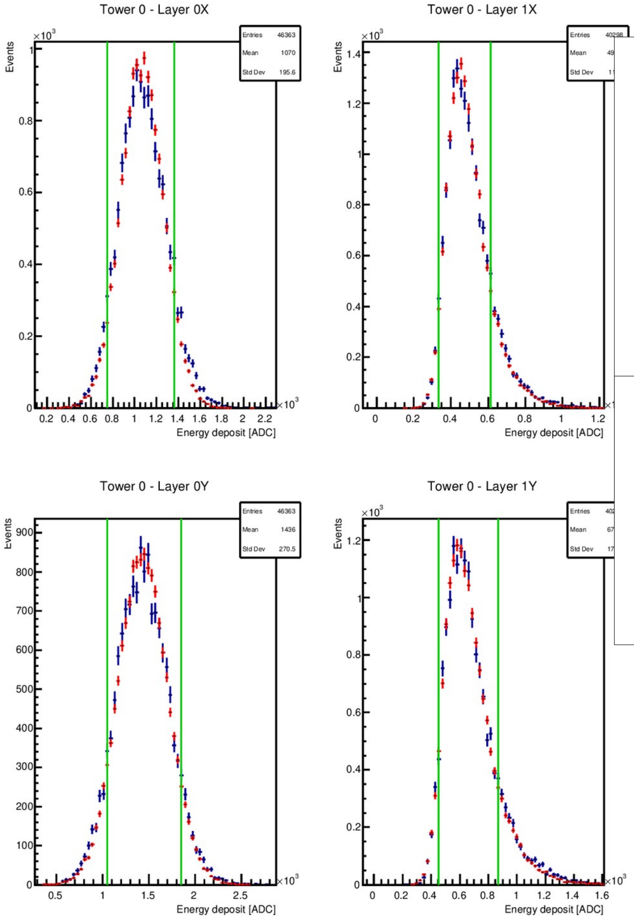
This gaussian width is taken from the quadrature difference of resolution in DATA and MC (before calibration) multiplied by an arbitrary factor (e.g. 0.85 for Layer 0, 0.50 for Layer 1)

...the good point is that the final gain factor is not significantly affected by applying or not applying this artificial smearing

Calibration Selection

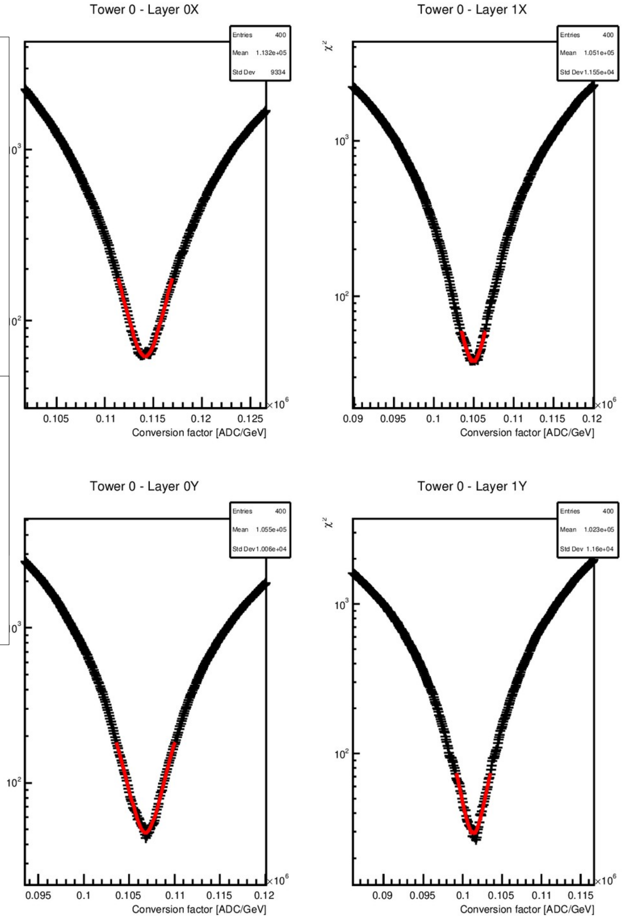
Method I - Front

SPS-Front - 200 GeV electron



In Method I, we select the strip to be considered for calibration by looking, event-by-event, only to the strip hit by the track on the <u>maximum layer</u> for the view

This method is more precise since it ensures a large signal and is not affected by the silicon layer misalignment

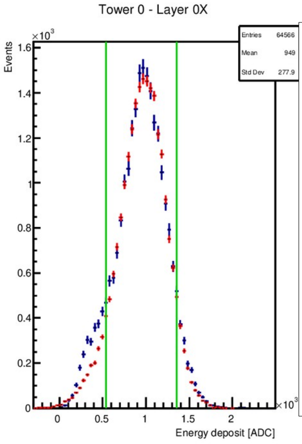


Calibration Selection

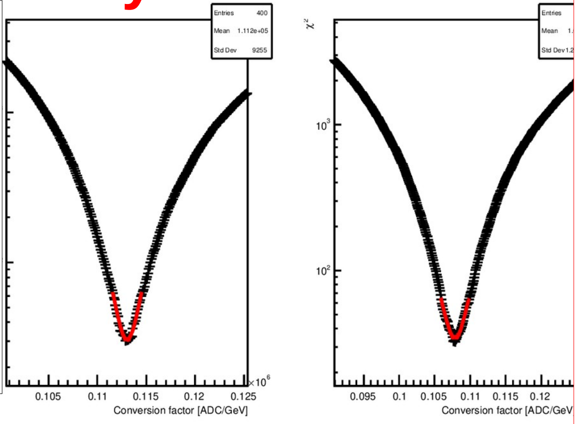
Method II - Front

SPS-Front - 200 GeV electron

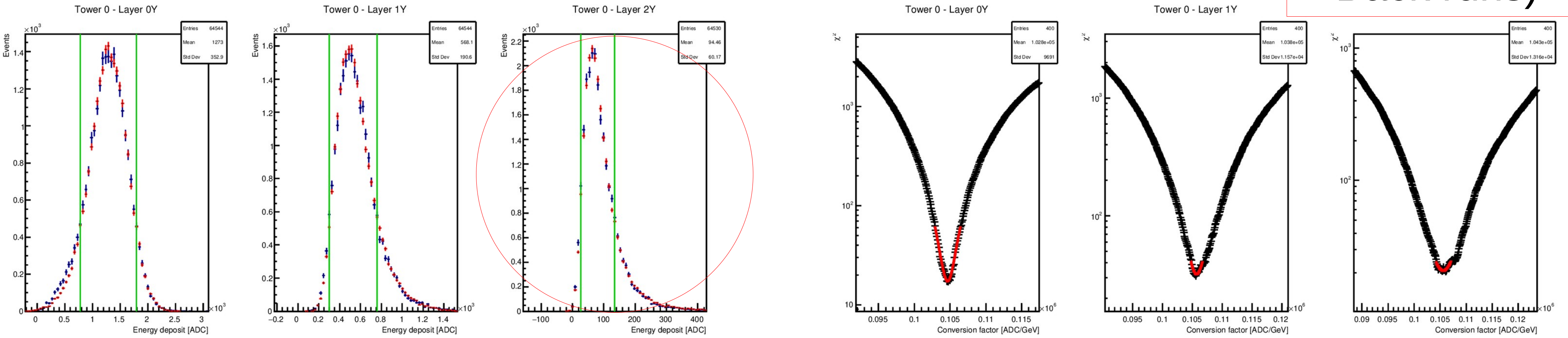
for Layer 2Y only!



In Method II, we select the strip to be considered for calibration by looking, event-by-event and <u>for each layer</u>, to the strip with maximum deposit within ±5 strips from the one hit by track



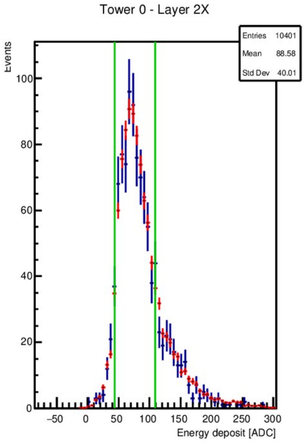
Less precise but necessary for layer 2Y which is never the maximum layer (neither in Front or Back runs)

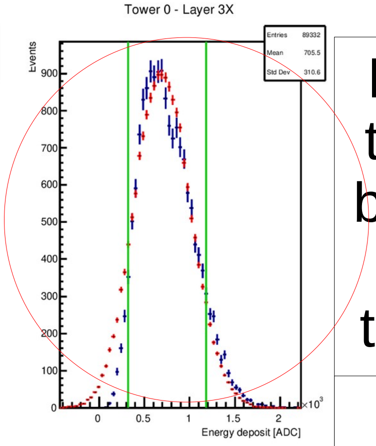


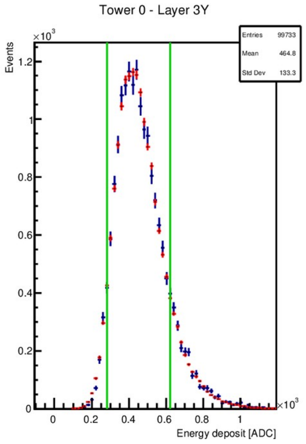
Calibration Selection

Method I - Back

SPS-Back - 200 GeV electron



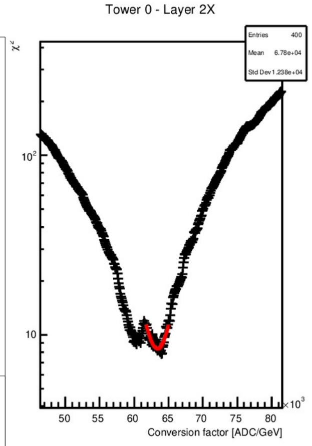


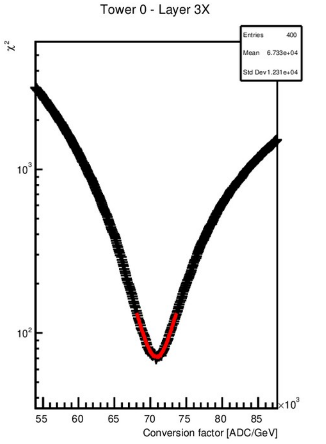


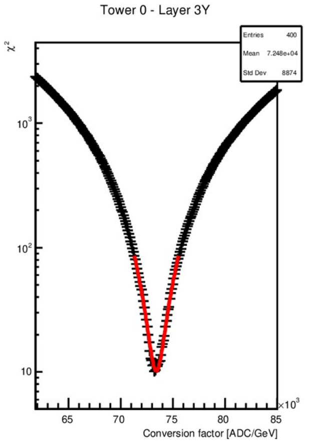
In Method I, we select the strip to be considered for calibration by looking, event-by-event, only to the strip hit by the track on the <u>maximum layer</u> for the view

This method is more precise since it ensures a large signal and is not affected by the silicon layer misalignment

I cannot get good agreement on layer 3X with any method or smearing factors I have tried

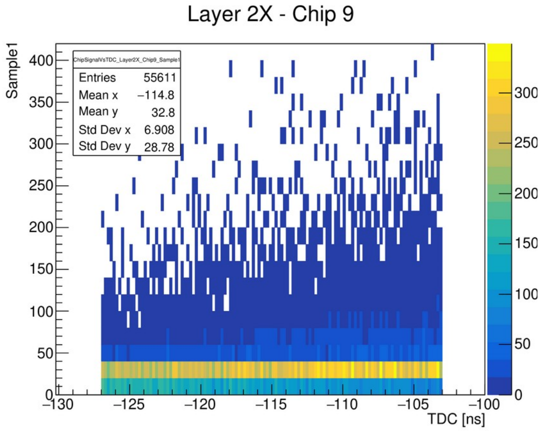


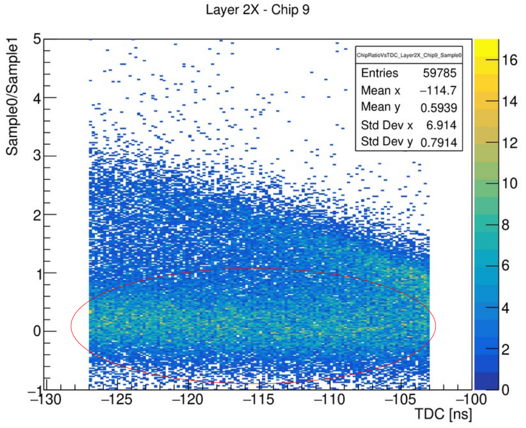




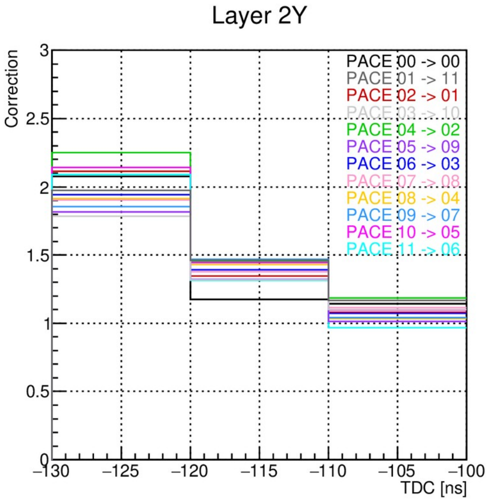
Problematic layers

Layer **2Y** (Front) and **2X** (Back) have both <u>small signal</u> and <u>limited statistics</u>

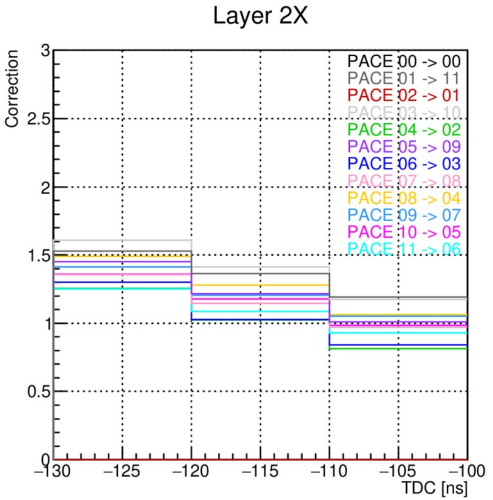




SPS-Front



SPS-Back

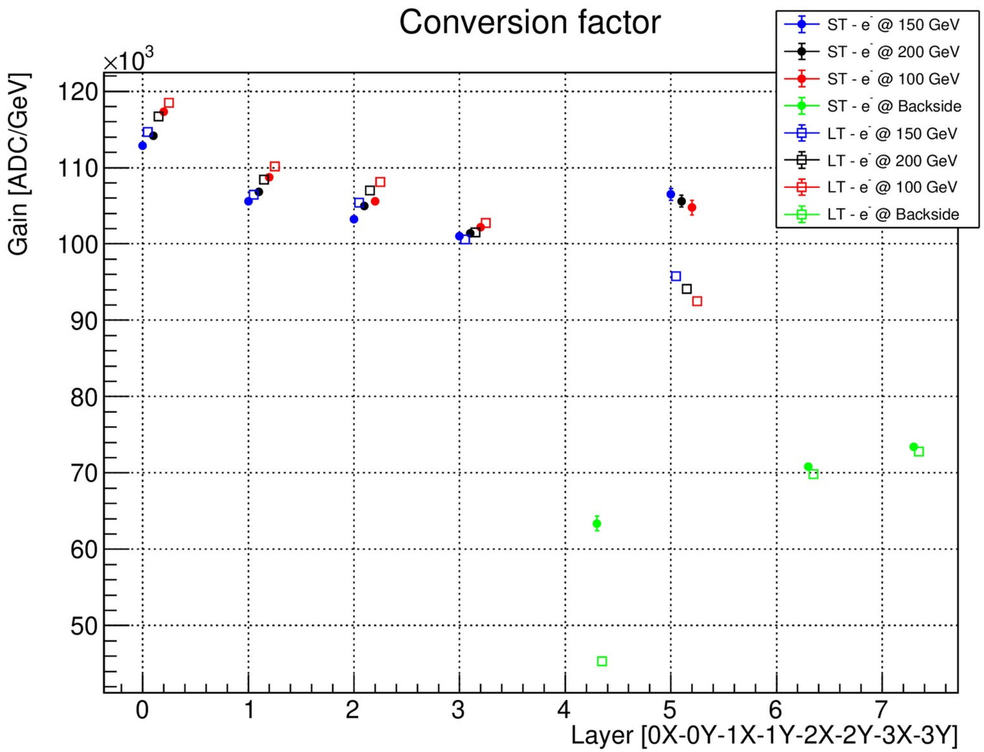


Layer **2X** has also a strange band in the trend of S0/S1 against TDC, therefore we will use curve from 3X for gain rescaling (see later)

TDC-Signal correction was estimated with large bins and spline interpolation

SPS results

Gain factors

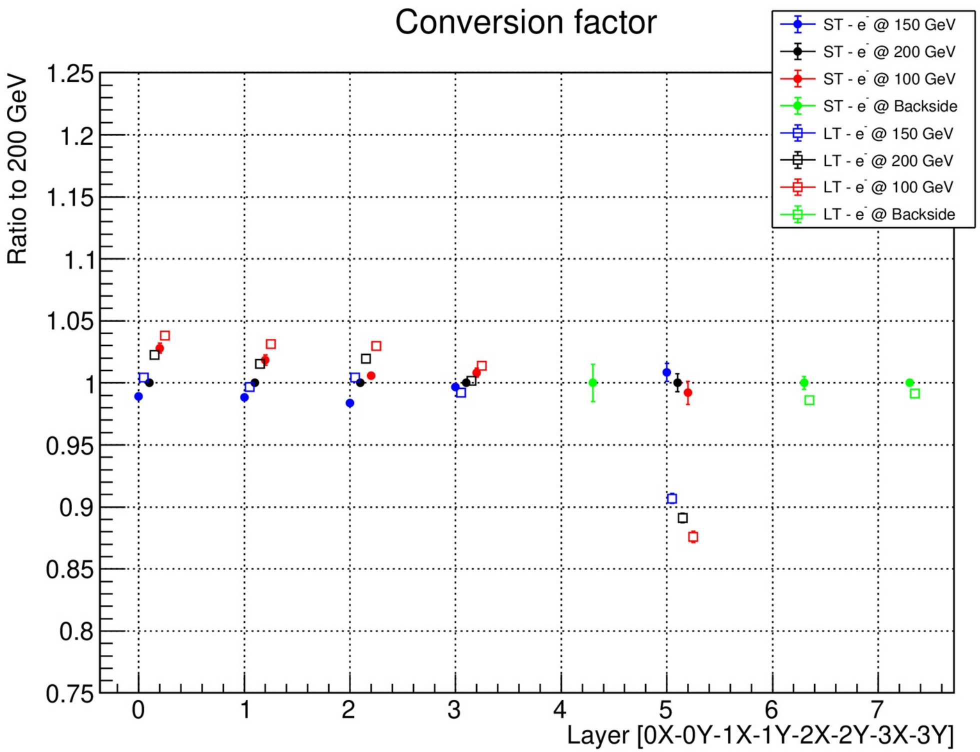


Front and Back calibration were done in very different latency configuration (S0/S1~0.4 and 1.1, respectively) hence the different gain of the layers

Problematic layers 2X and 2Y suffers of large TS-TL strip gain deviation

The clear energy trend in the first five layers may indicate non linearities due to charge capacitive coupling between strips or chip channels?

Gain ratio

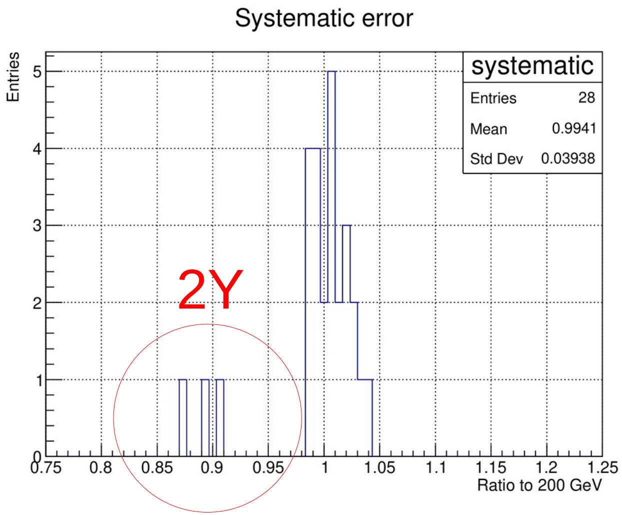


When considering the uncertainties, for all layers we can look at the TS-TL strip gain deviation and, for the first five layers, to the energy dependence

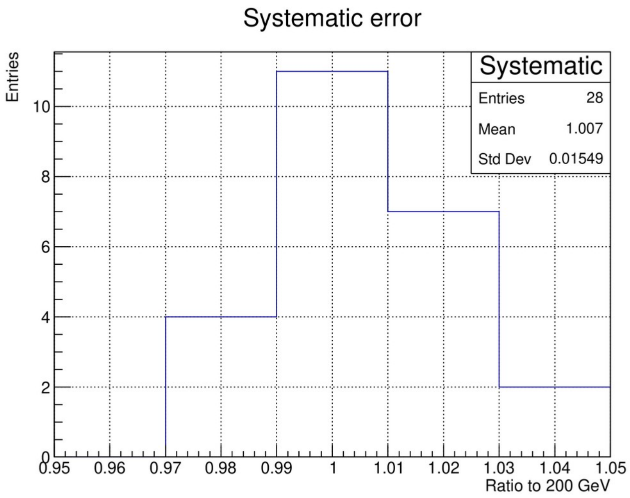
I would not consider layer 2X for the uncertainty since it should also not impact so much on energy deposit in developed electromagnetic shower.

Systematic uncertainties

Ignoring uncertainty on 2X



Ignoring uncertainty on 2X and 2Y



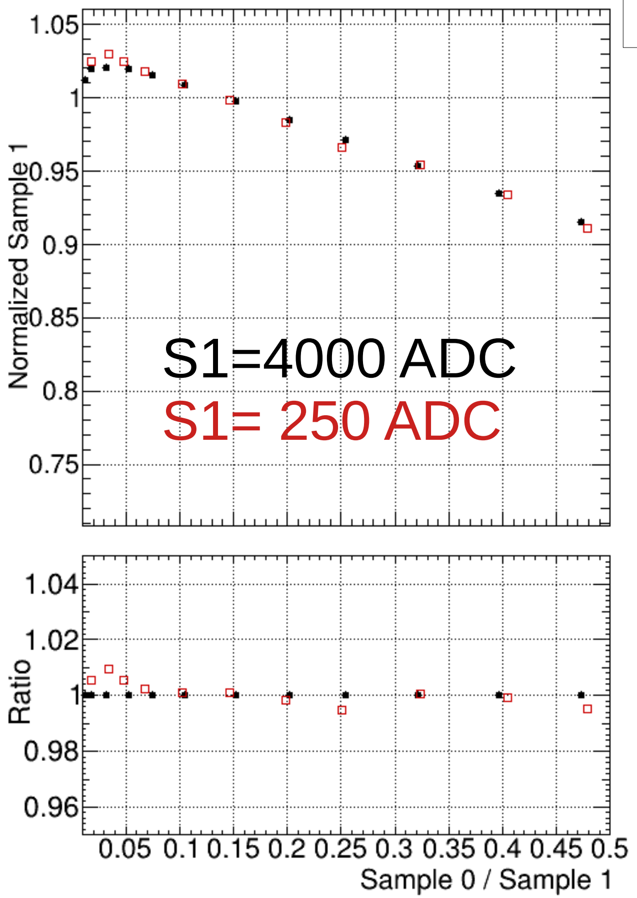
Depending on which layers we consider or not, the final calibration uncertainty changes between 1.5 and 3.9%

It is difficult to assess a number because there are several poorly understood effects in the silicon data.

Gain Scaling

Gain rescaling function

From Elena's work



External calibration

Since $S1_{norm}$ = f(S0/S1), knowing $S0/S1_{SPS}$ and $S0/S1_{LHC}$, we can rescale gains as:
$G \rightarrow G * f(S0/S1_{LHC}) / f(S0/S1_{SPS})$

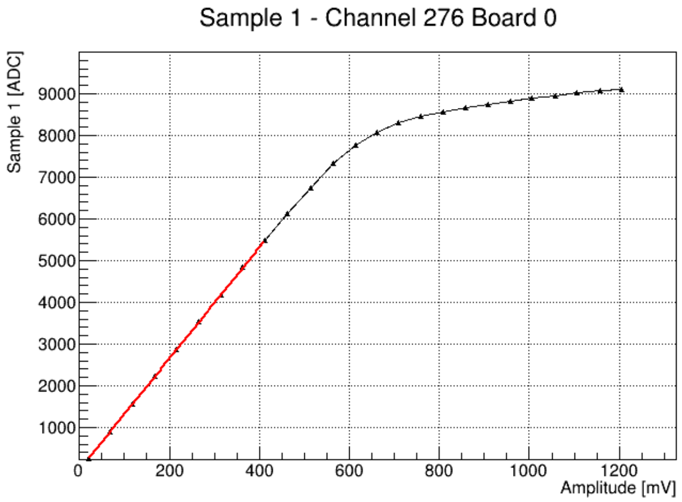
These functions have been measured by Elena at two reference amplitudes for SPS (250 ADC) and LHC (4000 ADC)

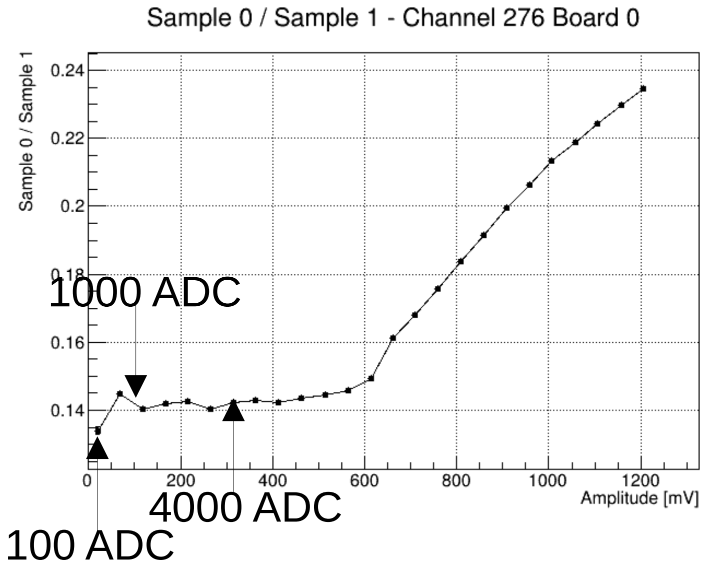
The deviation between the two functions is below 1% in the S0/S1 range considered: does it has a negligible impact on the gain?

Dependence of S0/S1 from signal amplitude

From Elena’s work

External calibration



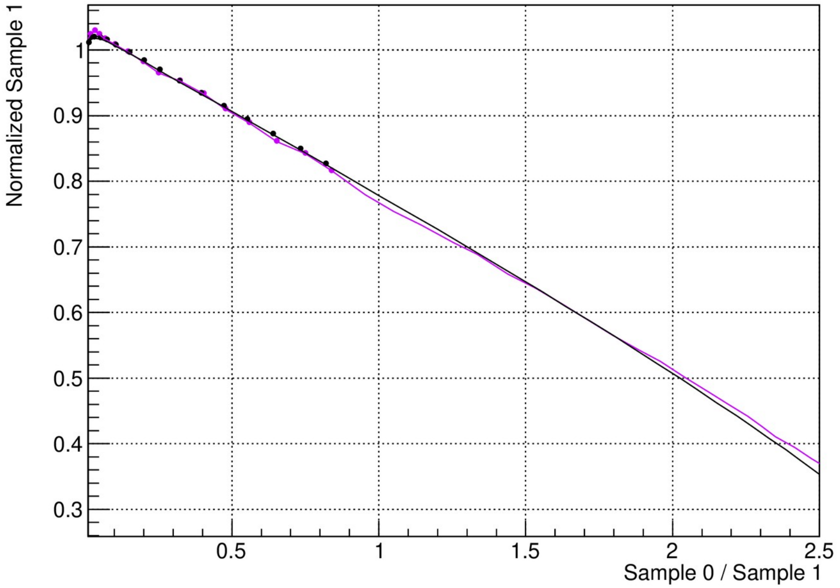


Fixing S0/S1=0.14, it changes of less than 0.005 between SPS energies (100-1000 ADC) and the LHC reference energy (4000 ADC)

Gain rescaling function

From Elena's work

External calibration



We will use violet/black function for SPS/LHC signal rescaling

Let's consider the following case:

- $\langle S0/S1 \rangle_{LHC} = 0.14$ for S1=4000ADC
- $\langle S0/S1 \rangle_{SPS} = 0.40$ for S1=100-1000ADC

If S0/S1 depends on amplitude by 3.5%, $\langle S0/S1 \rangle_{SPS}$ can change in [0.386, 0.414]

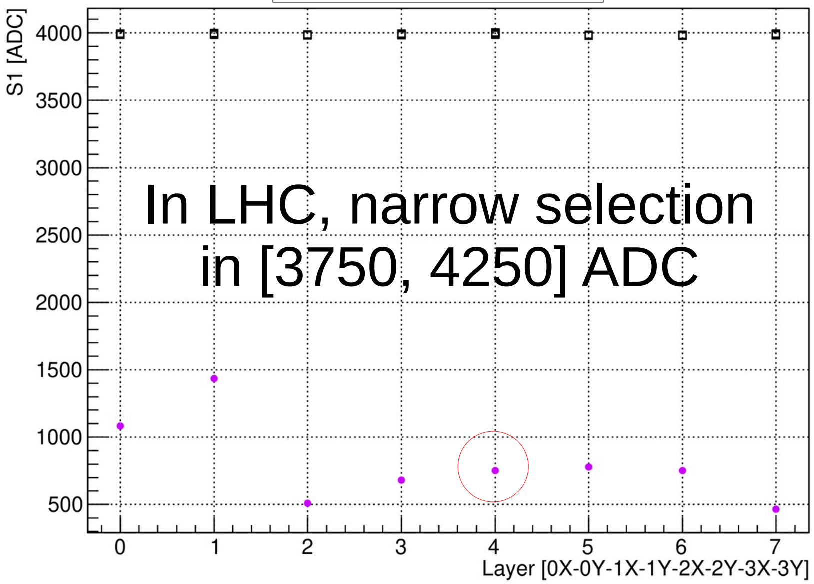
f(0.386)/f(0.14)=0.935	f(0.386)/f(0.14)=0.938
f(0.414)/f(0.14)=0.928	f(0.414)/f(0.14)=0.930

The difference between the two functions and the S0/S1 dependence on amplitude is significant for back (1%), not for front (0.5%)

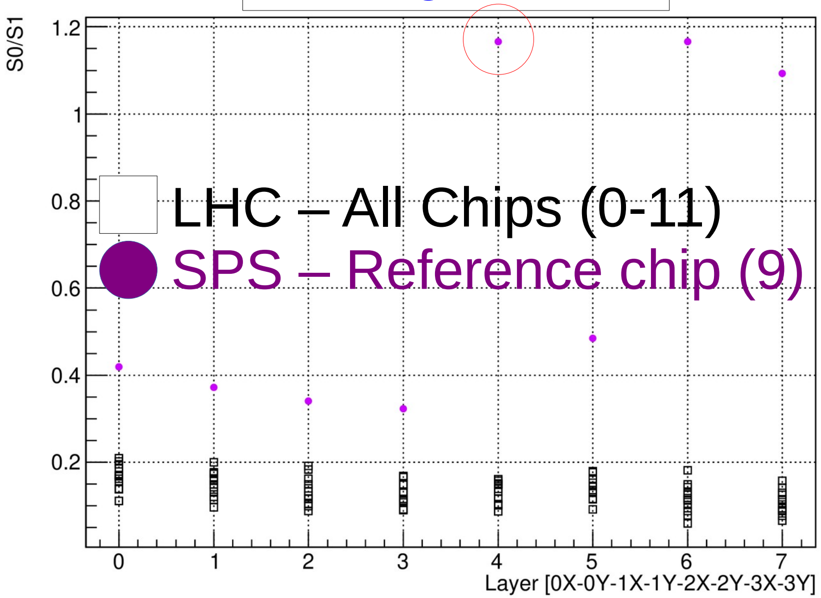
Final table

Reference values

Average S1



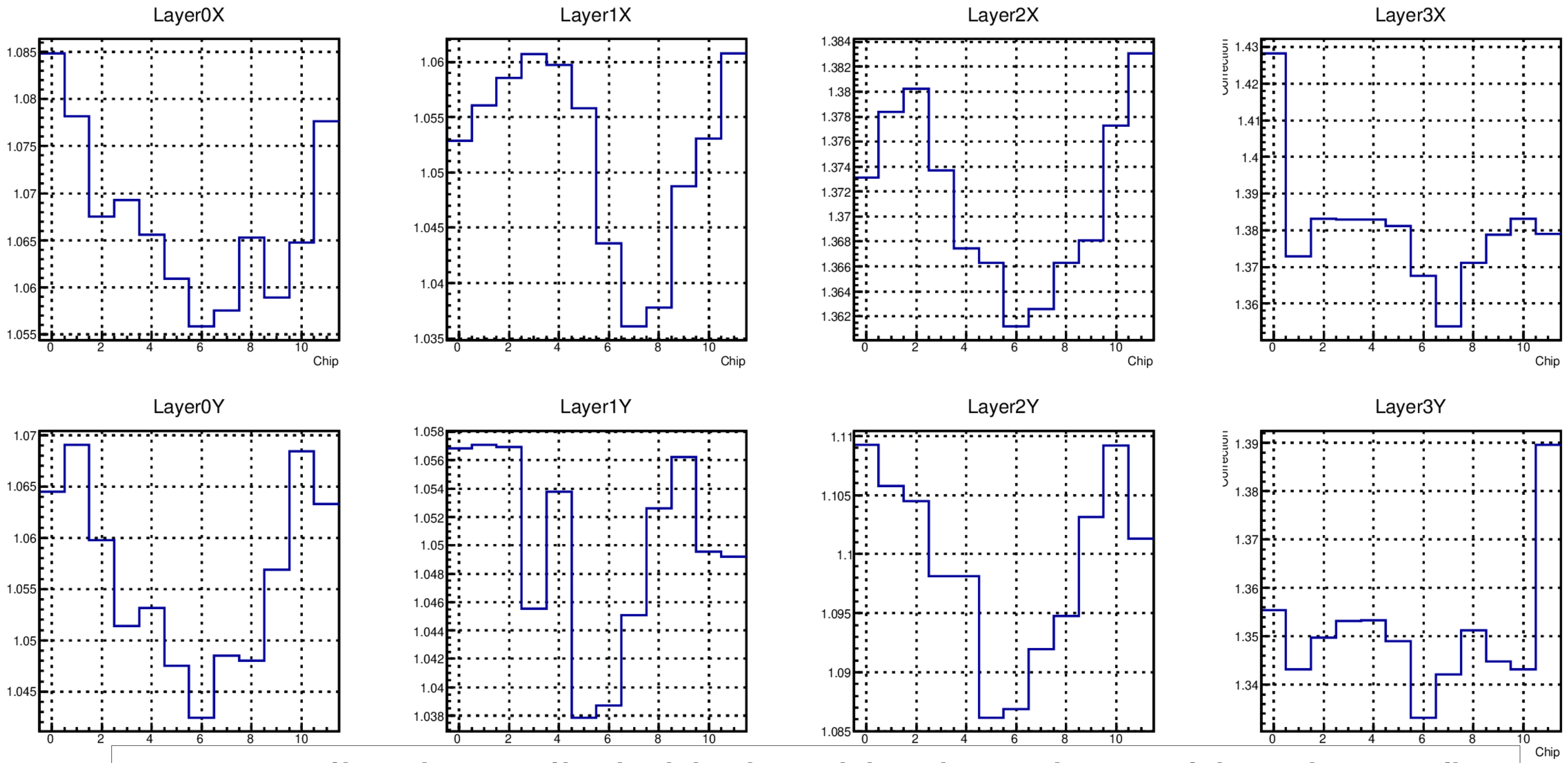
Average S0/S1



For SPS, Layer **2X** values are artificially taken from 3X values

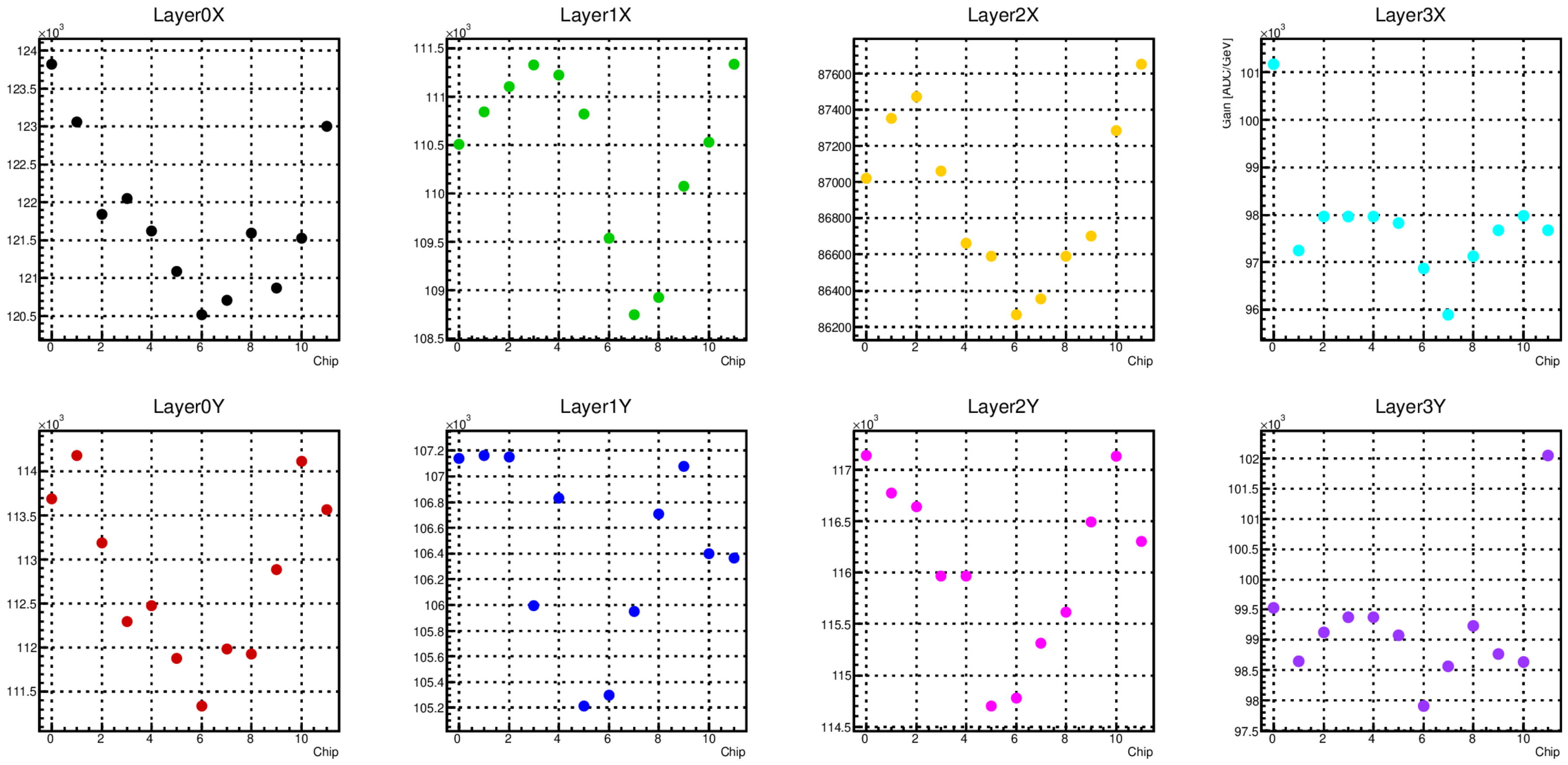
These are the S0/S1 values necessary to define rescaling factors using S1 vs S0/S1

Rescaling coefficients



NB: Scaling is applied chip-by-chip (not channel-by-channel)

Final gains for LHC2022 (Fill 8178 Subfill 1)

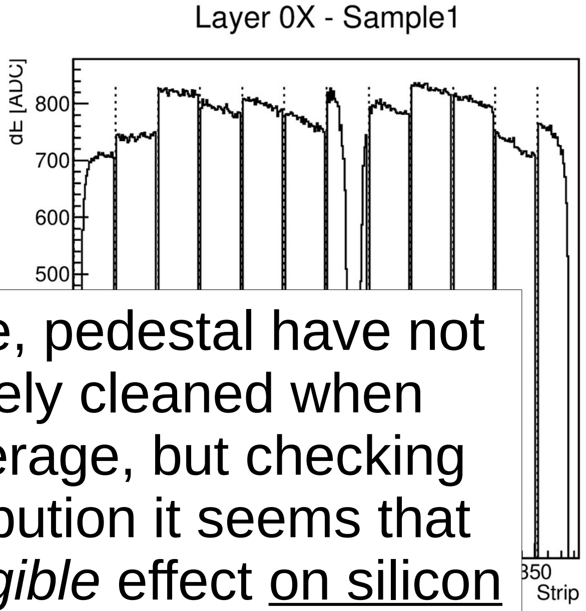


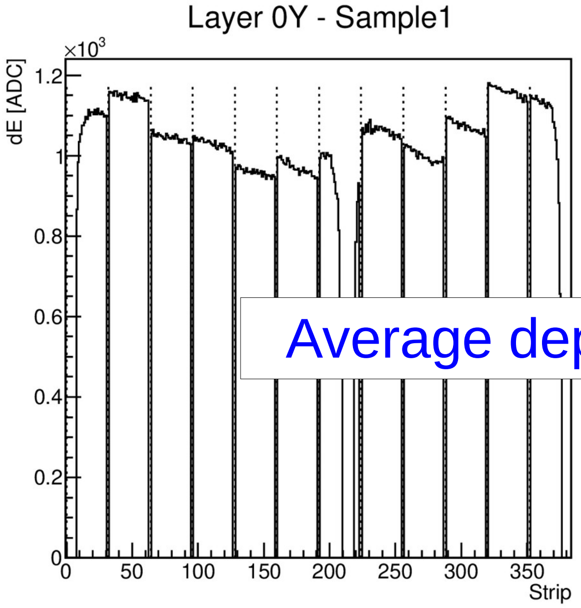
Residual chip dependence

Correction comparison

Using 200 GeV electron

Method A implicitly assumes the same gain for all chips/channels, which should be true at the present status of our knowledge, but it is clearly not the case since it is not compatible with Method B: **that why we decide to always correct using Method B only**



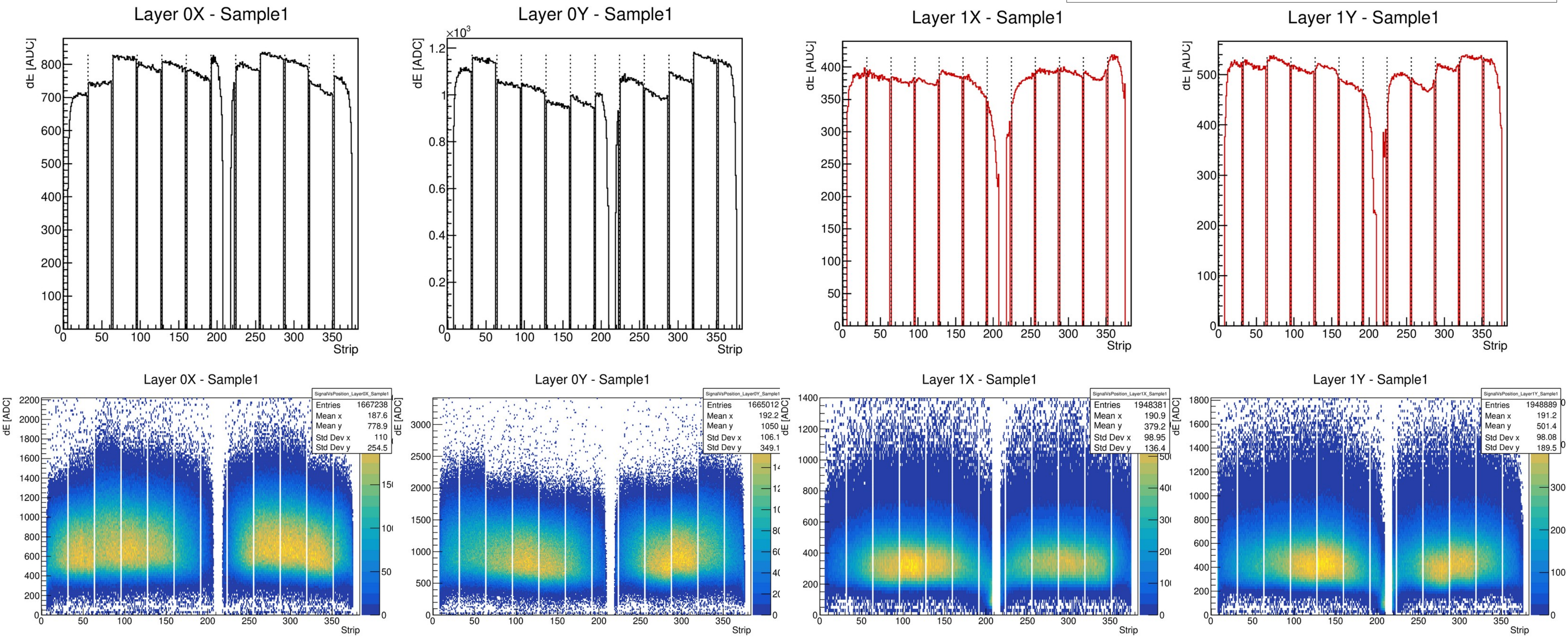


Average deposit profile

NB: By mistake, pedestal have not been iteratively cleaned when computing average, but checking pedestal distribution it seems that this has a *negligible* effect on silicon

Some investigation

Using 200 GeV electron



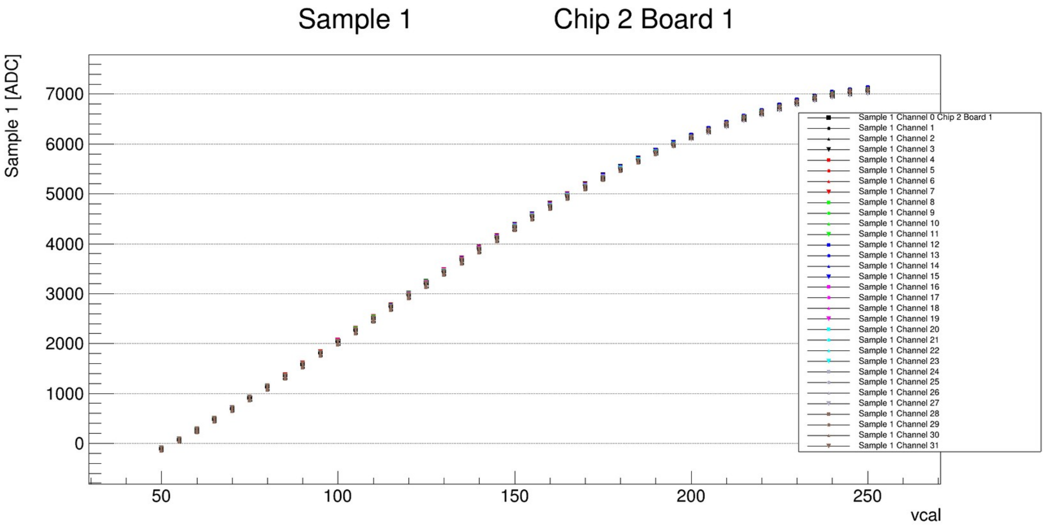
Sharp effect due to electronics (not pedestal)

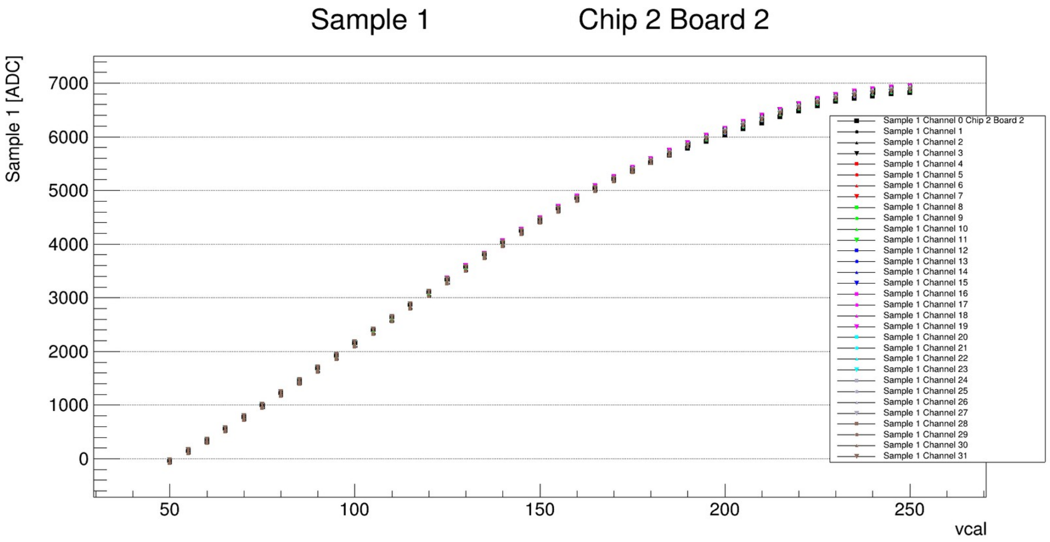
Smooth effect compatible with beam effect?

Channel-Channel Gain dispersion

From Elena’s work

Internal calibration





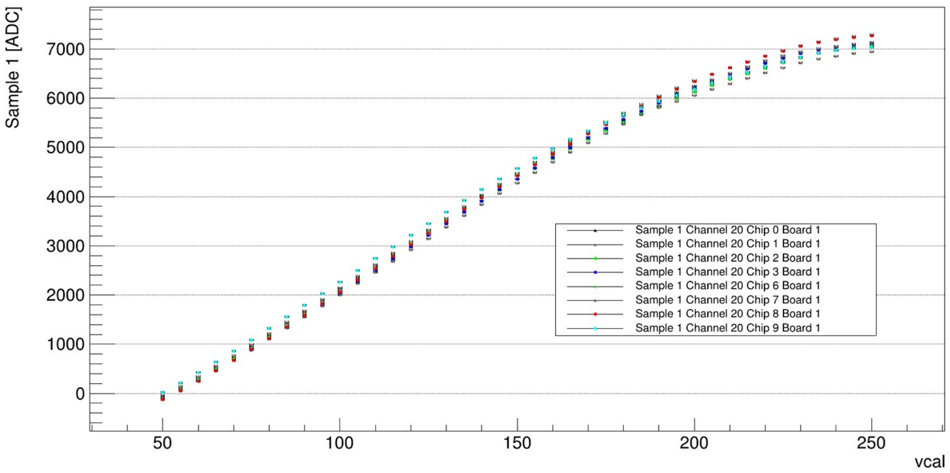
In the same chip, channel-channel gain dispersion is below 100 ADC

Chip-Chip Gain dispersion

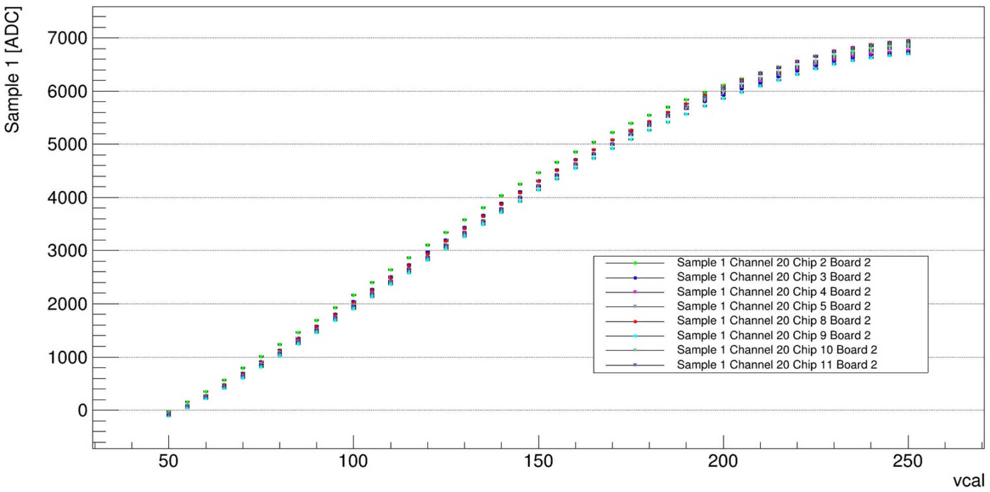
From Elena's work

Internal calibration

Sample 1 Channel 20 Board 1



Sample 1 Channel 20 Board 2

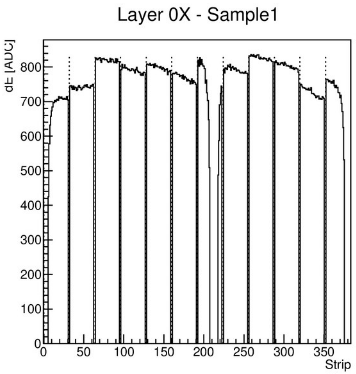


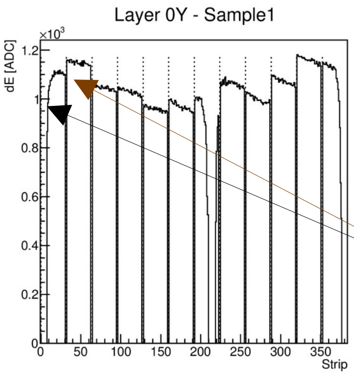
The same channel of different chips has different shape (not simply an offset or a scale factor)

The observed 300 ADC dispersion is compatible with what we see in data ...but if we compare the same chips we do not observe the same trend!

Comparison with internal calibration

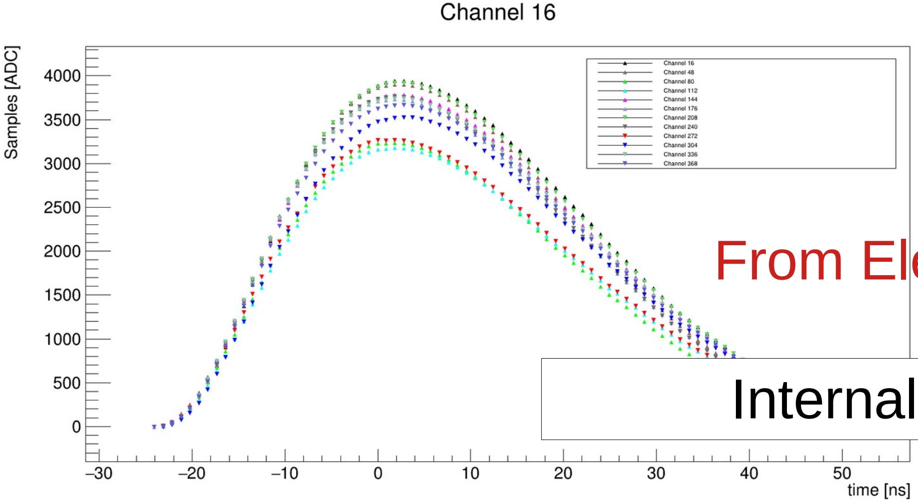
SPS-Front - 200 GeV electron



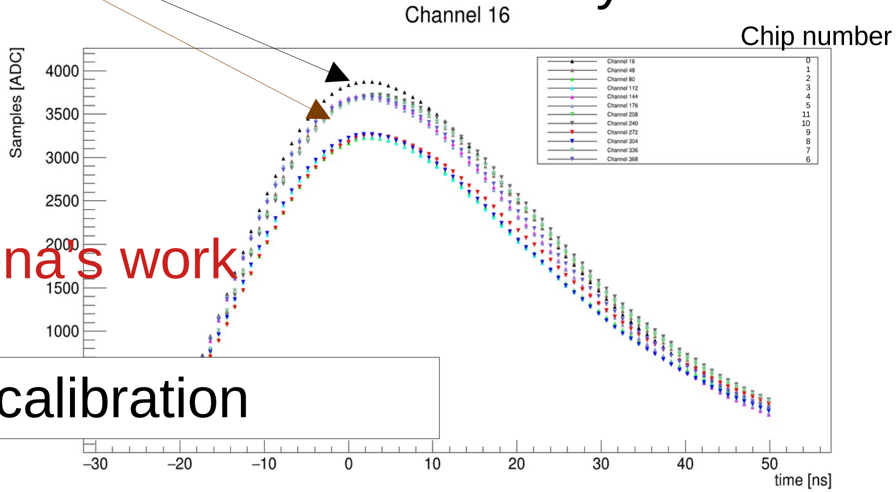


No clear common pattern...

Board 1.2 - 0x



Board 2.1 - 0y

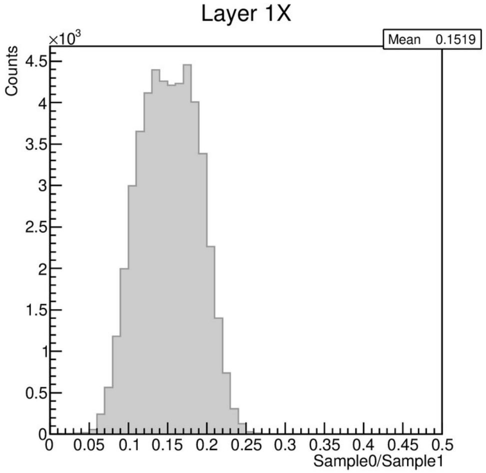


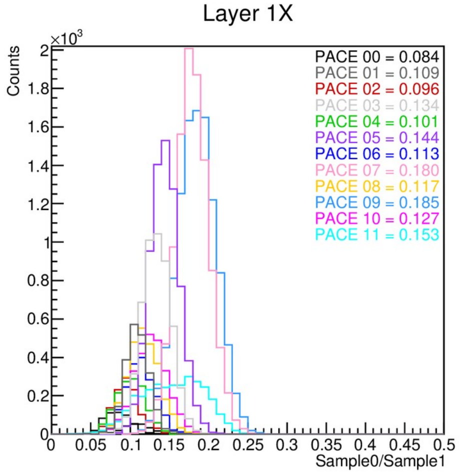
From Elena's work

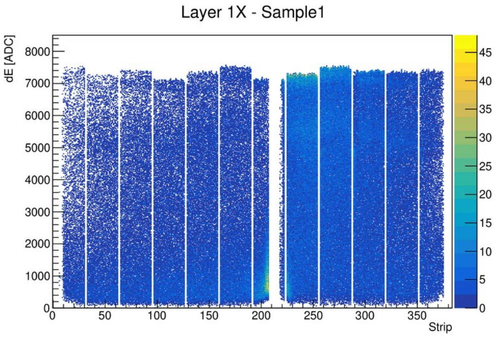
Internal calibration

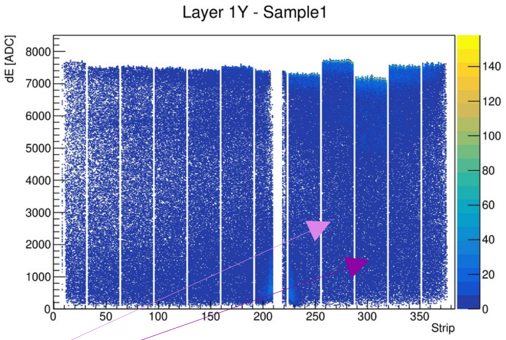
Comparison with different latency

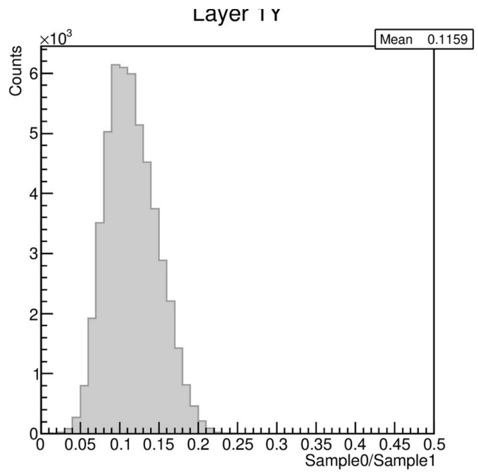
LHC - All particles – All energies

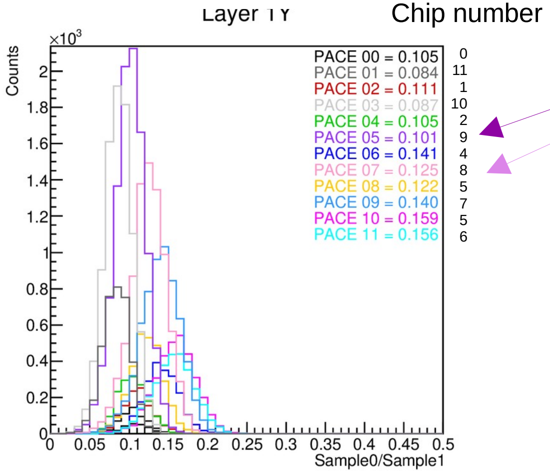












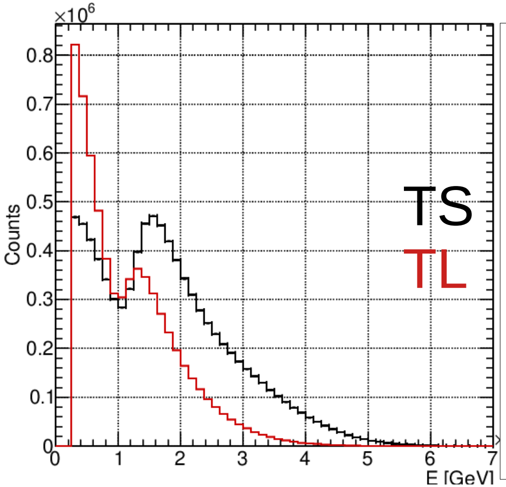
No clear common pattern...

Using LHC Data

Removing hadrons and multi-hit events

<u>Selecting only the **strip** *hit* by the track on the the **maximum** layer</u>
weighting the Si deposit with the (GSO)reconstructed energy
(with the scales of the two towers already corrected for mass shift)

(GSO)reconstructed energy



Clearly there are two problems:

- Position reconstruction clearly depends on silicon calibration
- Uncertainty on GSO energy scale calibration (for each tower)
- Different energy distribution in different regions of the detector

Weighting the deposit for reconstructed energy can only partially cure this effect, since longitudinal development - and thus deposit in a Si layer - depends on energy

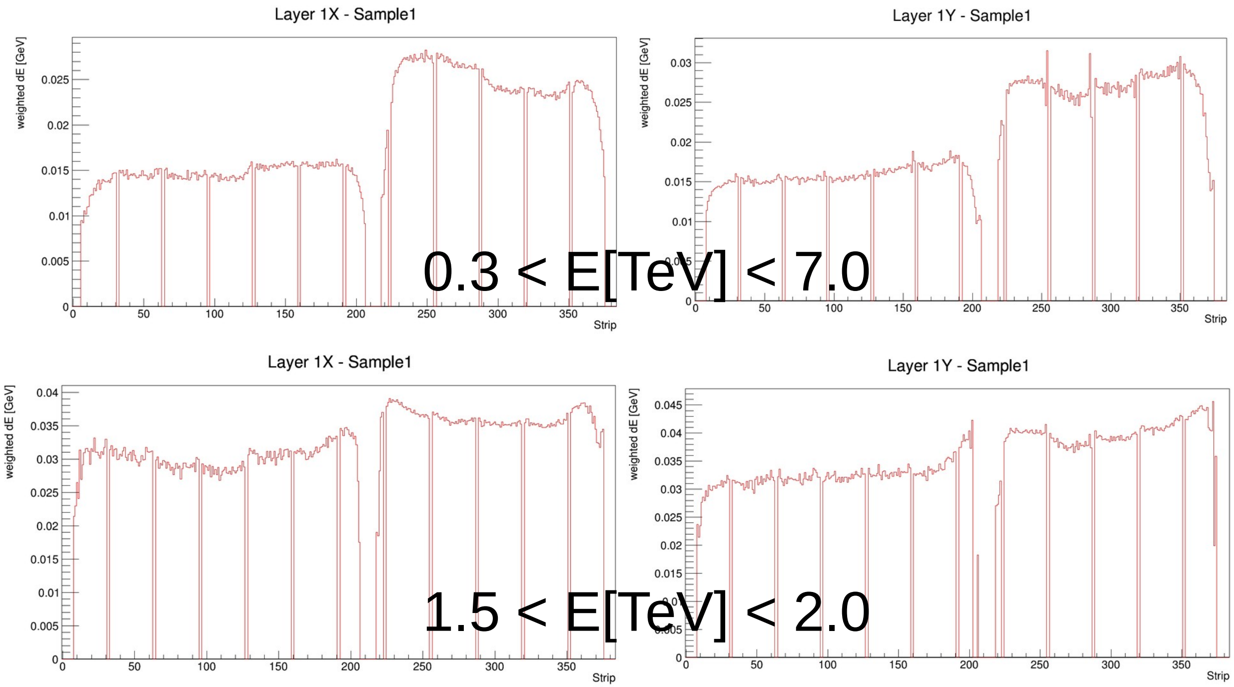
Using LHC Data

Removing hadrons and multi-hit events

<u>Selecting only the **strip** *hit* by the track on the **maximum** layer</u>
weighting the Si deposit with the (GSO)reconstructed energy
(with the scales of the two towers already corrected for mass shift)

Strange tower dependence...

No large chip dependence?



Summary

To estimate the silicon fain factors to be used for LHC2022 analysis:

- In SPS Data, we estimated signal correction due to TDC dependence
- Using all SPS Data (all energy and all geometries), we estimated gains
- Using Elena's measurements, we evaluated the latency signal correction
- In LHC Data, we estimated the average latency for each chip (not strip)
- Combining SPS gains and rescaling coefficient, we extracted the final table

Important notes

- Layer 2X/Y are difficult to calibrate because of low signal and statistics
- Layer 2X,3X/Y have a S0/S1 ratio in SPS far away from the LHC case
- Gain is energy dependent which hints unknown electronics effects

Open questions:

- What generates different gains in different chips having same S0/S1?
- Why is this relative gain different between SPS and LHC operations?
- Is capacitive coupling responsible for larger width observed in data?

Future plans for silicon calibration

I think it is important to have a beam test in 2025 for silicon calibration:

- properly set the latency to a value more similar to LHC operations
- use muons to check layer-by-layer/chip-by-chip gain dependence
- use muons to calibrate gains for layer 2x and 2y (and 3x and 3y)

RMS_{noise} ~ 7 ADC

HG/LG ratio should be around 7.5

1 MIP = 3.876 MeV/cm * 285 µm * 100000 ADC/GeV ~ 11 ADC

Assuming that noise is not seriously affected by gain, this means S/N~10

Caveat:

- I think HG option has not been implemented in driving logic yet
- MIP resolution should be very limited by the strip bonding scheme
- Some preliminary tests in laboratory are necessary...

Future plans for 2022 LHCf-only analysis

Need to define a recalibration procedure using LHC data and simulations

Elena's work can be very helpful here

Major issues:
- Recalibrate GSO gains layer-by-layer

<u>Intermediate</u> issues:
- Recalibrate silicon gains layer-by-layer and chip-by-chip

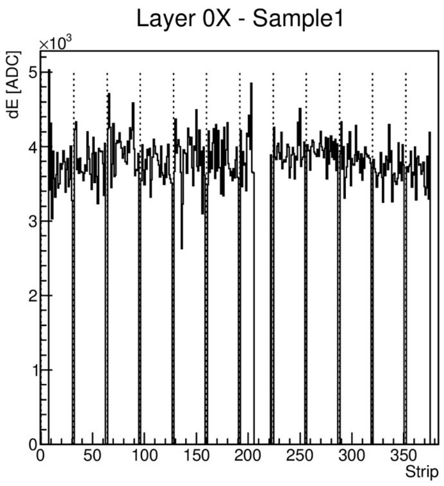
This is a major issue if we include silicon deposit in ML (for K^0)

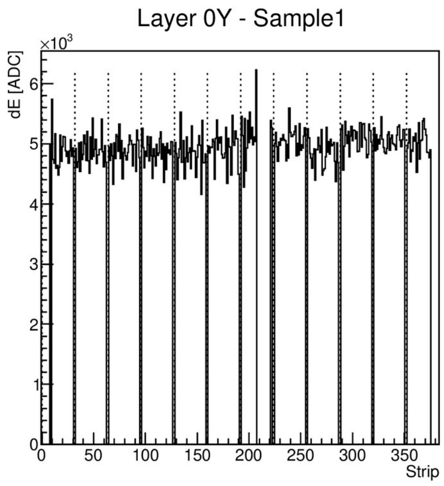
Minor issues:
- Impact of pile-up
- Beam-gas background

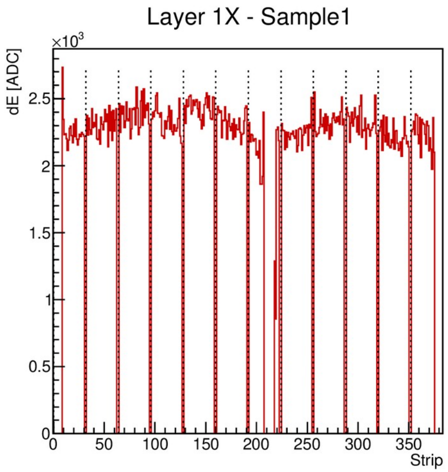
Back Up

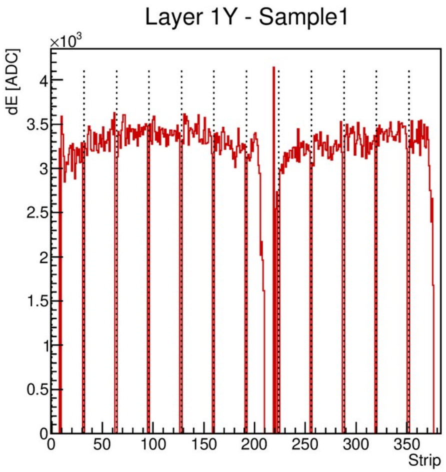
What about LHC Data?

Using 0.5-1 TeV photon

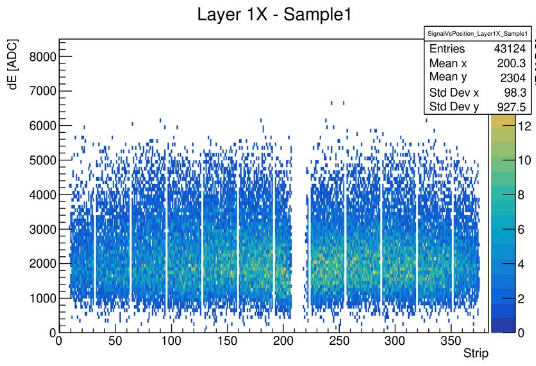


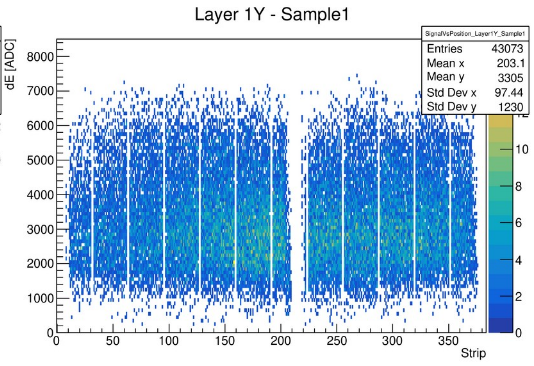






Currently, we do not have enough disk space at CNAF to process a large statistics and with a single file it is difficult to conclude something

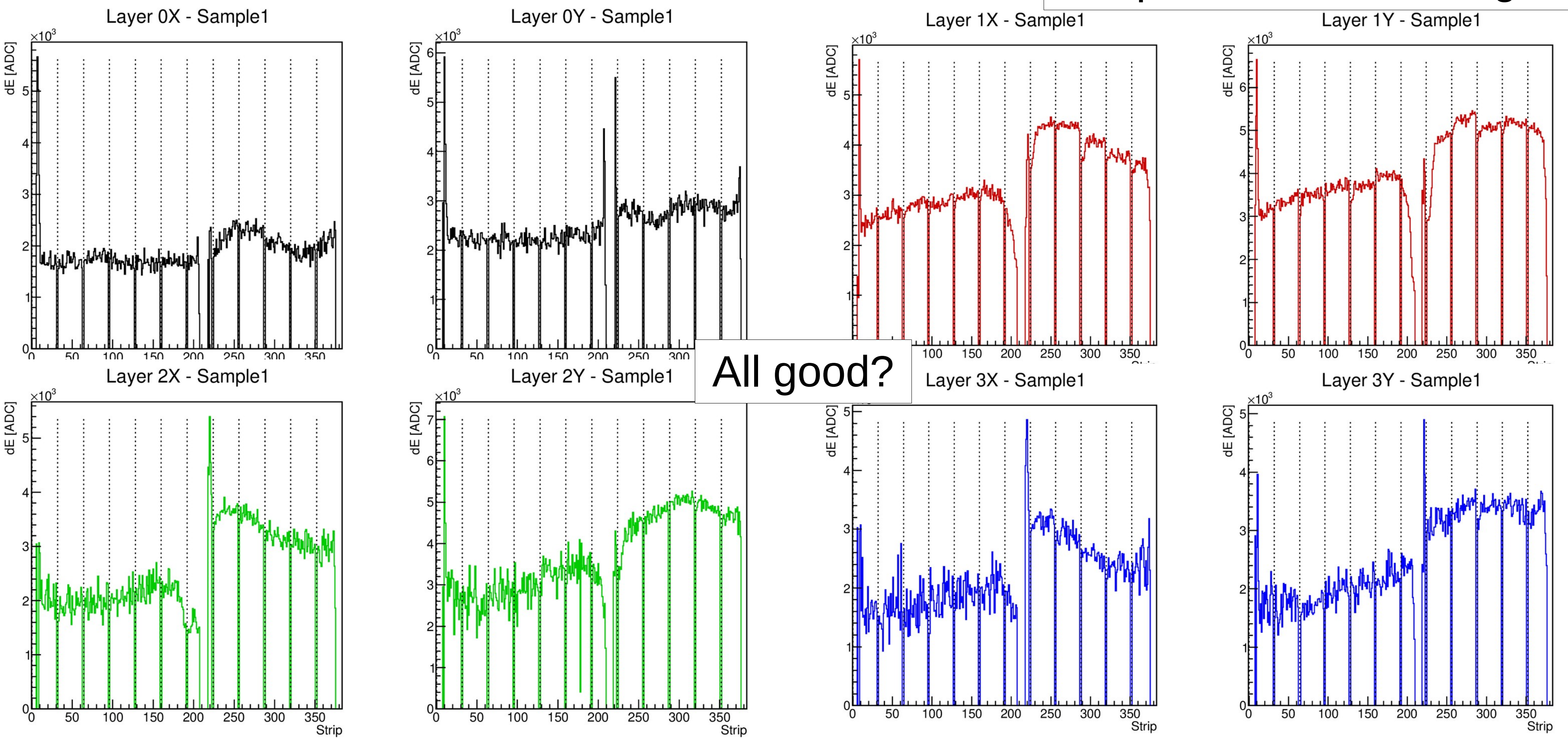




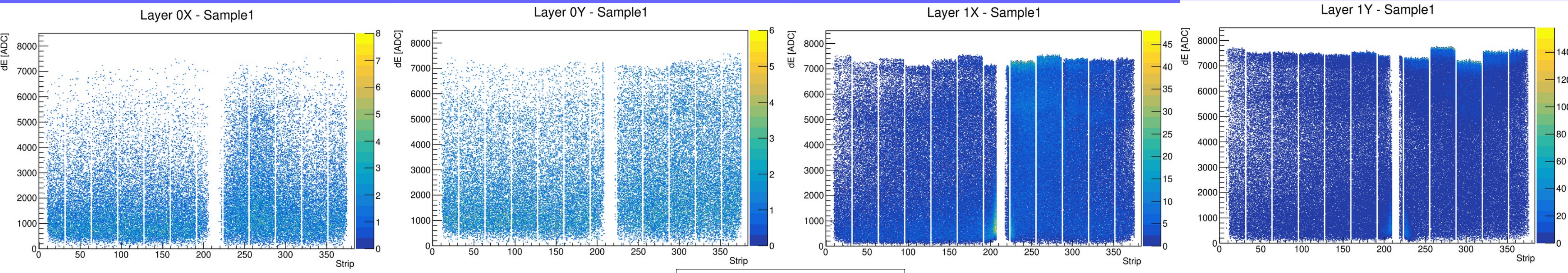
Another attempt with LHC Data

All particles – All energies

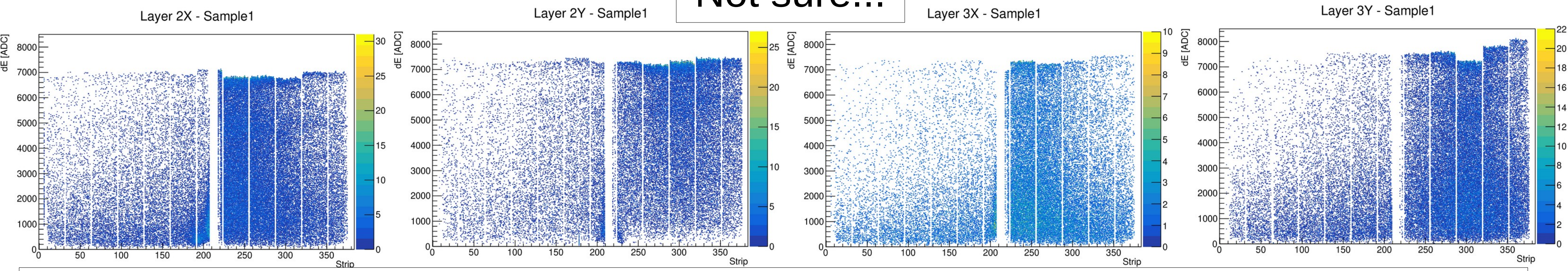
All good?



Another attempt with LHC Data



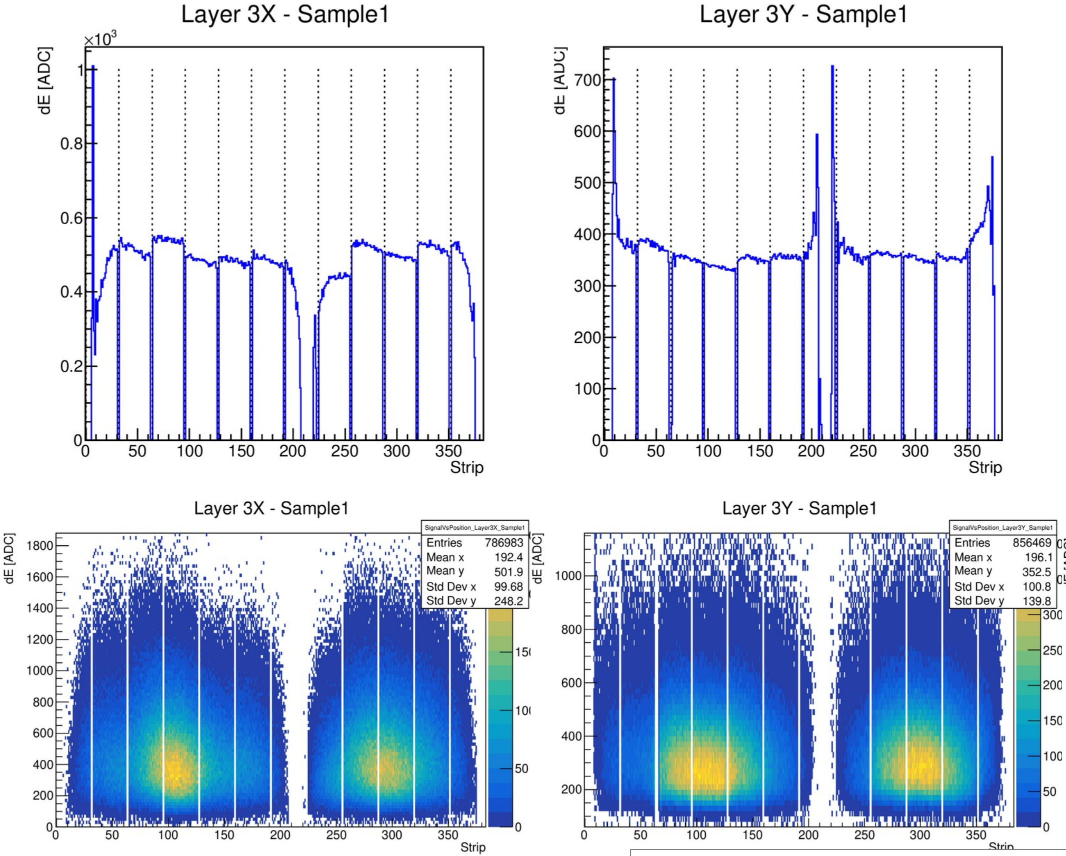
Not sure...



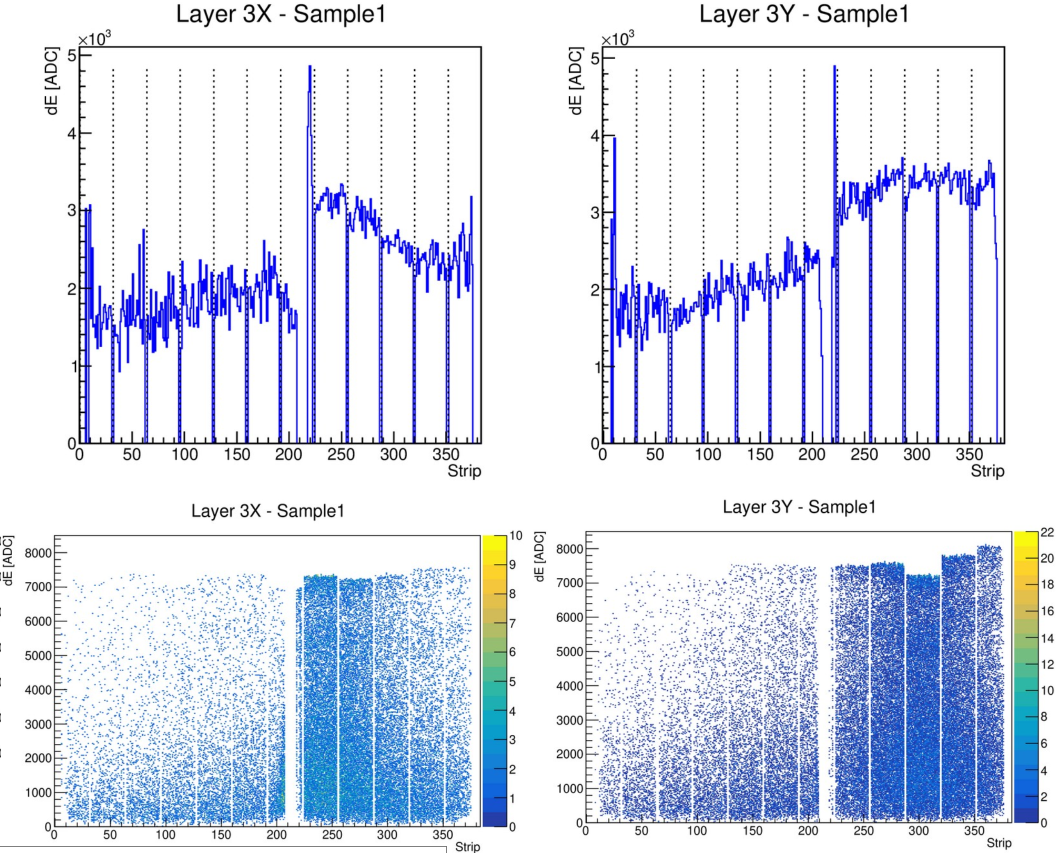
We may expect different saturation region because of energy distribution, but the chip-chip transition on some layers is clearly too much sharp: is **non-linearity** or gain that is different for different chips?

SPS vs LHC

SPS-Back - 200 GeV electron



LHC - All particles - All energies



No clear common pattern...