



RD50 HV-CMOS Meeting

Lab Measurements

Irradiated samples

(continued)

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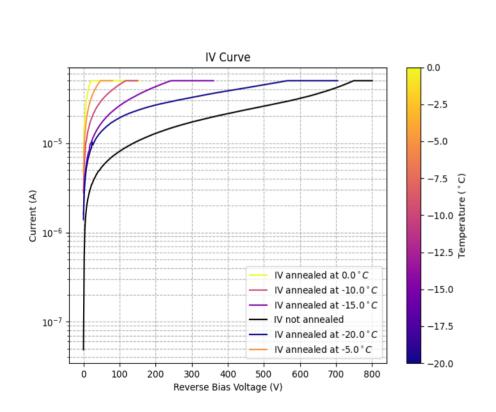
Update

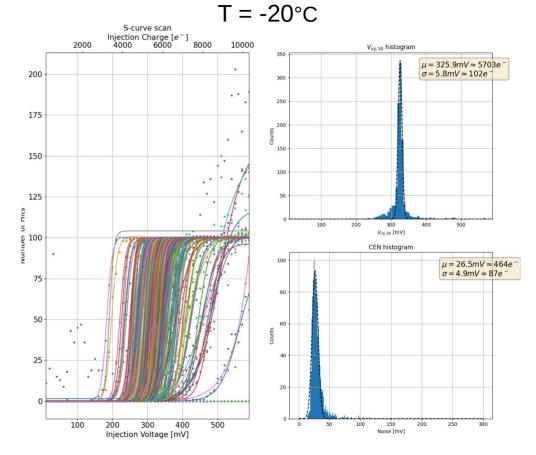
- Bonding technician interchanged the 1E16 and 3E16 samples
- Errata to last presentation:
 - Not 1E16 but 3E16 is dead
 - 1E16 is alive (measurements shown last time are from this sample)
- Sad news: HEPHY's 1E15 is not responding any more
 - 600mA on VDDA and not responding to I2C :(
 - Must have died during IV measurements or handling in between
 - Chip board now populated with W8 1E15
 - No W3 left at HEPHY





W3 1E16 backside biased

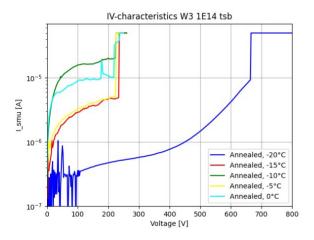


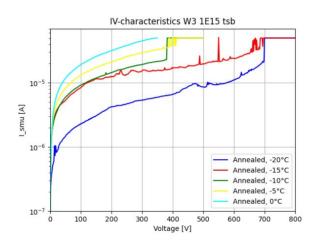


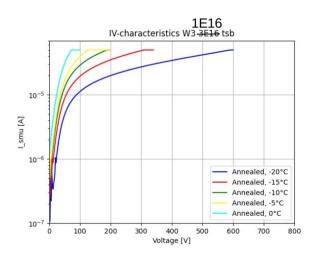




IVs topside biased





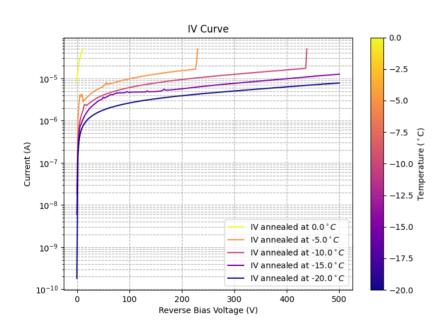






W8 1E15 topside biased

 $T = -20^{\circ}C$



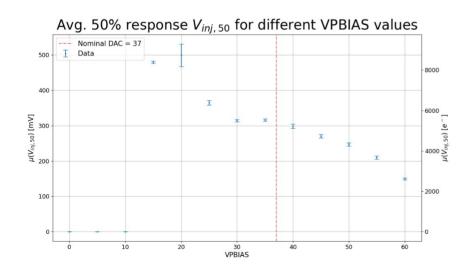
S-curve is WIP Not looking good though

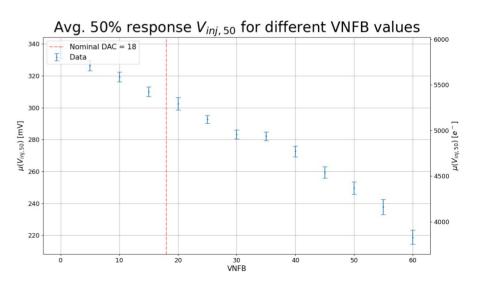




DAC Scans W3-1E16

- Performed S-curve measurements for 32 pixels
- extracted mean V_{ini,50}
- plot as function of DAC
- VPBIAS and VNFB can be used to improve "sensitivity"

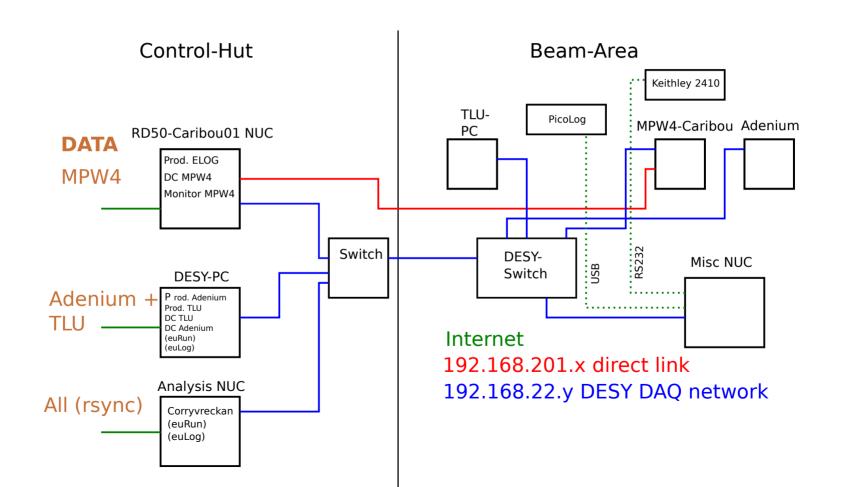








Setup proposal







Measurement plan proposal

- We have 5 samples
 - W3-1E14, W3-1E16, W8-1E15 from HEPHY
 - W3-3E14, W3-3E15
 - Biasing from top and back (when possible (W8 not possible)) → Effectively 9 samples
- Minimum time for a run:
 - Minimum statistic 200 000 tracks
 - Trigger rate of ~1kHz and ~0.4 tracks / event (both with Telepix) → minimum run duration ~ 500s ~ 8min → 10min
- Measure with lowest possible threshold settings at lowest possible temperature biased at -190V
 - Compare with non irradiated samples, make sure we measured the lowest possible threshold setting at the last testbeam
- Several samples can be biased up to 800V at -20C (hopefully properly working already at lower bias voltages)
 - Do a bias voltage scan, proposal (0, 800)V in 35V → 23 steps a 10 min → ~4h / sample
- Scan interesting DACs
 - VNFB, VPBIAS





Rough schedule

- Setup and verify with HEPHY topside ~2 days → 5 days for irradiated samples
- 9 samples → 2 samples / day
- Running over night, ~18h / day → 9h / sample
- Each sample:
 - 1) Standard measurement, Setup and debug until proper first results seen ~3h
 - Lowest threshold, -190V bias, as cold as possible → std. / best operation conditions for irradiated sample
 - Fixed threshold (~1V), -190V bias → compare samples aka fluences directly
 - 2) Bias scan
 - 0 ~800V or max. in 35V steps a 10 min ~ 4h
 - 3) DAC-scans ~2h
- This is a realistic if not conservative schedule which is realistically achievable (most likely more time available)
- FINGERS CROSSED