AGH UNIVERSITY OF SCIENCE AND TECHNOLOGY

Developments for DRD6 WP4 at AGH

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DRD6 Collaboration Meeting 30/10/2024 CERN

Objectives

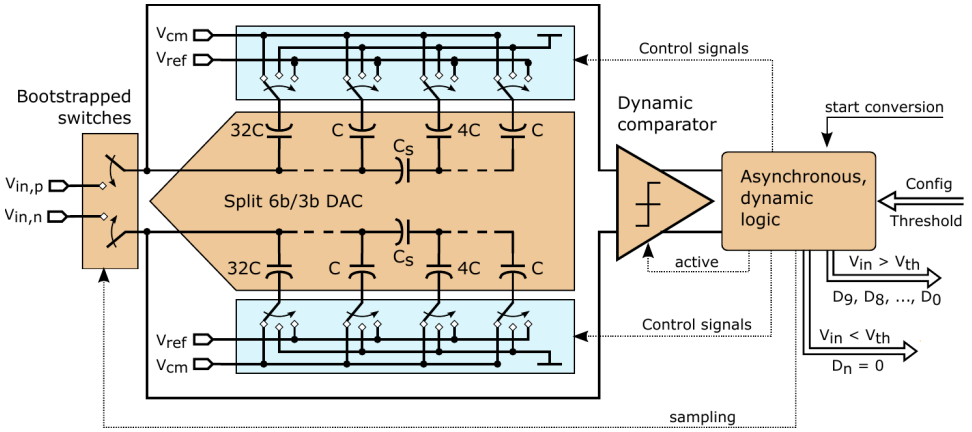
- Main goal
  - **Cooperation with WP4 partners (Omega, Irfu) in designing perfect front-end ASIC(s) for calorimetry**
    - Development of key functional blocks (ADCs, Amplifiers, Serializer&Transmitters,...) and integrating it together with partners into complete front-end ASIC(s)
    - Common request – ultra-low power ~few mW per channel
    - Technologies: presently CMOS 130/65 nm, later on CMOS28nm
    - Christophe will talk more about...
- Additional goal
  - **Continuation of works on already developed front-end ASICs (FLAME, FLAXE) for calorimetry**

Development of blocks for perfect CAL-ASIC
Lowest power fast 10-bit ADC in CMOS 130nm

Existing 10-bit ADC in CMOS 130nm used in FLAME, HGCROC, HKROC, TOFHIR

- power 680uW@40MSps
- works up to 50MSps

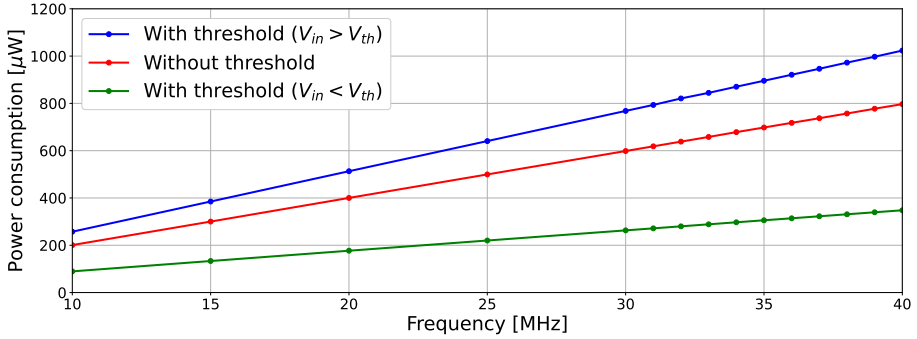
New ADC with internal threshold



To decrease power consumption, additional comparison with internal threshold is introduced, in orded to make full conversion only for signal (and not for noise)

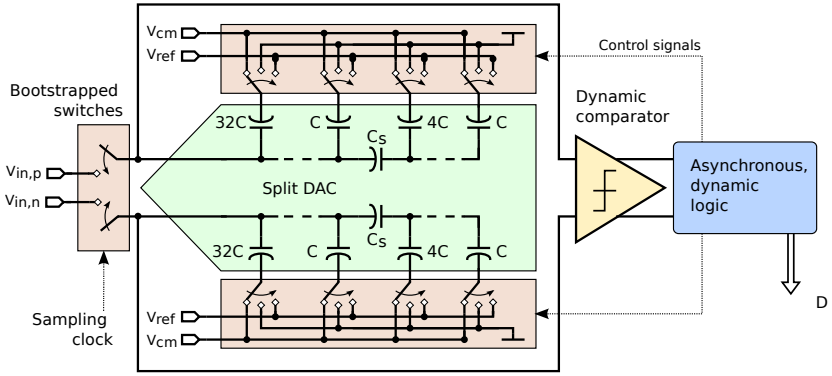
- ADC is slightly slower, but consumes much less power for low signal occupancy
- Schematic&Layout completed and simulated
- Prototype ASIC should be prepared for submission in near future...

Power with/without threshold (post-layout simulations)

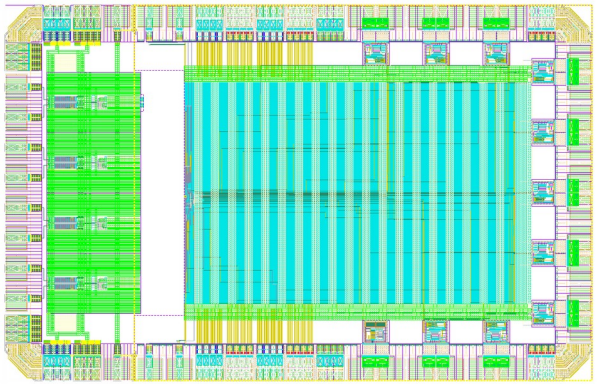


Development of blocks for perfect CAL-ASIC R&D on fast 10-bit SAR ADC in CMOS 28nm

The Goal - Ultra-low power and the highest sampling rate



SAR architecture already verified in 130/65 nm



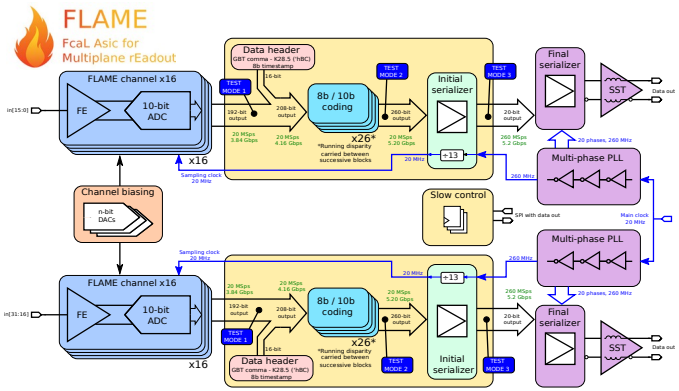
Layout of 4-channel ASIC, 280x110um^2/channel

MiniASIC submitted in July 2024...

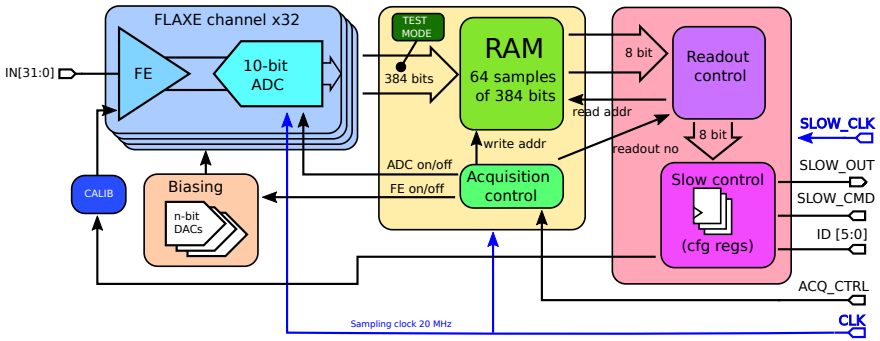
CMOS [nm]	Verification	Power@40MHz [uW]	Max Fsample [MHz]	
130	Prototype ASIC	680	50	M. Firlej et al. JINST 18 P11013 (2023)
65	Prototype ASIC	~550	80-90	M. Firlej et al. JINST 19 P01029 (2024)
28	Post-layout simulation	<150 ?	~180 ?	

FLAXE front-end ASIC for LUXE ECALp (WP1)

FLAME



FLAXE



FLAME/FLAXE are a 32-channel chips in CMOS 130nm comprising analog front-end and fast ultra-low power 10-bit ADC in each channel. FLAME has two high speed (5.2Gb/s) serialisers&transmitters, while FLAXE is intended for low trigger rate.

~1000 FLAXE ASICs were produced in 2024 and ~140 was packaged and tested

- Catastrophic yield of ~5% found – huge (leakage) currents in power domains = ~shorts
- No single chip with all channels working
- 7 chips with most (20-30) of channels working
- Channels that work – very good agreement with simulations

Preliminary conclusion (still under investigation) - production failure

New submission planned soon...