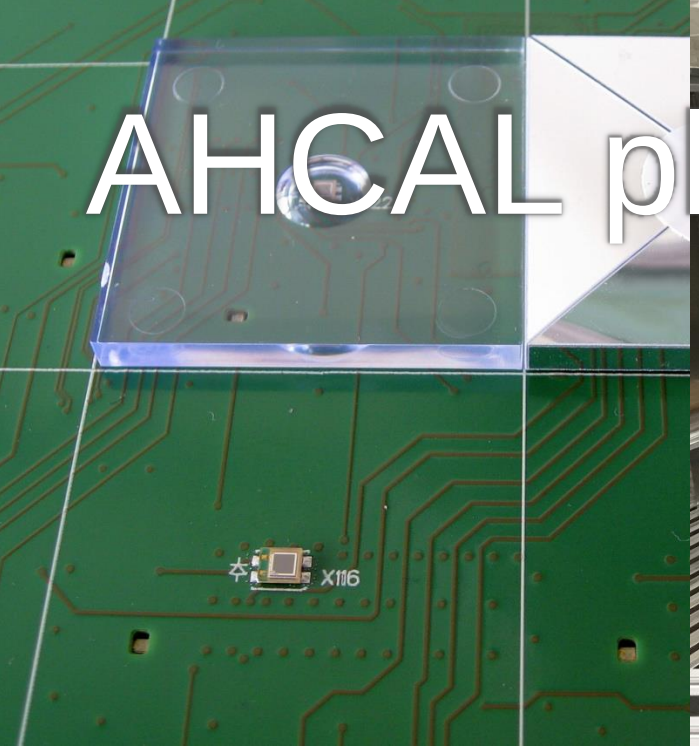
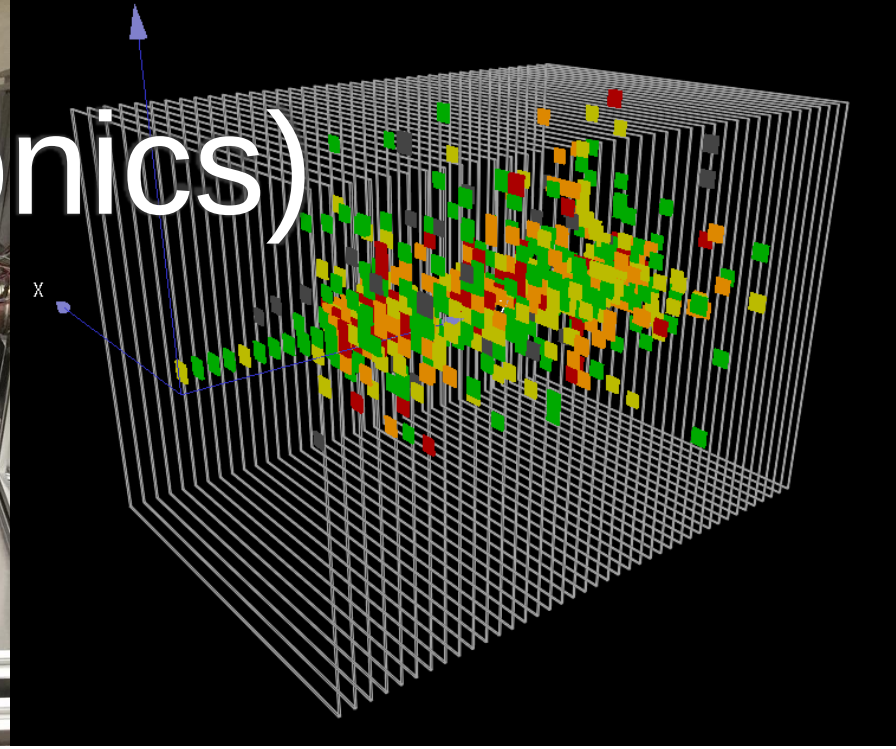
AHCAL plans (for electronics)





Katja Krüger (DESY)

DRD6 meeting, CERN
30 October 2024

HELMHOLTZ RESEARCH FOR GRAND CHALLENGES

AIDA innova

DESY.

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 101004761.

AHCAL Status

Applications of SiPM-on-Tile technology

High channel count of highly granular calorimeters remains a challenge on all levels

- production, test, calibration, software, management
- each step in size requires higher degrees of automation

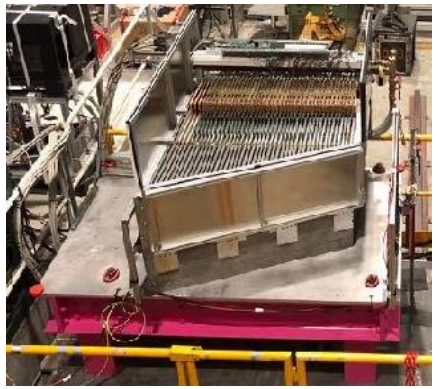
Large CALICE AHCAL technological prototype

- Demonstrated feasibility of SiPM-on-tile with integrated readout electronics
- optimised for ILC running conditions: power pulsing, no cooling inside active layers

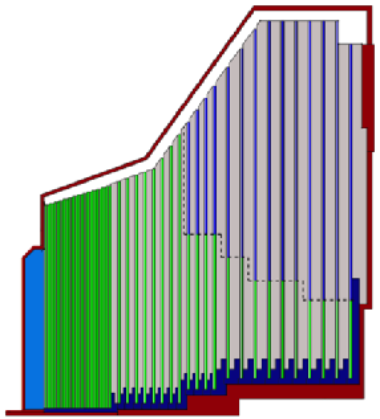
CMS HGCAL

- First use of SiPM-on-tile concept in a collider detector
- New challenges: radiation levels, data rates, operation at -30 degrees

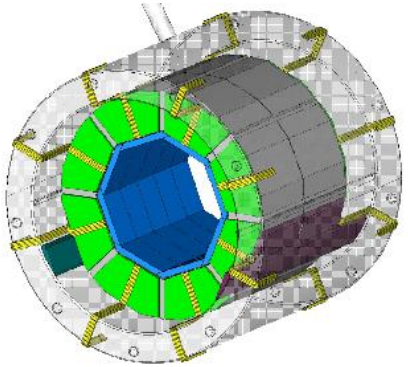
Next step in DRD6: AHCAL for a circular e+e- collider



2018
CALICE AHCAL prototype
22’000 SiPMs



2028(?)
CMS HGCAL
(2 end-caps)
280'000 SiPMs



???
CLD / ILD HCAL
barrel only
4’000’000 SiPMs

AHCAL Plans

Develop technology for further applications

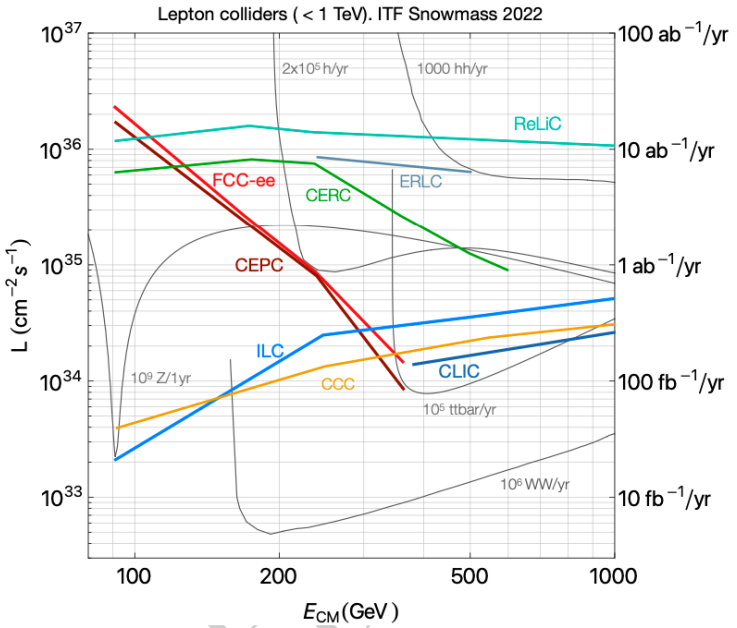
Studies towards AHCAL @ circular collider

- Continuous running
  - Both readout ASIC and interfaces (power supplies) need to support this

- High data rates at Z pole
  - Expect ~100 kHZ physics rate
  - For comparison: ~6 orders of magnitude more than HZ, but nearly an order of magnitude less than HGCAL L1A rate and smaller occupancy
  - Will have an effect on the readout system
    - Much higher data rates than for ILC -> faster bus/links
    - Maybe: change of the architecture needed (one link per ASIC instead of one bus reading many ASICs)

- Need realistic estimate of expected conditions
  - Understand active cooling needs
  - re-optimise absorber structure

- Develop hardware that can cope with these conditions



AHCAL Work Plan

Activities and task sharing

- Build a small AHCAL prototype (“EM stack”) with continuous readout and with hit timing capability
  - starting with small reconfigurable prototype in first 3-year period.

- *Task sharing* between institutes working on CALICE AHCAL (DESY, U Göttingen, U Hamburg, U Heidelberg, KIT, U Mainz, Prague, Omega)
  - Front-End boards & ASIC (DESY, HD, Omega)
    - Candidate ASICs: KLauS; HGCROC/CALOROC(?)
    - In the past (both CALICE and HGCAL) have profited strongly from ASICs developed for silicon pad readout
  - Data interface & concentration, Back-End / DAQ (KIT, Prague)
  - Photon sensors (Hamburg)
  - Scintillator materials, megatiles (Mainz)
  - Mechanical and thermal integration (Mainz, HD, DESY)
  - Common tasks for all: software, testbeams, analysis, …