Recent changes to the PcInterlock following the injection of a pilot bunch into the LHC with a D1 power converter in off state

State of protection before the issue

- Circuits operational mode is monitored by SIS (e.g. simulation)
  - Circuit state monitoring was removed during LS2
  - Wrong mode = no injection
- Interlocked circuits faulty state is monitored by PIC
  - Faulty state = dump
  - Note: OFF is not a faulty state
- PcInterlock monitors that the circuits current is within given tolerances
  - It does not act on the state of the circuits by design, it only considers circuits in states: IDLE, ARMED or RUNNING
  - Wrong current = dump (depending on the circuit family, table in the next slides)

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Weakness:

Working circuits in invalid states are not monitored (e.g. OFF)

Issue on 10/04/2024

1. Successful MPS test involving switching OFF of RD1.LR1
2. Preparation of the machine for beam
3. Injection of pilot beam with RD1.LR1 accidentally left OFF
4. Quench of triplet IT1

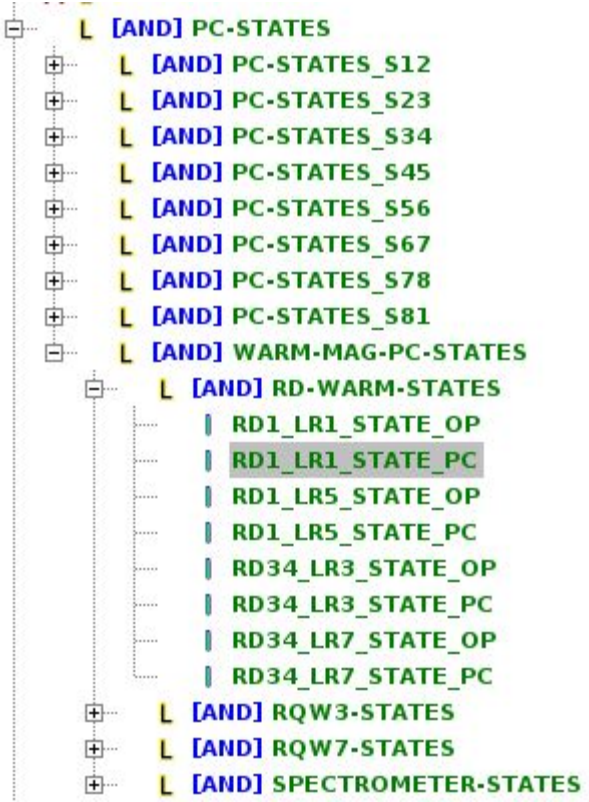
RD1.LR1 protection issue

- Following a test for triggering the FMCM without PC fault during an inter-scrubbing period, the RD1.LR1 separation dipole was left off accidentally for the probe injection.
  - The test does not seem fully conclusive to me, FMCM seems to trigger with a delay.
- When the probe was injected, it was lost in the IT1, and triggered a **quench of IT1**.
- This is a "**feature" in the PC_INTERLOCK:**
  - The system correctly **ignores orbit correctors in OFF state** because we often operate with one of them missing (for availability).
  - But for any other circuit, a circuit that is not ON must NOT be ignored.
  - PIC/WIC **do not interlock** with a circuit is just **OFF**.
- Today we will restore a STATE test on injection for all circuits except for the orbit correctors.
  - Existed in the past, was removed due to redundancy with PC_INTERLOCK.
- **This event is a good example of why, in the design of LHC MP, we enforced by HW to always force a probe injection into an empty ring.**

LHC 2024-04-10 Morning Meeting
https://indico.cern.ch/event/1397435/

Mitigation #1 SIS

- STATE PC is now checked in SIS
  - Valid states: IDLE, ARMED, RUNNING, ABORTING
  - All other states are invalid (e.g. OFF) → interlock
- The check is performed for every circuit
- Interlock prevents injection



Mitigation #2 PcInterlock

- PcInterlock checks that the PCs currents are within given tolerances
- Previously, checks were performed only for “active” PCs
  - “active” = IDLE, ARMED or RUNNING
  - “inactive” = all other states
- Now, each “interlocking strategy” have access to the state of each PC
- Logic for interlock depends on the circuit type

Circuit type	# of inactive PCs to interlock
RBs, IPDs	1
RQs, IPQs, WARM QUADS, TRIPLETs, TUNE TRIMs	1
BBLRs	1
Orbit correctors	STATE is ignored

Implementation in production

- Mitigation #1 SIS
  - Deployed on 10/04/2024
- Mitigation #2 PcInterlock
  - Required changes in PcInterlock software are implemented and tested locally
  - Pending test with LHC circuits
  - Deployment during TS2

    (could be anticipated if necessary, 1 shift needed for testing)