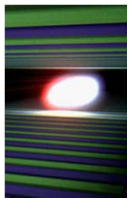
Libera Workshop 2011

Experience with Noise and Signal Integrity within a µTCA crate

Frank Ludwig – DESY
for the LLRF Team

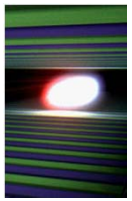
Outline



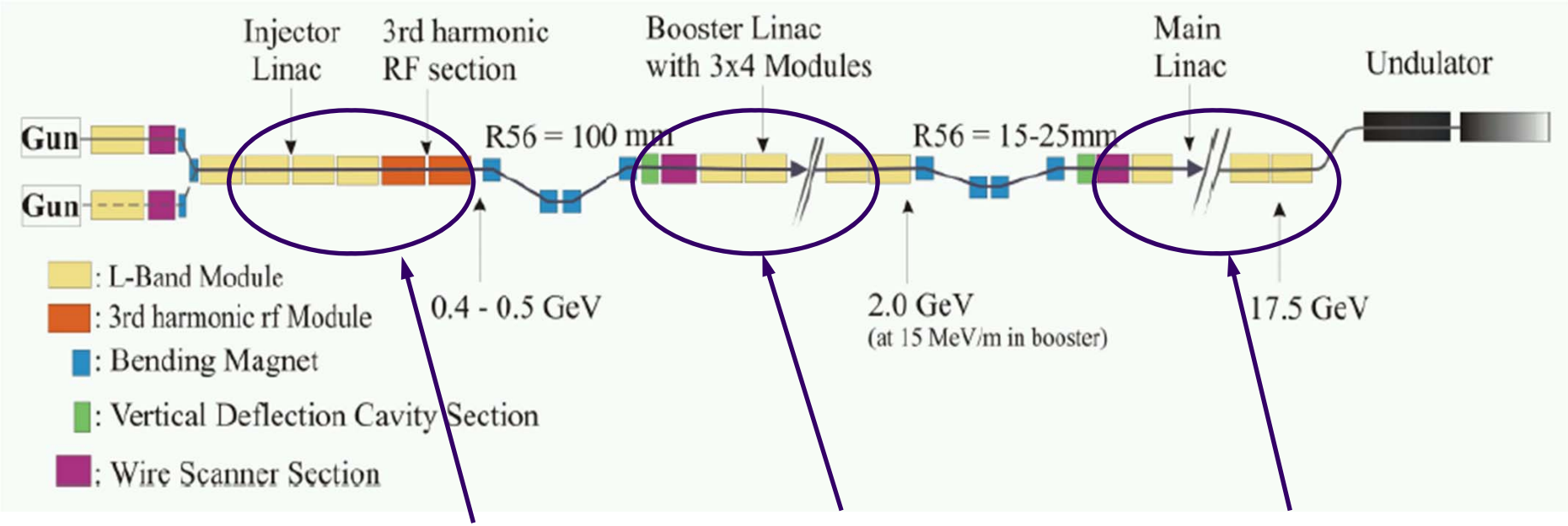
- Motivation / Requirements / Status
- Noise, Drifts and Distortions in a LLRF system
- Signal Integrity in the uTCA architecture
- Beam Operation
- Outlook

European XFEL

Motivation



- **Requirements for the cavity field stability (long- and short-term) :**



Cavity field @ 1.3GHz :
Amplitude and phase stability

$\Delta A / A_{rms} = 0.01\%, \quad \Delta\varphi_{rms} = 0.01\ deg$

$\Delta A / A_{rms} = 0.03\%, \quad \Delta\varphi_{rms} = 0.03\ deg$

$\Delta A / A_{rms} = 0.1\%, \quad \Delta\varphi_{rms} = 0.1\ deg$

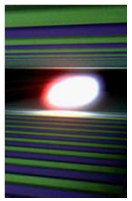
FLASH. Free-Electron Laser FLASH

A cavity field fluctuation of 1% causes 6ps bunch arrival time:
0.0016% required for 10fs (without feedbacks)

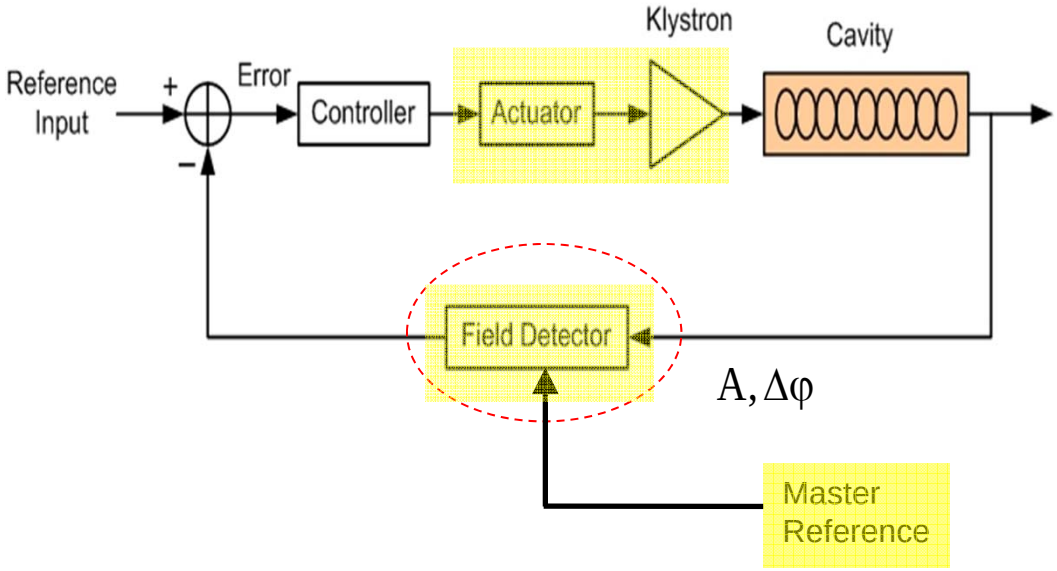
F.Löhl, „Optical Synchronization of a Free-Electron Laser with Femtosecond Precision “, Hamburg 2009, Section 4.2

HELMHOLTZ ASSOCIATION

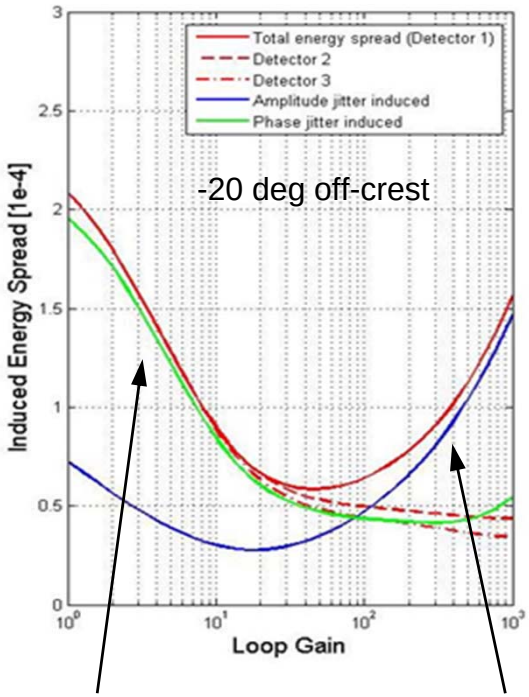
Motivation



Field regulation and noise sources :



Beam energy jitter (simulated)

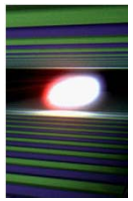


Main requirements for the field detector

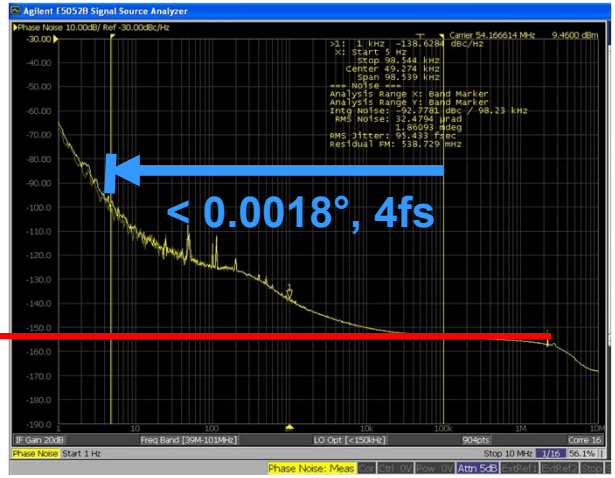
- Shortterm amplitude/phase stability	<0.01%,<0.01deg (10Hz-1MHz)
- Longterm amplitude/phase stability	0.01%, 0.01 deg (forever-10Hz)
- Nonlinearity	< -55dBc, 1% error
- Channel crosstalk	< -70dB
- Overall latency	<100ns

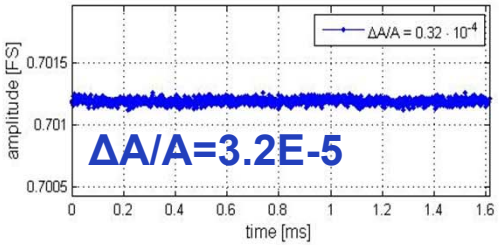
Actuator phase noise ⟷ Field Detector amplitude noise

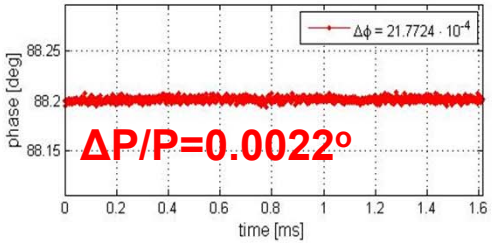
Noise: Single cavity resolution

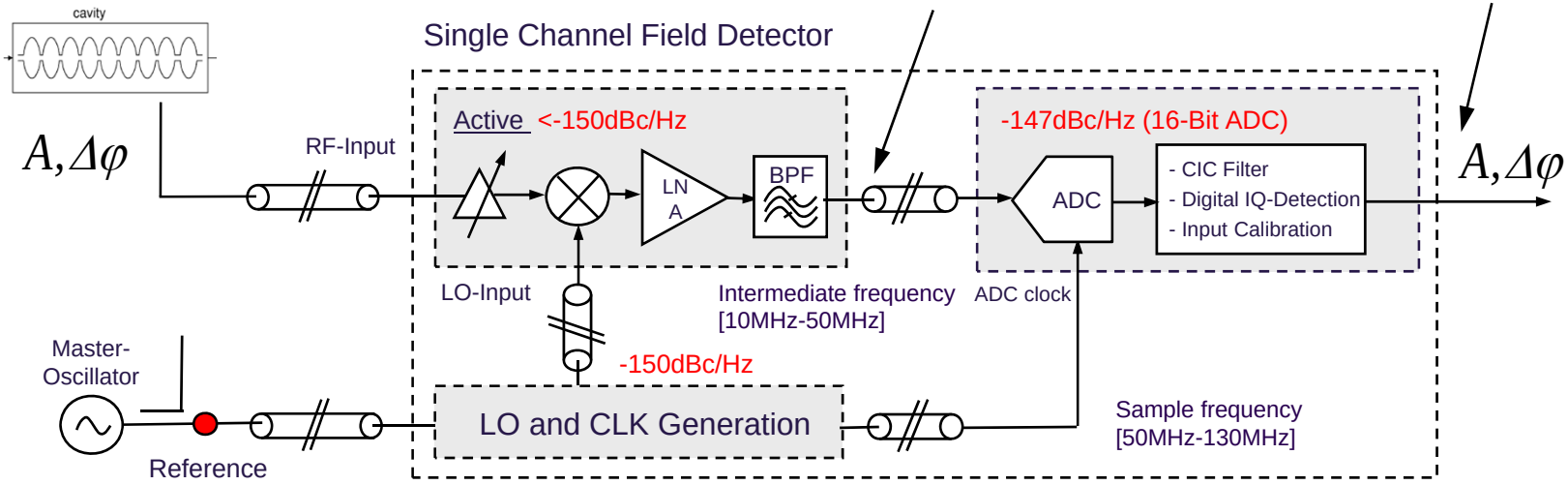


- **Non-IQ sampling field detection : Noise balance**
  - Receiver
  - LO-Generation
  - ADC (limitation)









Drifts: Single cavity resolution

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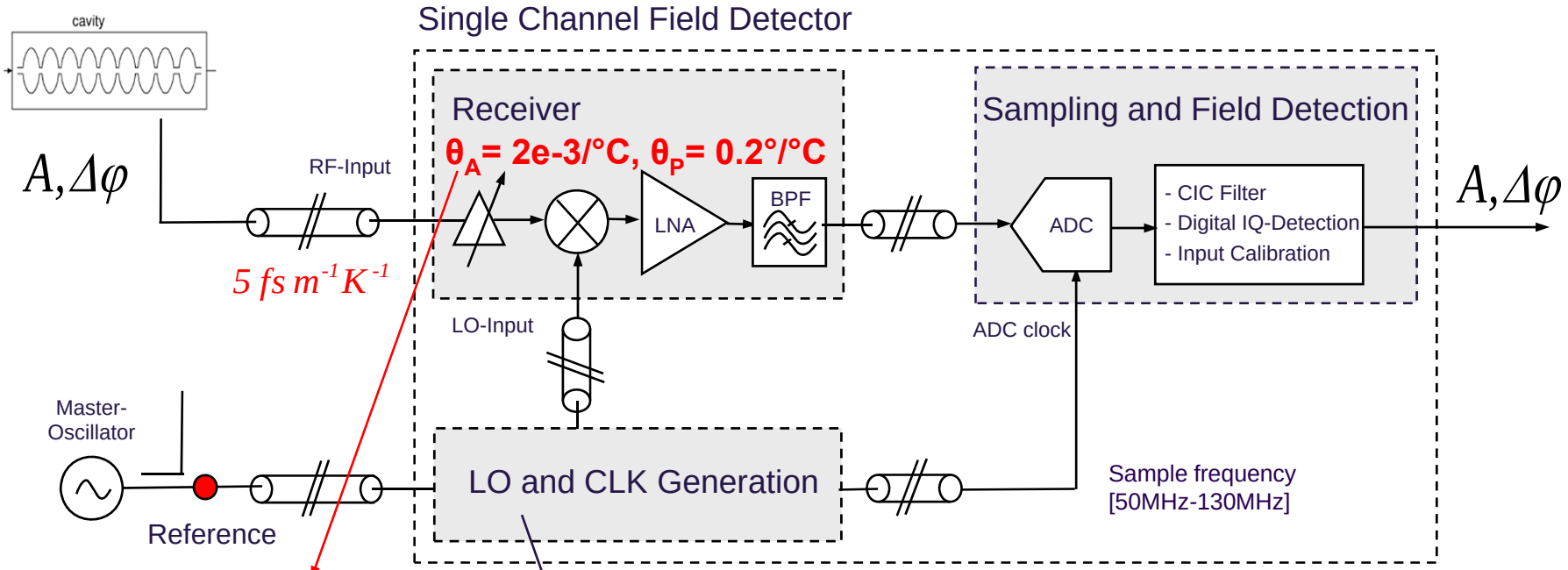
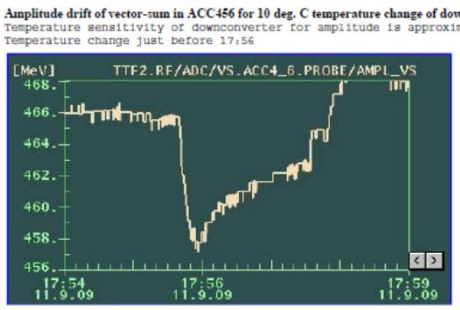
- **Long-term instability of the field detection :**

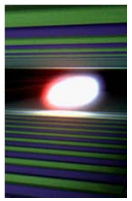




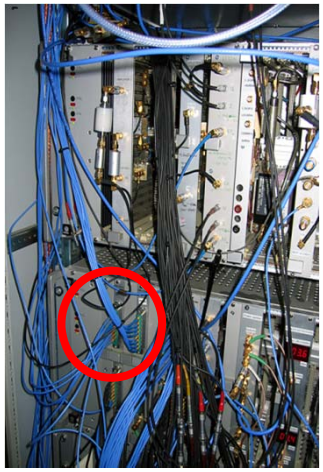
…caused by temperatur and humidity act on cables, dividers, amplifiers, filters...

…hopeless in a distributed system...

Distortions: Mechanical vibrations

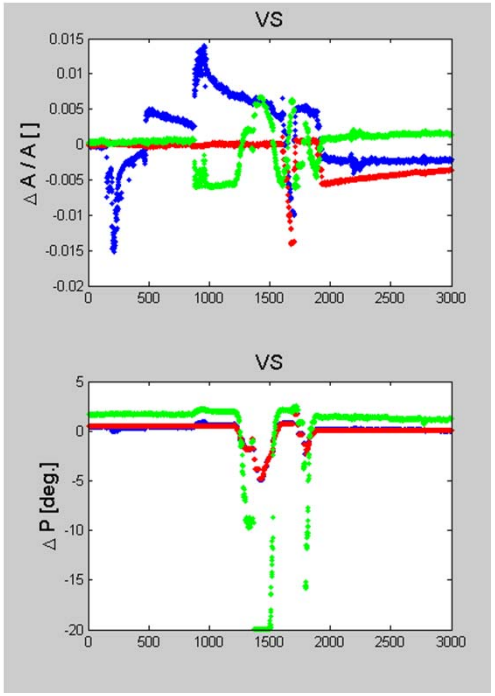


ACC1 pickup-cable vibrations :

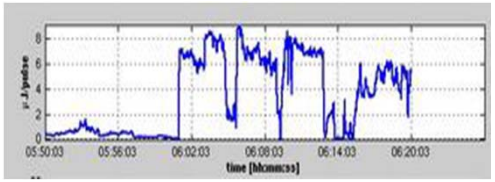


ACC1-LLRF-System

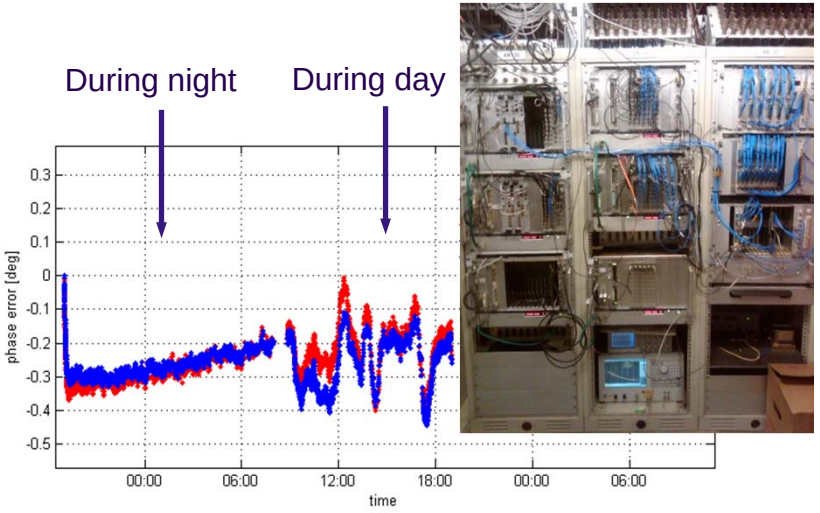
Several degree vector sum phase changes

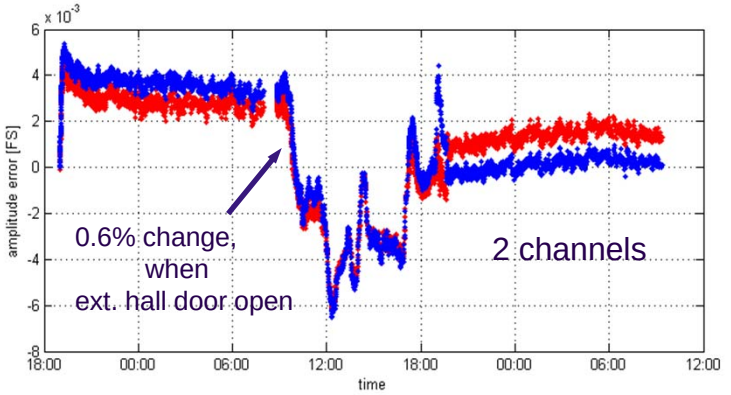


SASE:



ACC456 Ext. Hall 3 :





Status 2010: FLASHs LLRF system

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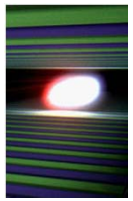
Upgrade of all injector RF stations

- New cabling for RF-Gun, ACC1, ACC39
- Enclosed racks for better temperature stability
- Parallel cabling for development system
- Careful noise investigation, documentation

→ Energy stability improved by a factor of 3 to dE/E=5E-5.

We‘re done ? . . .

Consequences from FLASH operation



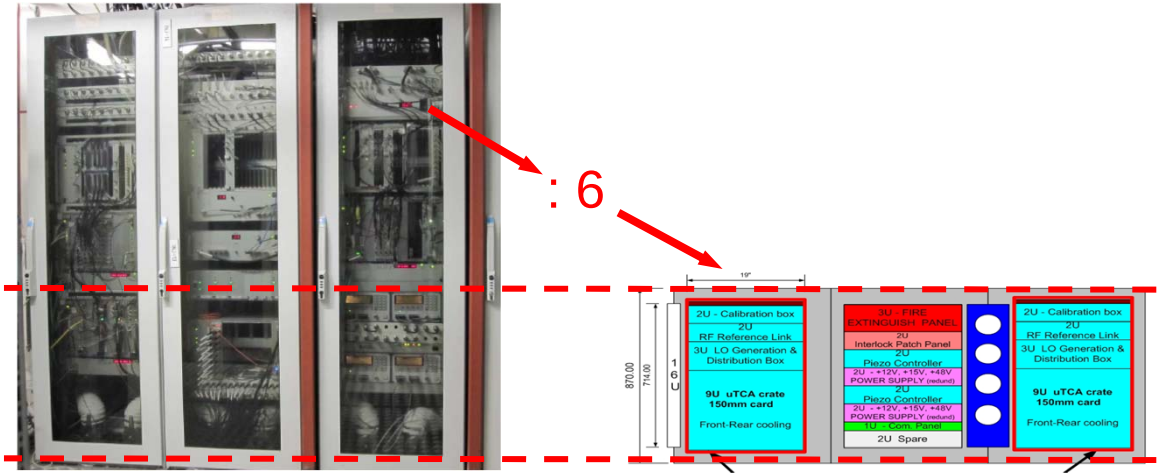
Actual FLASHs LLRF limitations

- Rack size is strongly limited (J0-16U, L1-26U) compared to (ACC1-42U)
- LLRF system is outside the tunnel
- Central FPGA concept (limited comp. power)
- Process only 8x3 cavity signals (P,F,R)
- SimconDSP 14-bit ADC limitation
- Baseband field detection
- No redundancy
- Pluggable connectors are not drift compensated
- No channel parallelization for more performance

Roadmap for the LLRF

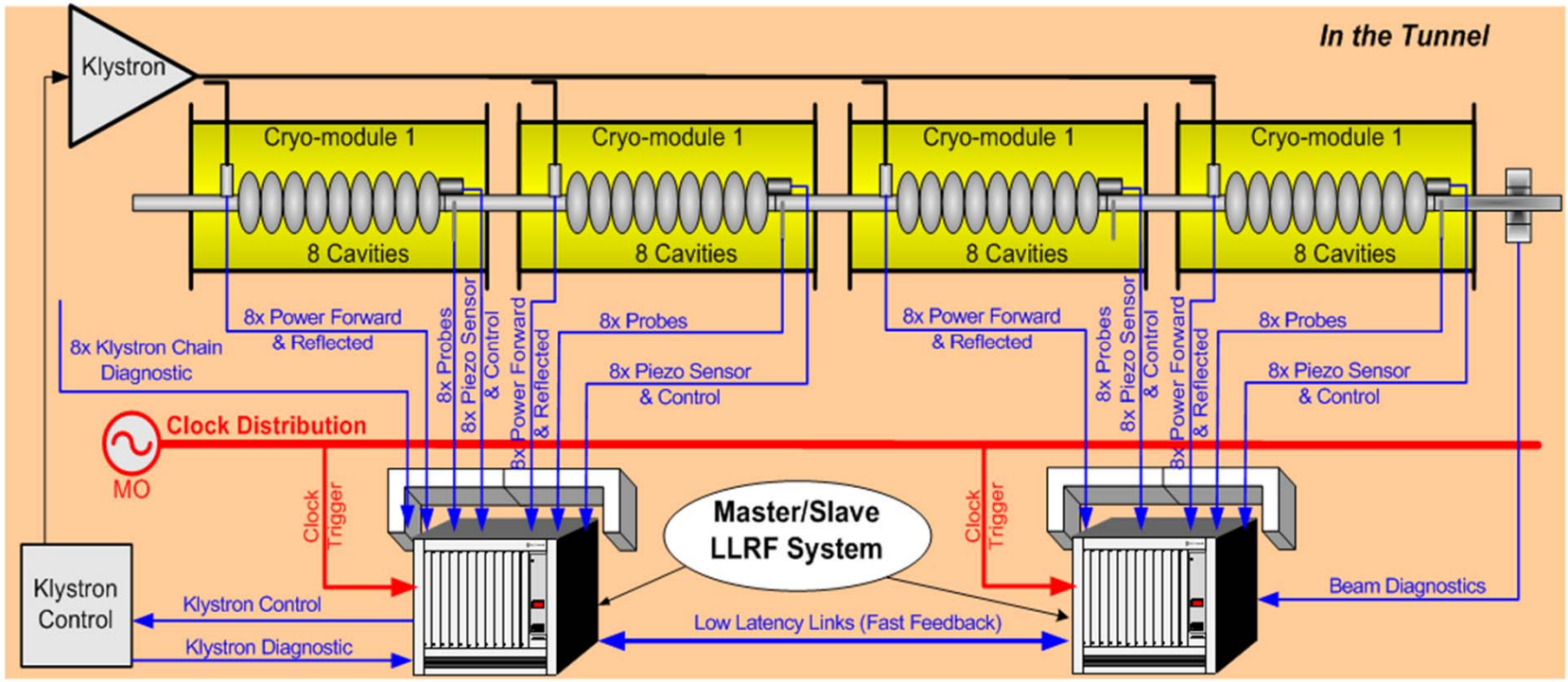
- VME -> uTCA (uAMC, uRTM) concept

- LLRF system will be in the tunnel
- Distributed FPGA, DSP concept
- Process 2 times more signals
- Lowest spectral density (16-bit ADCs)
- Non IQ sampling scheme
- Redundant systems in the injector
- Rack will be fully drift compensated
- Scaleable system



Consequences from FLASH operation

- **2 semi-distributed uTCA stations supply 4 cavity modules (J0,L1,L2,L3)**



Driving Argument → Short pickup cables for low drifts (10fs/m/K) and prevent crosstalk from high power cables

Packaging Balance for <-80dB Measurements

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Orthogonal packaging balance:

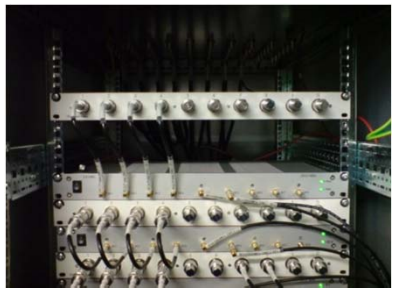
Modular Crate System :

(+) Sharing resources with the market
(+) Compact design
( ) Channel parallelization limited
(--) Not robust against distortions
(--) GND imperfections

Balance Limits ?

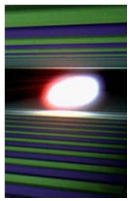
19“ Module Design :

(--) Special Design
(--) More space consuming
(+) Channel parallelization
(+) Robust against distortions
(+) No GND imperfection

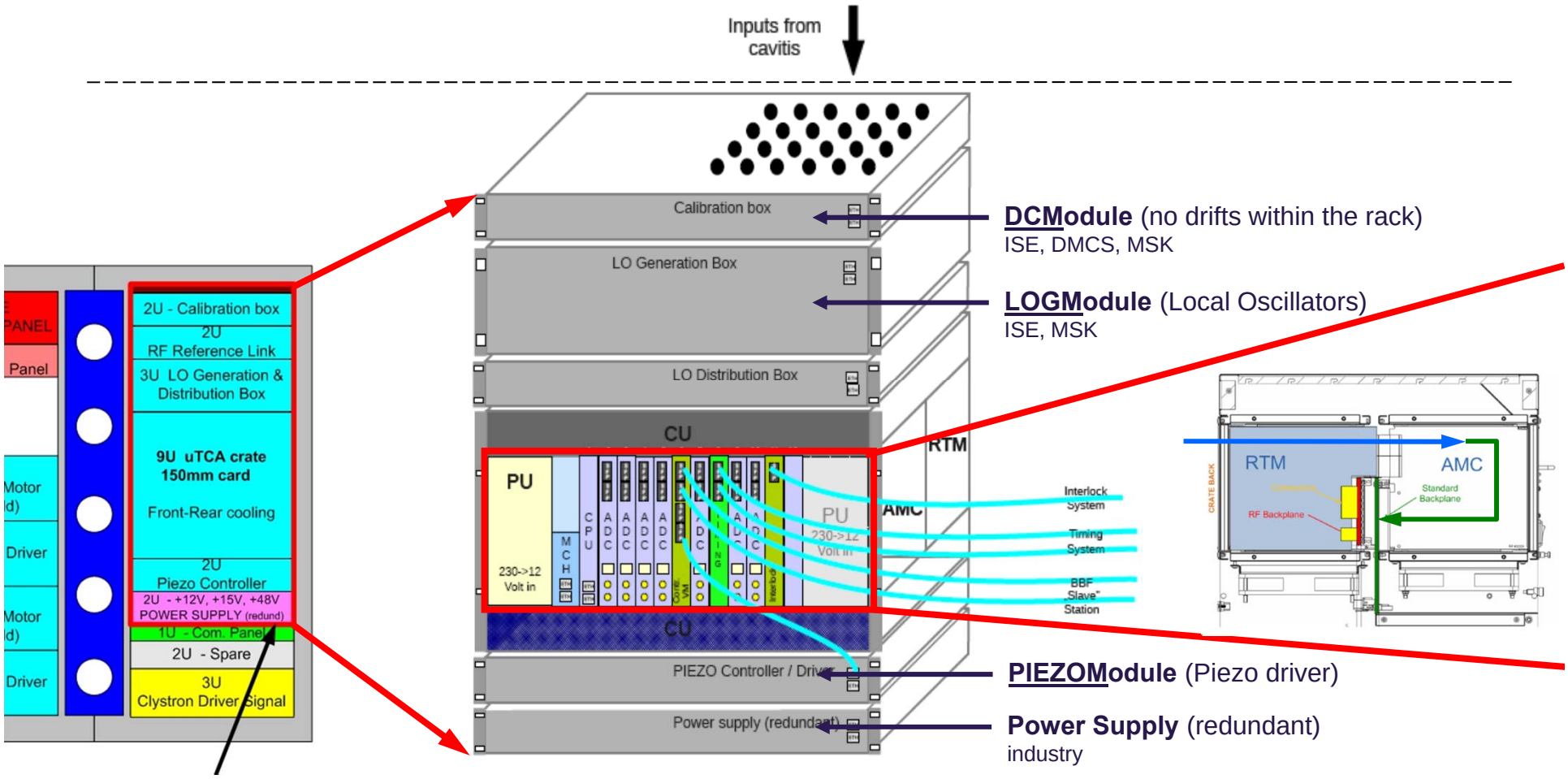


Crate signal integrity →
- GND concept has to be revised (towards RF-housing)
- Inner distortions have to be reduced (Power Supplies)
- AMC, RTM board classification

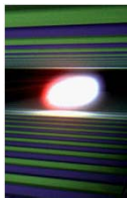
uTCA LLRF hardware platform



- **How will a LLRF System look like inside . . . 19“ modules . . .**

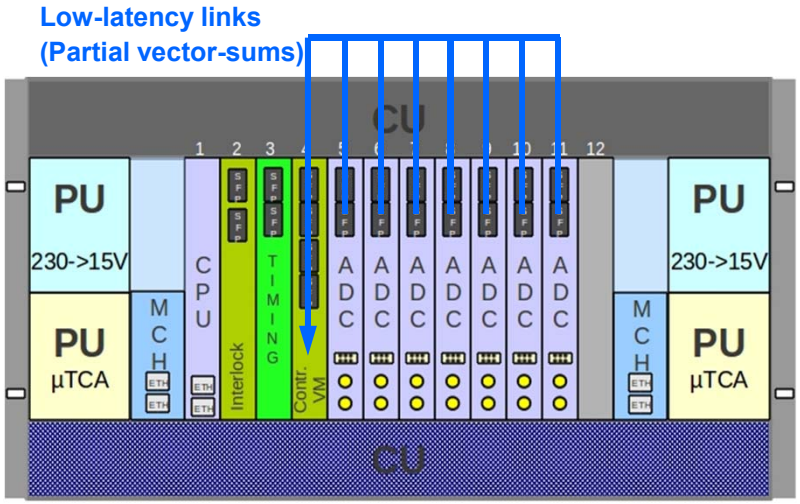


uTCA LLRF hardware platform



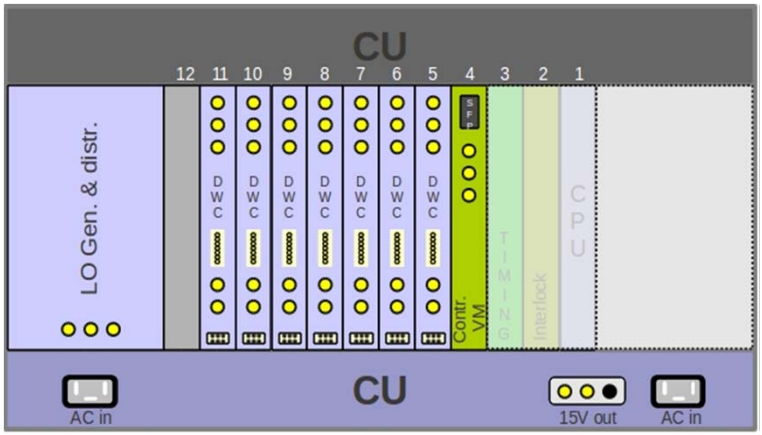
- **. . . and the crate . . .**

AMC front : (data pre-processing)



Slot #01: CPU	(Industry)
Slot #02: Interlock	(MCS)
Slot #03: Timing	(MCS)
Slot #04: **LLRF Controller**	**(uTC / DMCS, MSK)**
Slot #05: ADC, Klystron Chain	(Industry, MCS, MSK)
Slot #06: ADC, VS Reflected	(Industry , MCS, MSK)
Slot #07: ADC, VS Reflected	(Industry , MCS, MSK)
Slot #08: ADC, VS Forward	(Industry , MCS, MSK)
Slot #09: ADC, VS Forward	(Industry , MCS, MSK)
Slot #10: ADC, VS Probe	(Industry , MCS, MSK)
Slot #11: ADC, VS Probe	(Industry , MCS, MSK)
Slot #12: free	

RTM rear: (signal conditioning)



Slot #01: -	
Slot #02: -	
Slot #03: -	
Slot #04: **Klystron Driver**	**(uTC VM / DMCS, ISE)**
Slot #05: **DWC, Klystron Chain**	**(DWC8300 / ISE, MSK)**
Slot #06: DWC, Reflected	(DWC8300 / ISE, MSK)
Slot #07: DWC, Reflected	(DWC8300 / ISE, MSK)
Slot #08: DWC, Forward	(DWC8300 / ISE, MSK)
Slot #09: DWC, Forward	(DWC8300 / ISE, MSK)
Slot #10: DWC, Probe	(DWC8300 / ISE, MSK)
Slot #11: DWC, Probe	(DWC8300 / ISE, MSK)
Slot #12: LO-Generation	(Instrumentation Technology)

uTCA LLRF hardware platform

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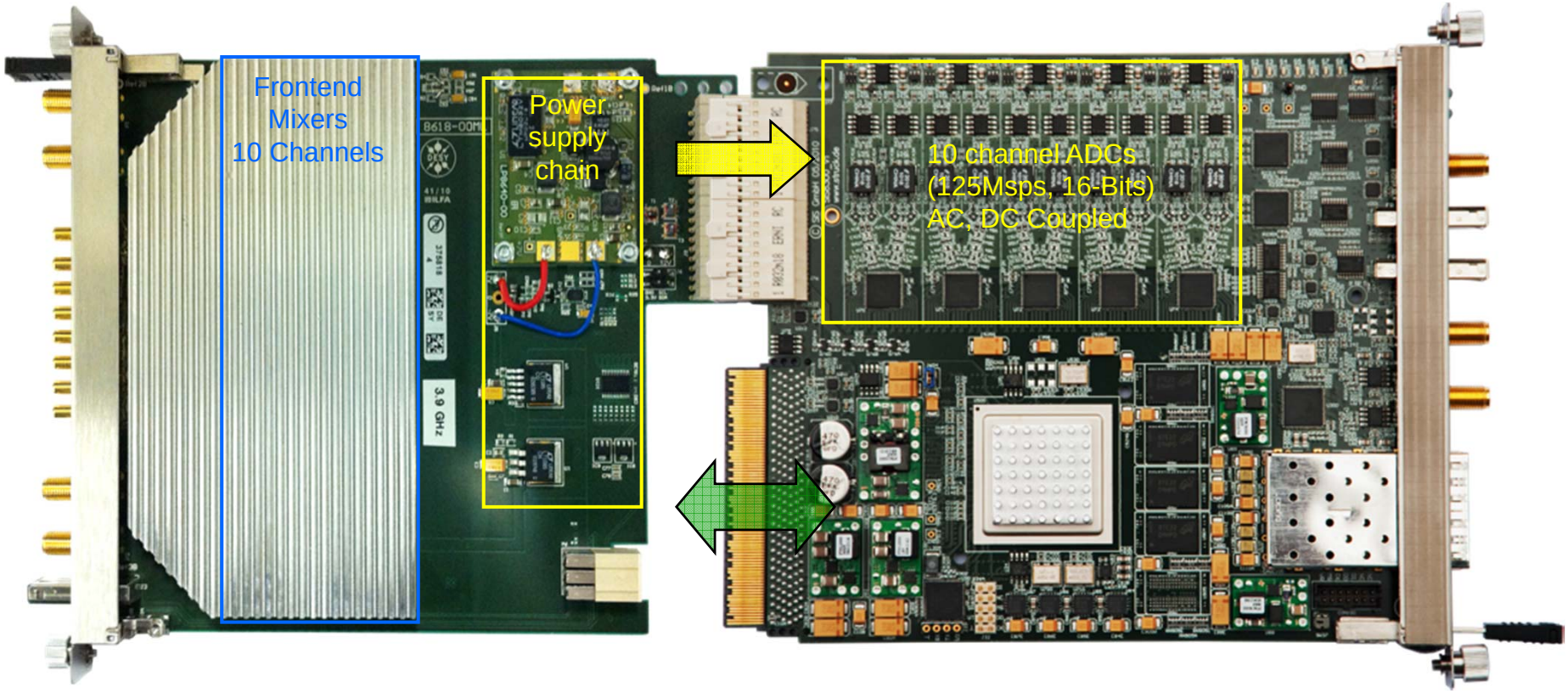
10-channel Down-Converter

Digitizer, Partial Vector Sum

struck innovative systeme



- 10 channel field detection
  (1.3GHz, 3.0GHz, 3.9GHz)

- 10 channel ADCs (125Msps, 16-Bits)
- FPGA partial cavity vector sum
- Low latency links via uTCA-backplane

uTCA LLRF hardware platform

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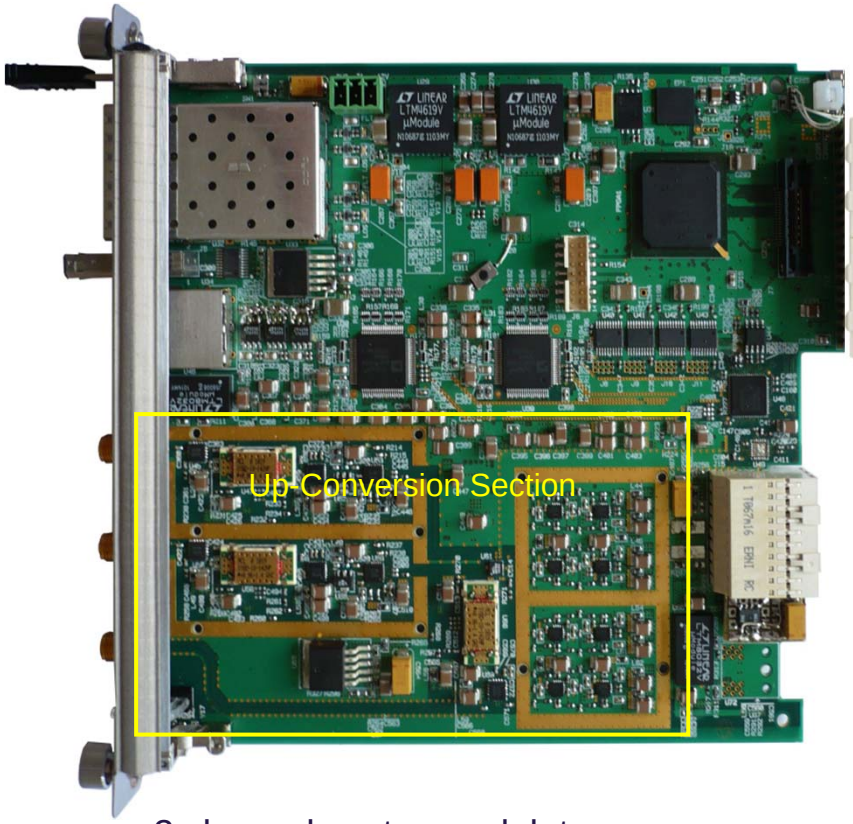
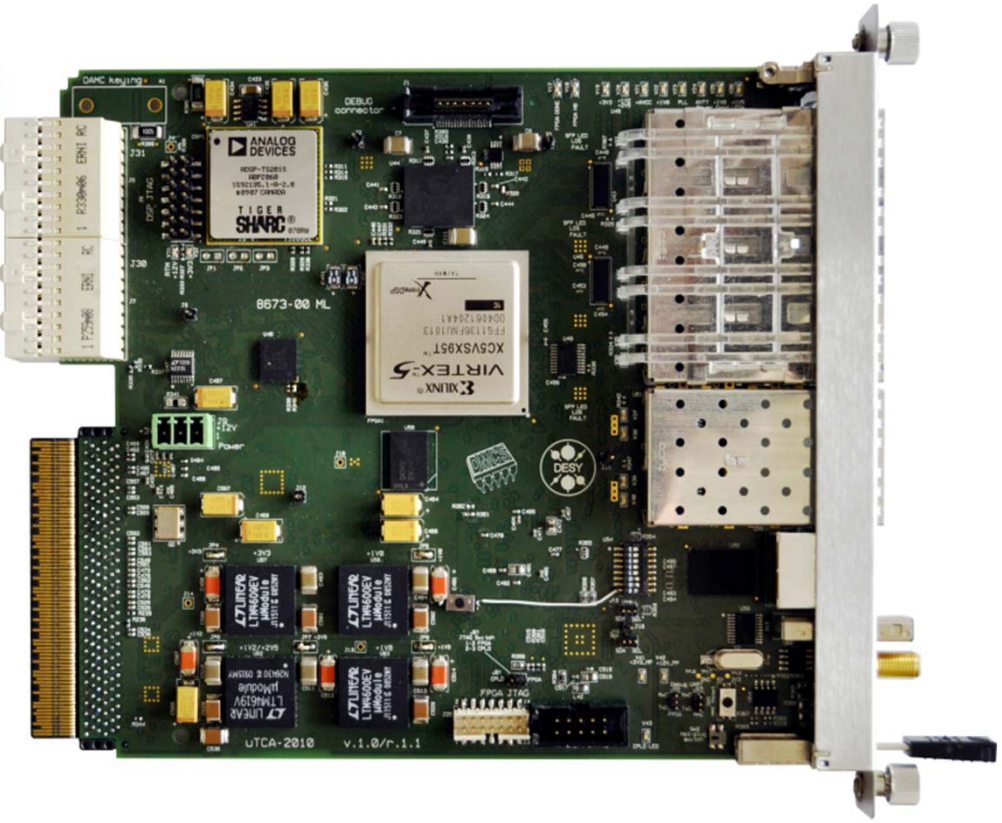
Klystron Driver



- 2 channel vector modulator
  (108MHz, 216MHz, 1.3GHz…3.9GHz)
- 16-bit DAC

LLRF Controller



- LLRF Controller, 6 Fiber-Ports, 2 GB-Links
- FPGA(V5), DSP

Status 2011: FLASH injector prototype system

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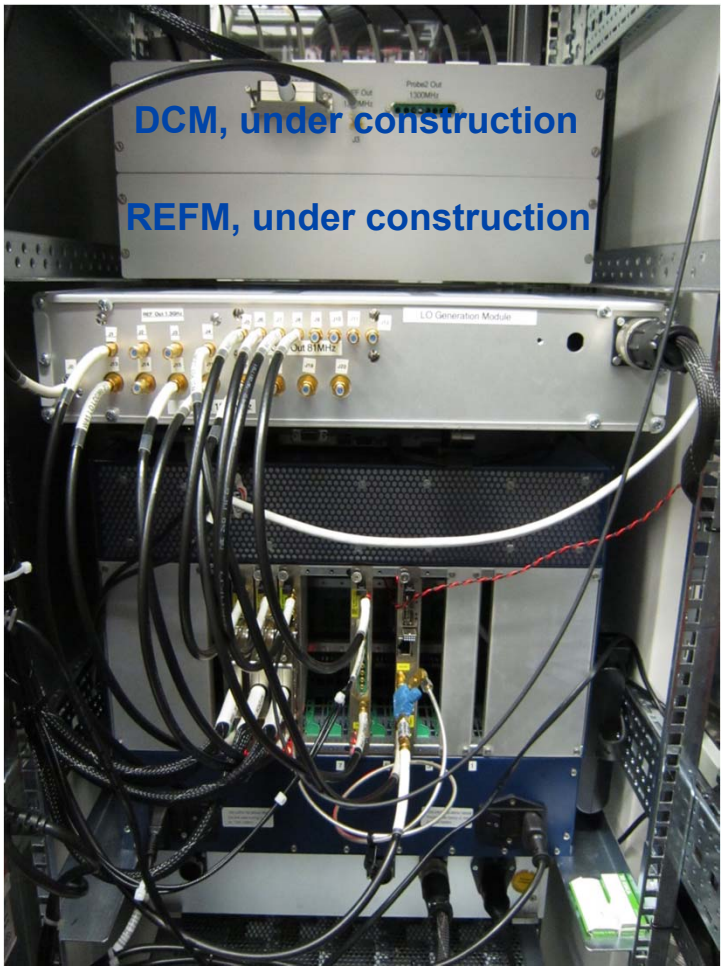
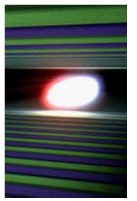
uTCA Prototype Front view

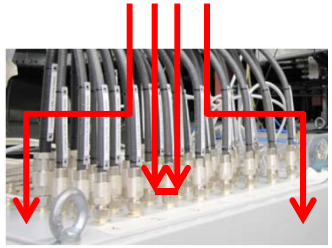
uTCA Prototype Rear view

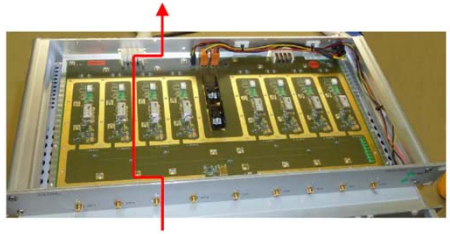


Signal integrity : Grounding concepts

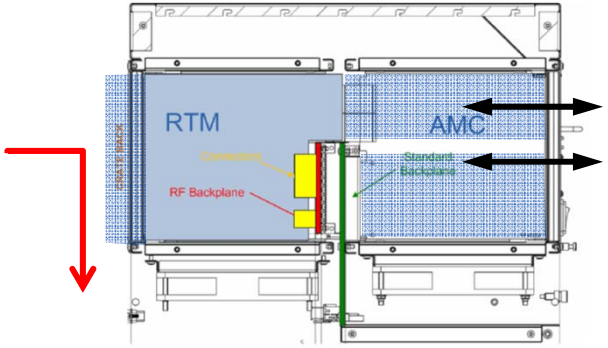


- **Bypassing … external distortions or grounding distortions :**

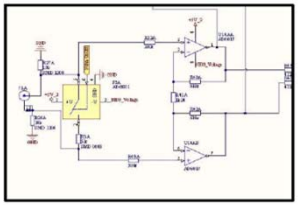




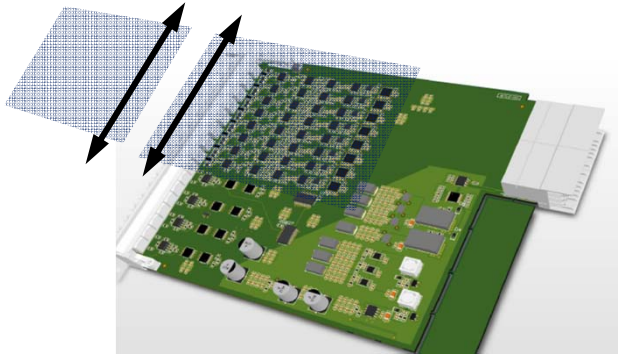
- **Shared GND via ZONE3-connector for AMC – RTM – AC coupled applications :**
  - Single-ended RTM input signals
  - Analog differential signal transport over ZONE3
  - Bypassing distortions into the chassis (controlled - TBD)
  - Controll GND backcurrents



- **GND decoupling using diff. Inputs for RTM – DC-coupled applications :**
  - Digital signal transport over ZONE3



- Pseudo differential input



. . . or combinations . . .

Signal integrity : Zone3 IF-Performance

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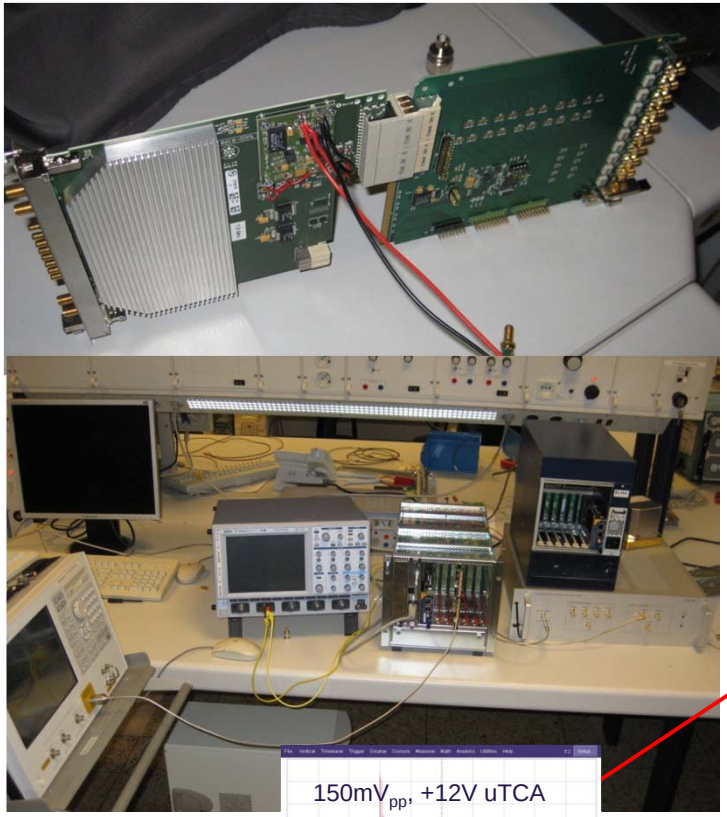
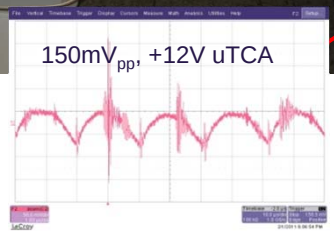
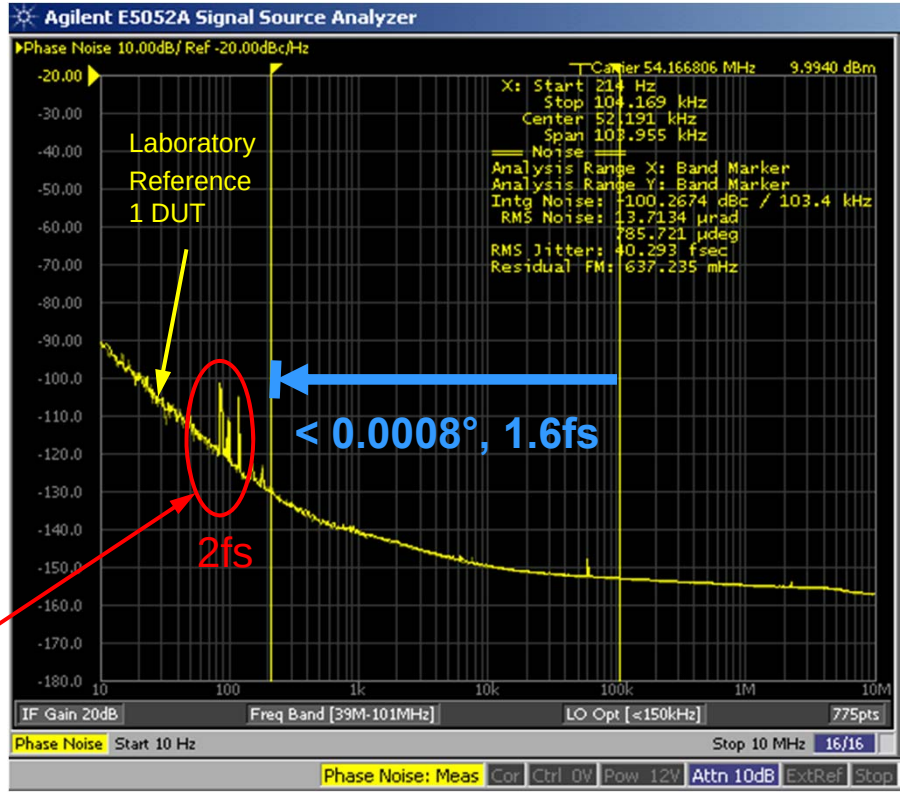
- **Short-term stability in a uTCA crate (laboratory)**







→ XFEL field detection requirement of the receivers short-term stability is fulfilled.

Signal integrity: Single channel performance

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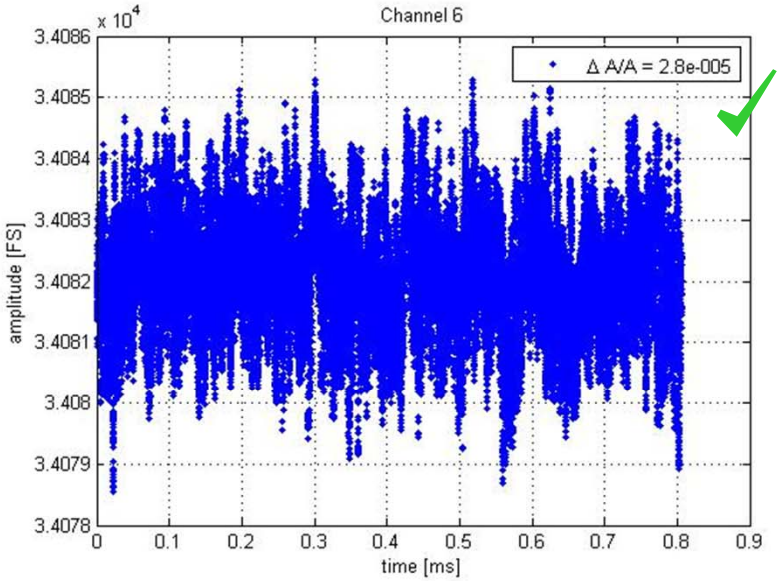
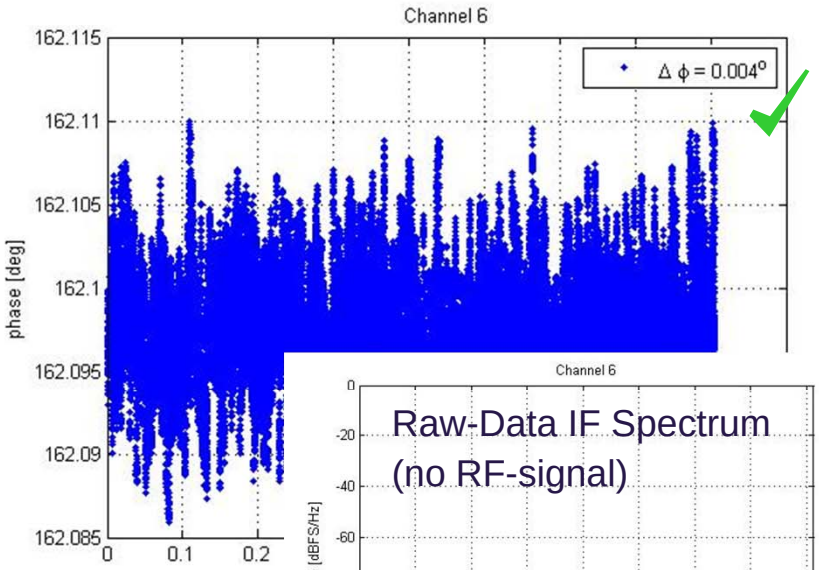
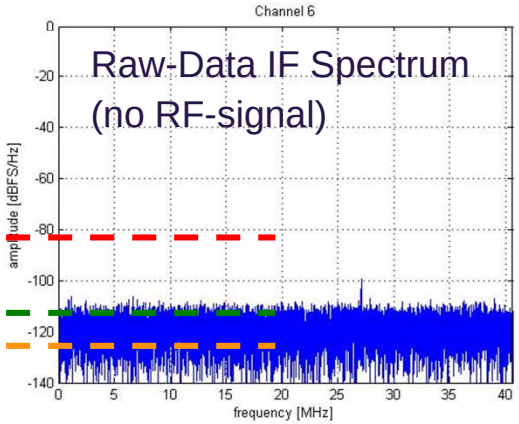
Short-term stability in a uTCA crate (laboratory) :







Testconfguration:

- DWC8300 R1.0, SIS8300_V2, MCH, CPU, uTCA crate
- DRO 1.3GHz (PSI), 1354 MHz LO, 54MHz IF, 81MHz SR
- LO-Generation Module (19“, FL, PM version)
- Offline Matlab non-iq analysis (N=65K), 1MHz Bandwidth

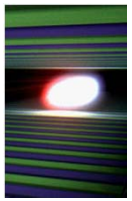
Power-Entry-Modules: < 110dB spurious free
Poor Power Supplies : < 80dB SFDR
VS-Scaling : < 120dB SFDR

→ Single cavity resolution improved by a factor of 5 to dA/A=2.8E-5.

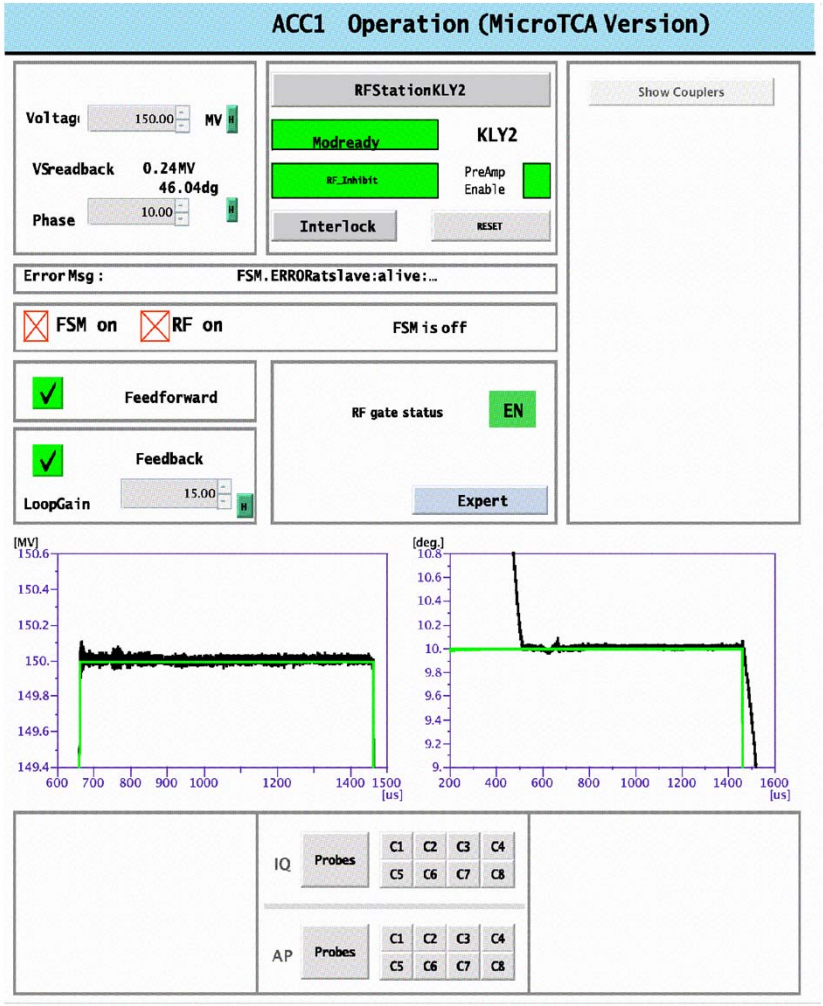
→ Signal integrity in uTCA crate achieved Eval board performance.

(using a Power-Entry-Module, Ericsson BMR911483)

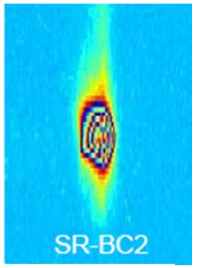
Beam operation using the uTCA-platform

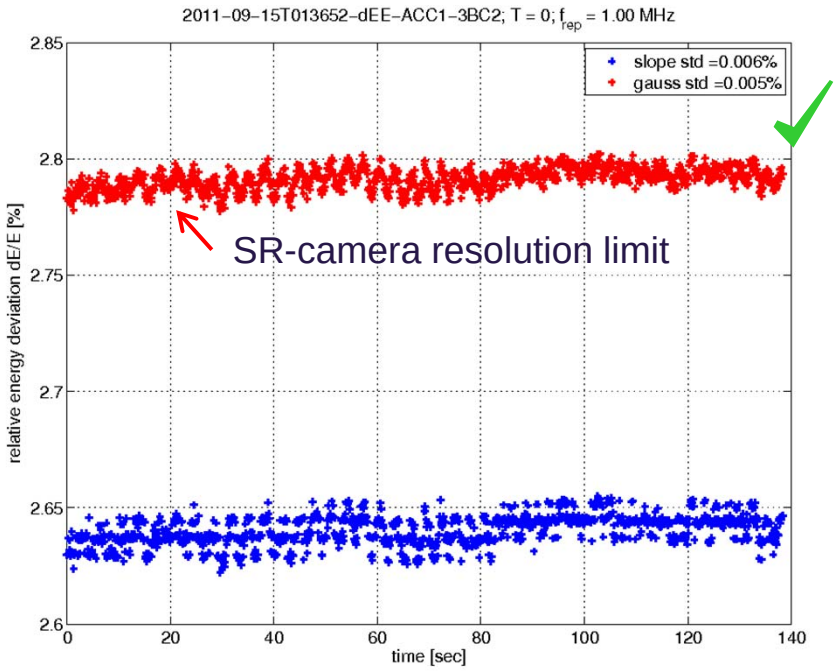


FLASH operation :



On-crest energy stability :





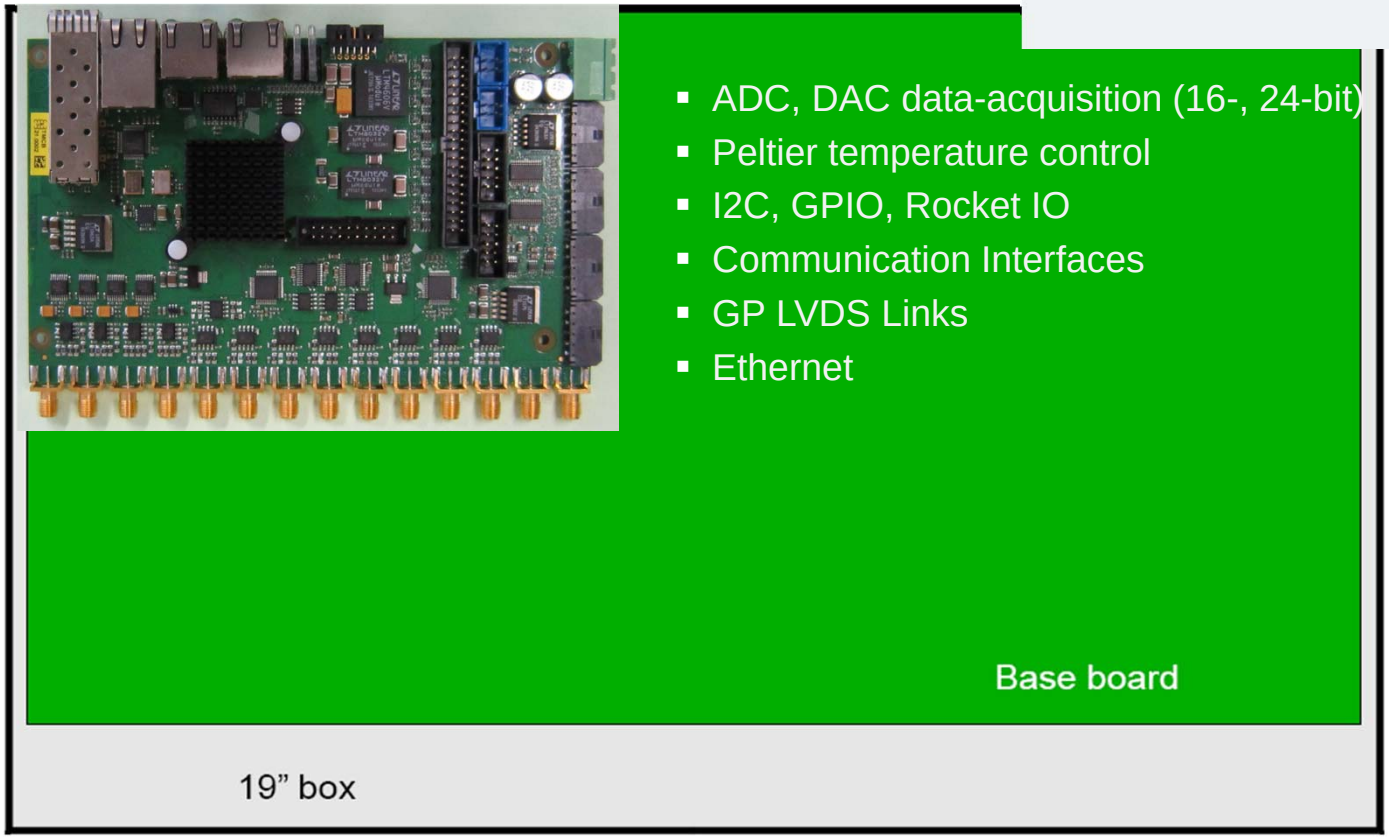
→ Energy stability dE/E=0.5E-4.

uTCA LLRF hardware platform

Temperature Control & Monitoring Board for 19“-modules

- Control module for all 19“ modules
- Common hardware, software and firmware

Instrumentation Technologies

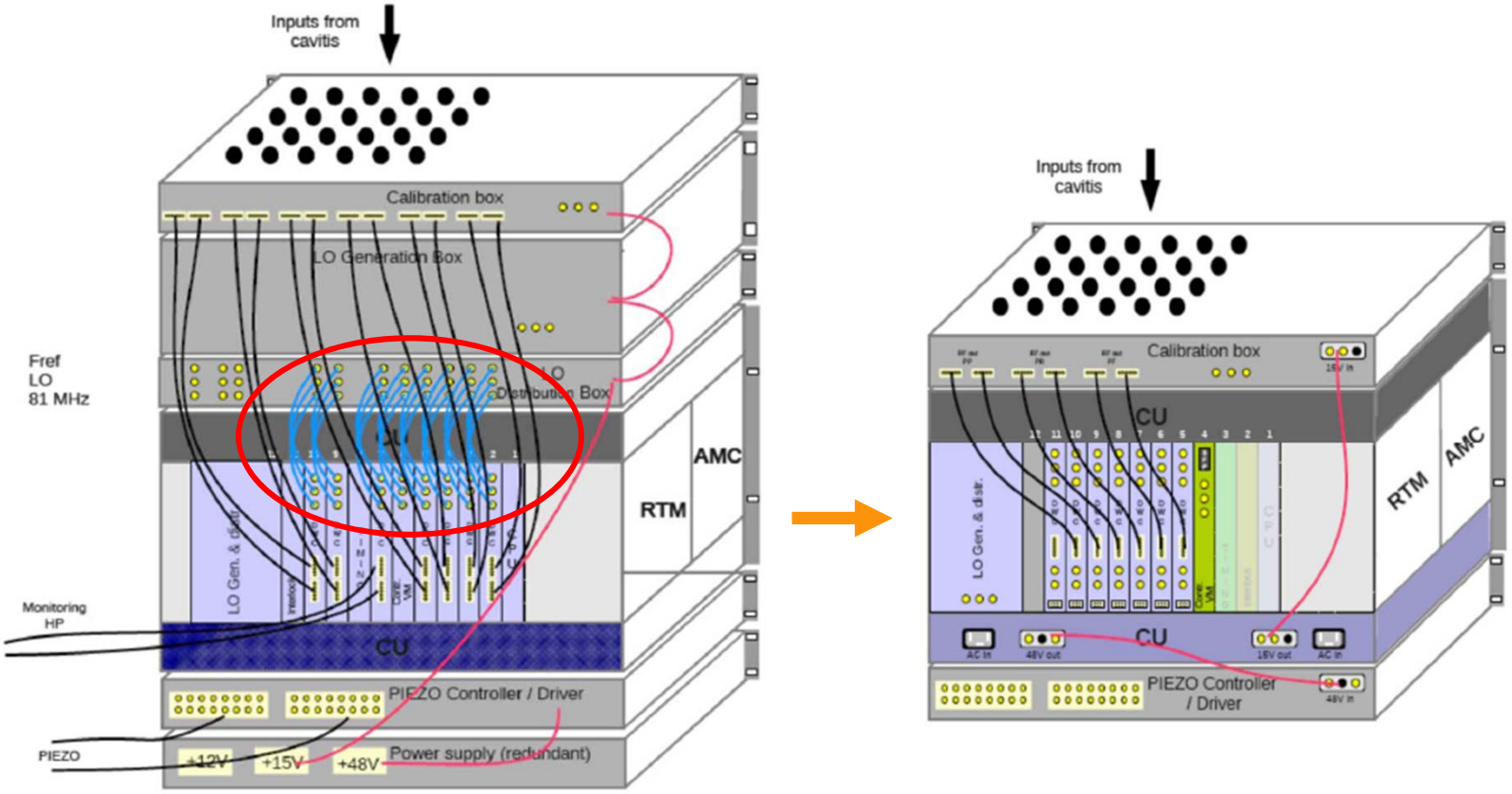


→ Fruitful and uncomplicated cooperation.

Signal integrity: Low jitter signal distribution

FIL

Introduction of an uTCA RTM-backplane



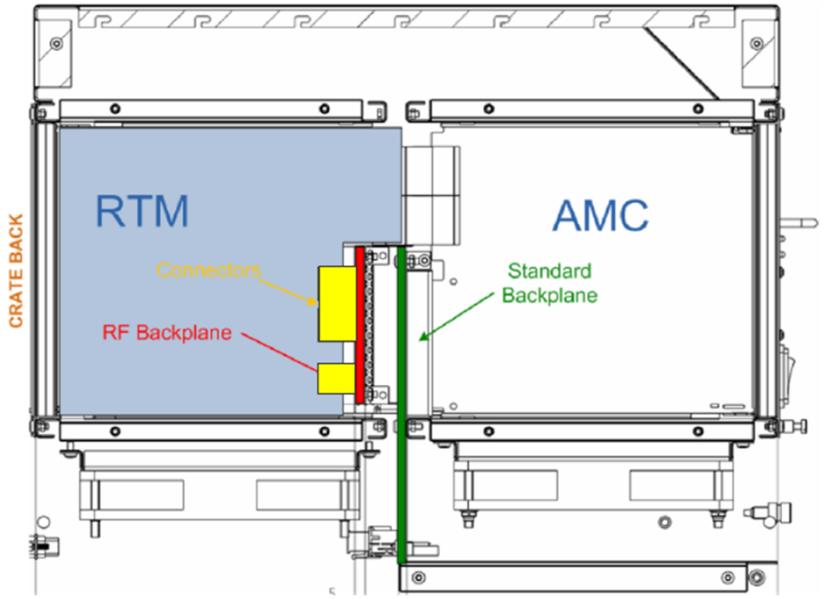
Complicated cable management → LLRF RTM backplane concept

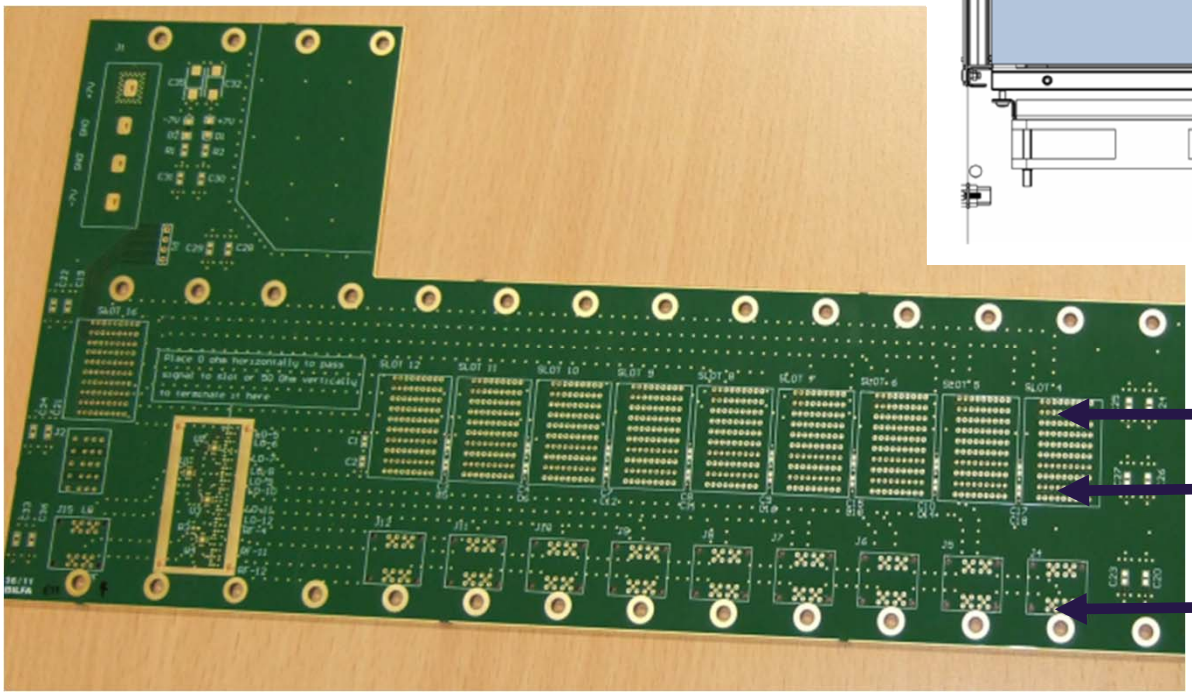
Signal integrity: Low jitter signal distribution

FIL

- **uRTM and uAMC LLRF backplanes**

. . . to be tested . . .





Low jitter clock distribution < 200fs (e.g. ADC-Clocks)

Redundant linear power supplies (e.g. +7V, -7V)

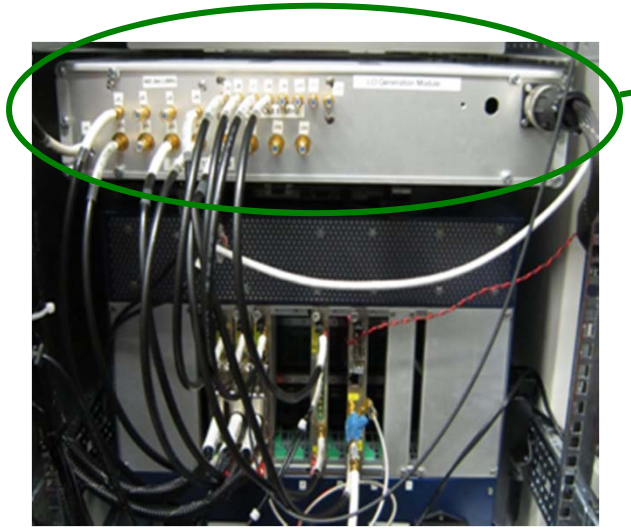
Low jitter RF-signals <10fs (e.g. LO-Distribution)

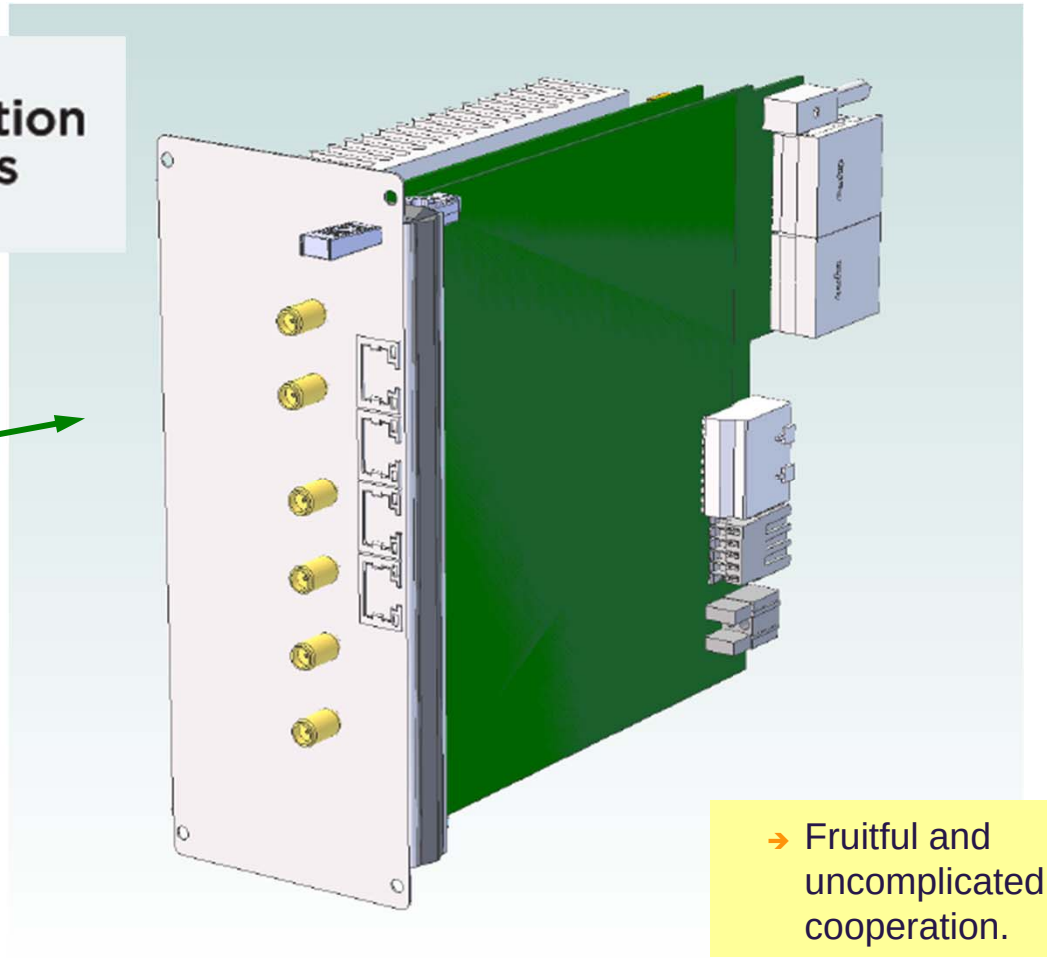
Signal integrity: Low jitter signal distribution

FIL

- **uLOG : RTM low jitter signal generation**

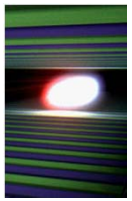
Instrumentation Technologies





➔ Fruitful and uncomplicated cooperation.

Timeline - Deadlines

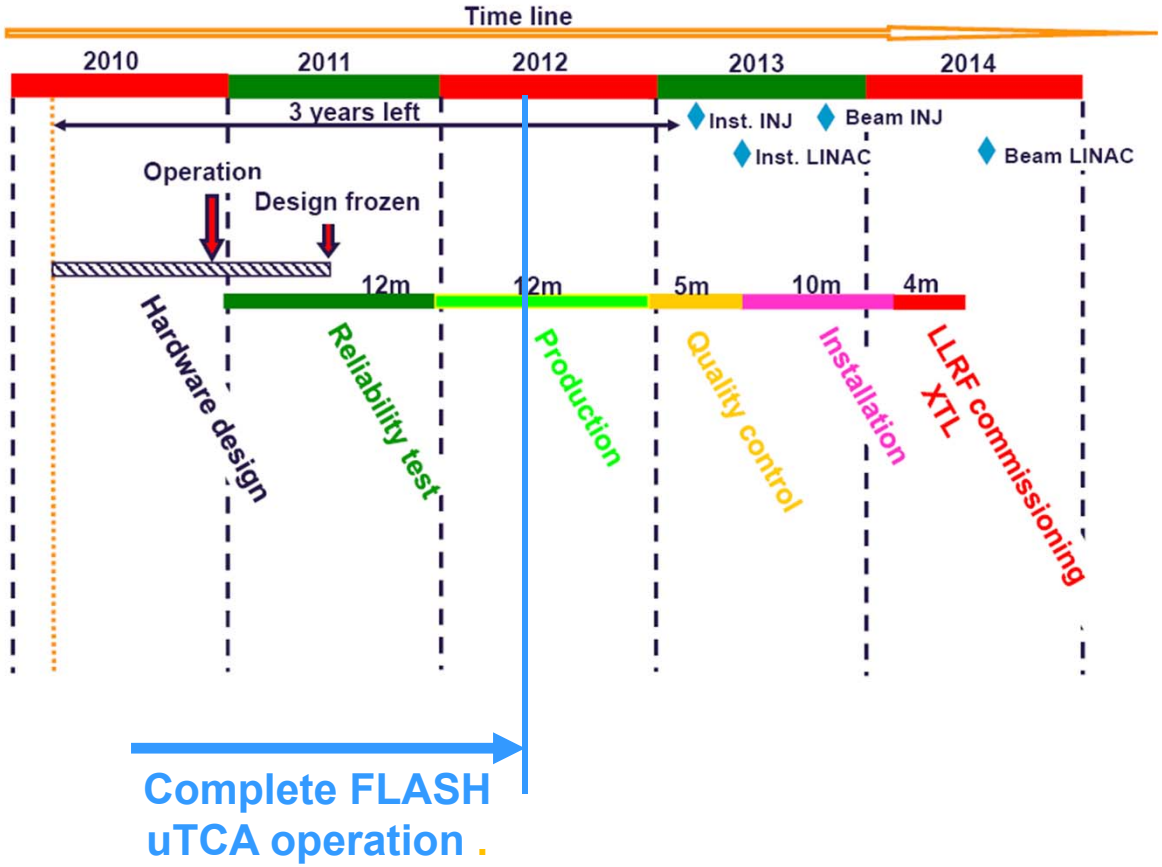


DESY-BAHRENFELD

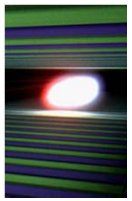
OSDORFER BORN

SCHENEFELD

XFEL LLRF uTCA Timescale



Summary of the XFEL LLRF Roadmap



- A LLRF concept based on uTCA - platform is presented.
- Recources are shared within DESY, collaborators and industry.
- First beam energy stability measurements using the uTCA platform fullfil the XFEL requirements.
- Low distortion power supplies are needed.
- A Crate, AMC, RTM module distortion classification is helpful.

Thanks for your attention!