A 512-channel FEE prototype based on the custom ASIC for MPGD

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Outline

1、Background and requirements

2、Design of the FEE

3、Test results

4、Conclusion

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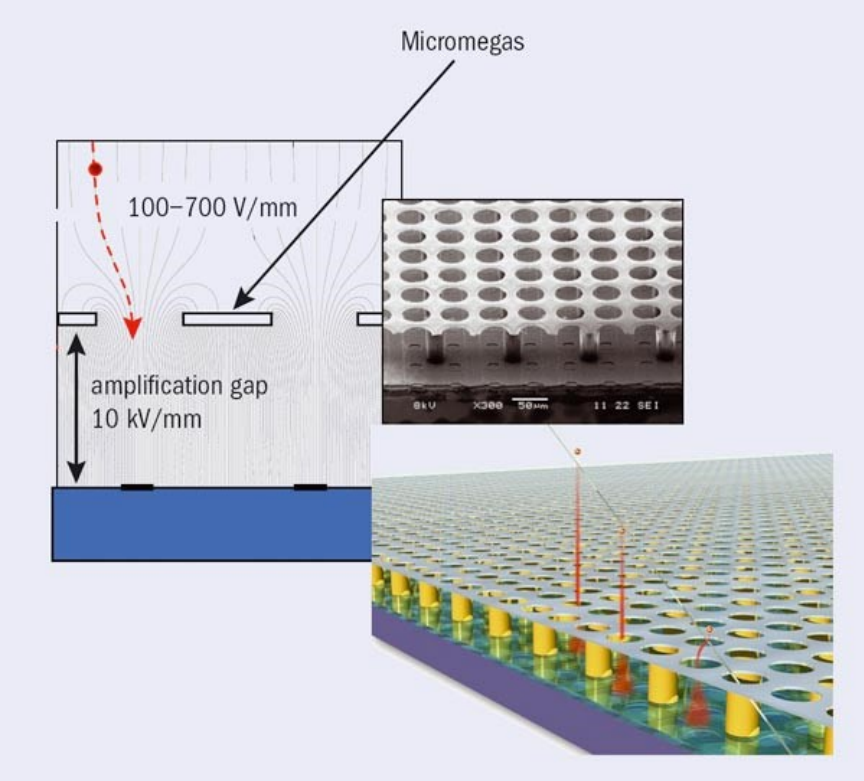
Micro-Pattern Gas Detector

Advantage:

- High counting rate capability
- Good spatial resolution
- Good time resolution
- Large area production
- Low cost
- Robust
- ……

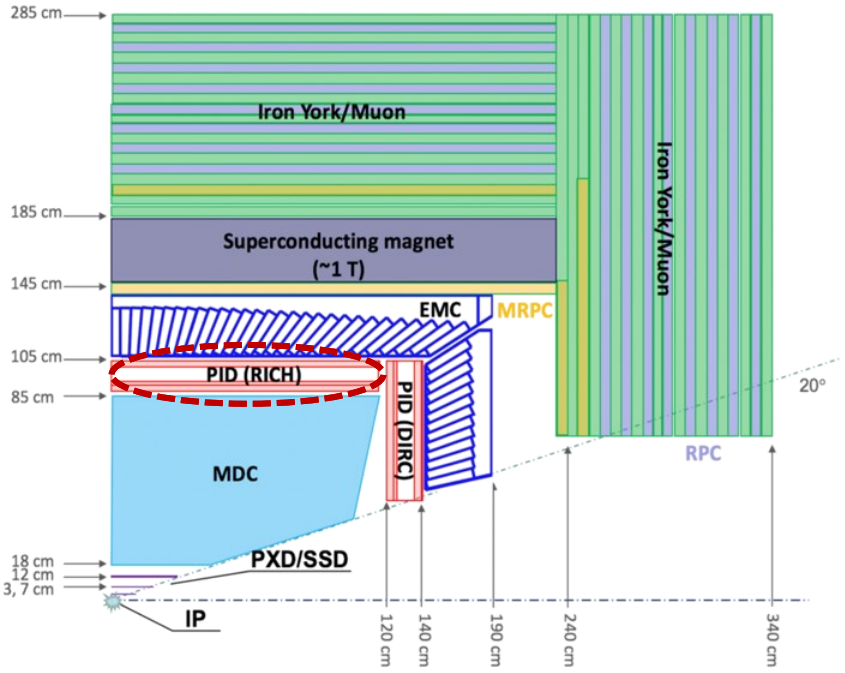


Schematic view of a kind of MPGD

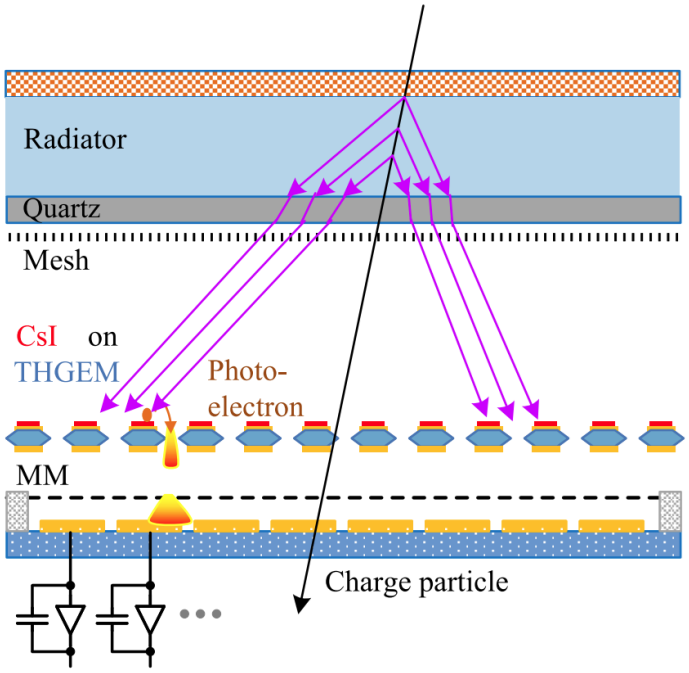
Wide use in physical science research

MPGD at STCF PIDB

- Super Tau-Charm Facility (STCF) is a electron-positron collider to be built in China with a peak luminosity up to 0.5×10^{35} cm^{-2} s^{-1}.
- Particle IDentification detector on Barrel (PIDB)
  - Ring Imaging Cherenkov Detector (RICH)
  - Hybrid amplification of THGEM-MicroMegas



Cross section of the STCF detector



Working principle of the prototype RICH detector

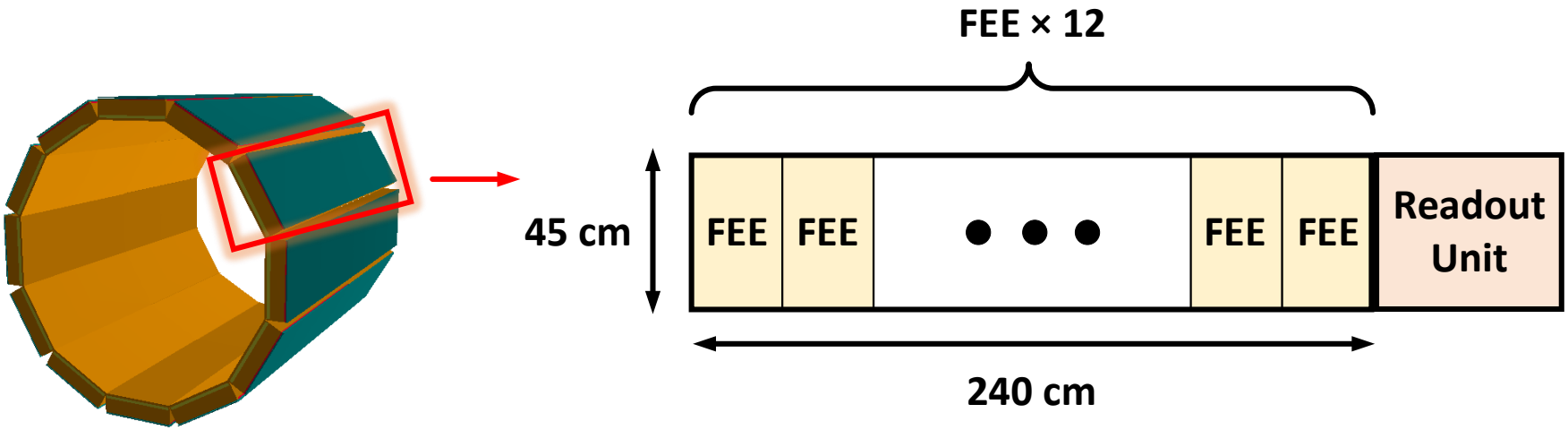
PIDB Readout Electronics

Challenges posed to readout electronics:

- High density
- Large number of channels
- High resolution
- Short dead time

Requirements for the readout electronics

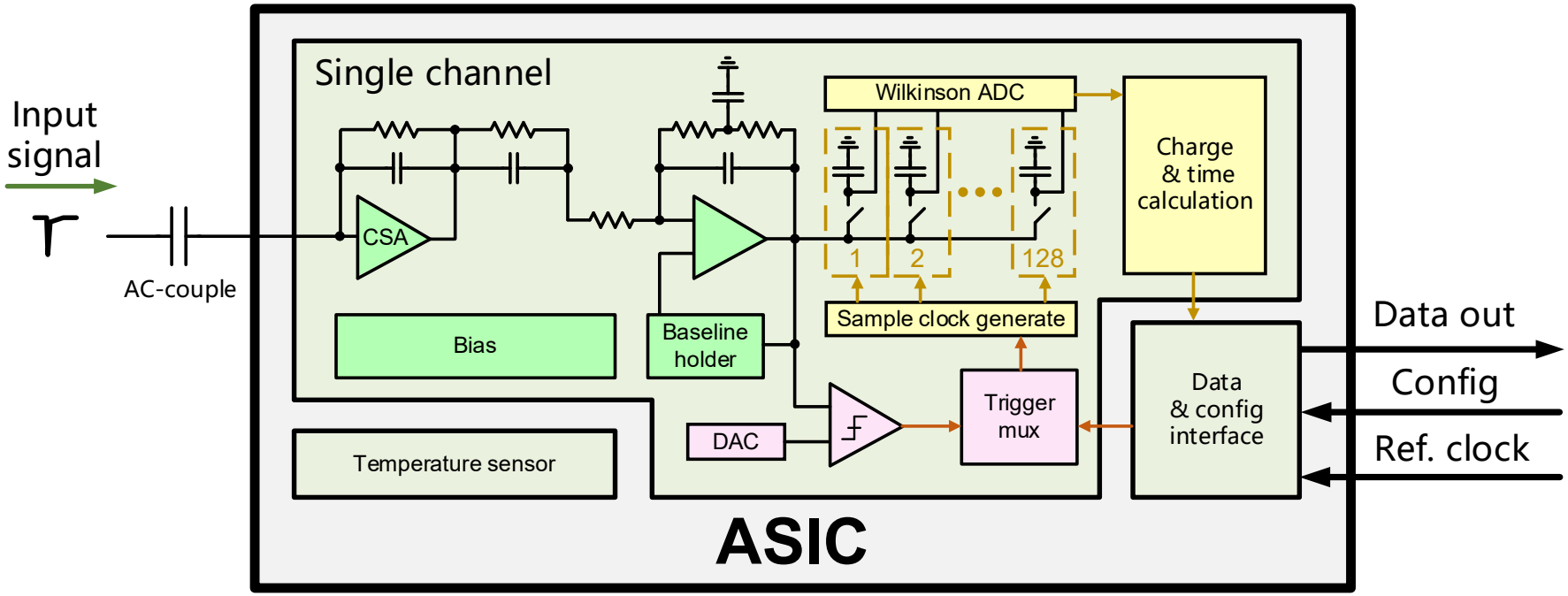
	Requirement
Charge measurement range	48 fC
Equivalent noise charge (ENC)	0.5 fC @ 20 pF C_{in}
Time resolution	≤ 1 ns @ 16 fC @ 20 pF C_{in}
Total redout channels	~ 518,400
Dead time	< 66 μs/channel



Conceptual design of the RICH PIDB readout electronics

Front-end ASIC Prototype

- The prototype ASIC integrates 32 channels, including analog processing circuits, analog-to-digital conversion (ADC) circuits, and charge & time calculation circuit.
- Compatible with both external trigger mode and triggerless mode.
- All outputs are digital and can be sent directly to the FPGA.



Block diagram of the prototype ASIC

Front-end ASIC Prototype

- Output waveforms are sampled and digitized by 128 independent cells, the mismatch between cells results in different codes for the same input.
- This mismatch is a form of fixed pattern noise that can be corrected by the stop position information in the output data.

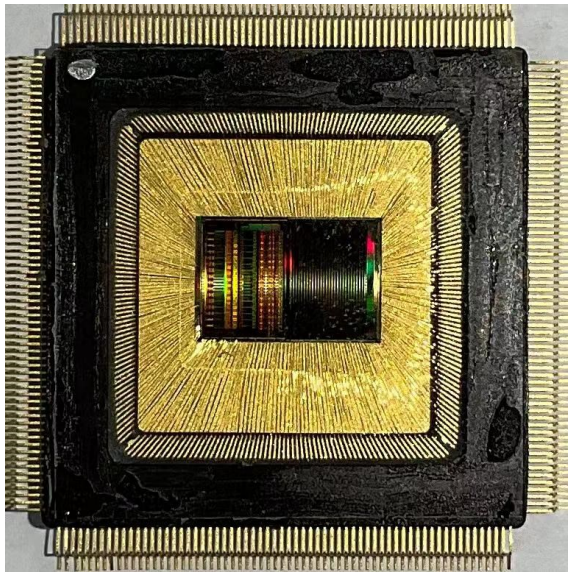
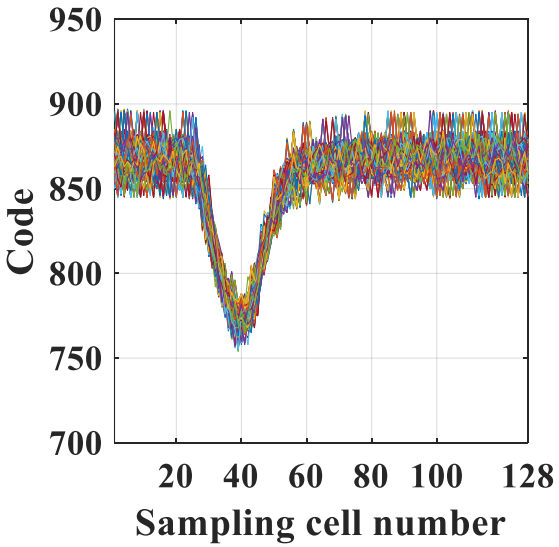
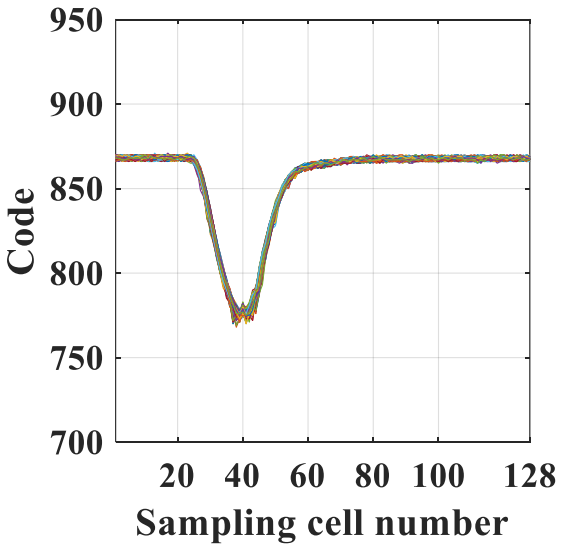


Photo of the ASIC



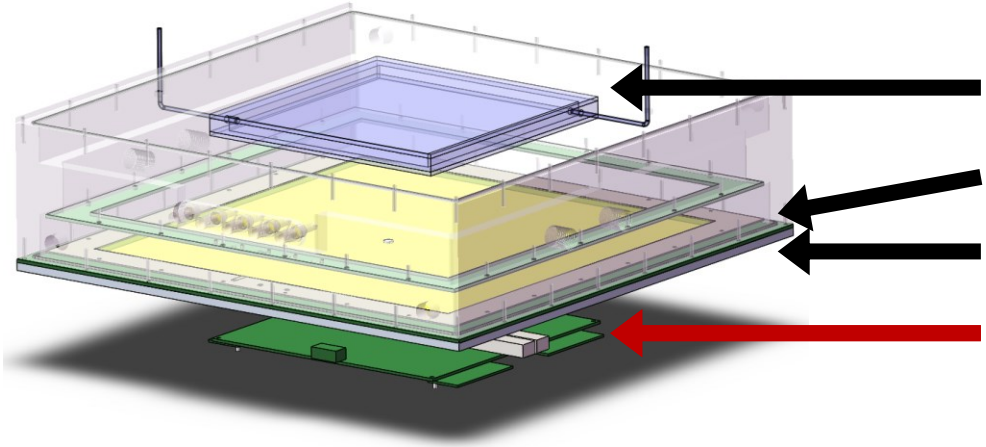
Pre DC calibration waveforms of 6 fC charge signals



Post DC calibration waveforms of 6 fC charge signals

PIDB Readout Electronics

- In the R&D phase, an engineering prototype is designed to study and optimize the performance of RICH.
- The effective area of the prototype is 32 cm × 32 cm.
- The readout electronics are located directly behind the detector to avoid a large number of long readout cables.



Liquid radiator

CsI on THGEM(32 cm×32 cm)

MicroMegas (5 mm×5 mm pad)

Readout electronics

Engineering prototype of the detector

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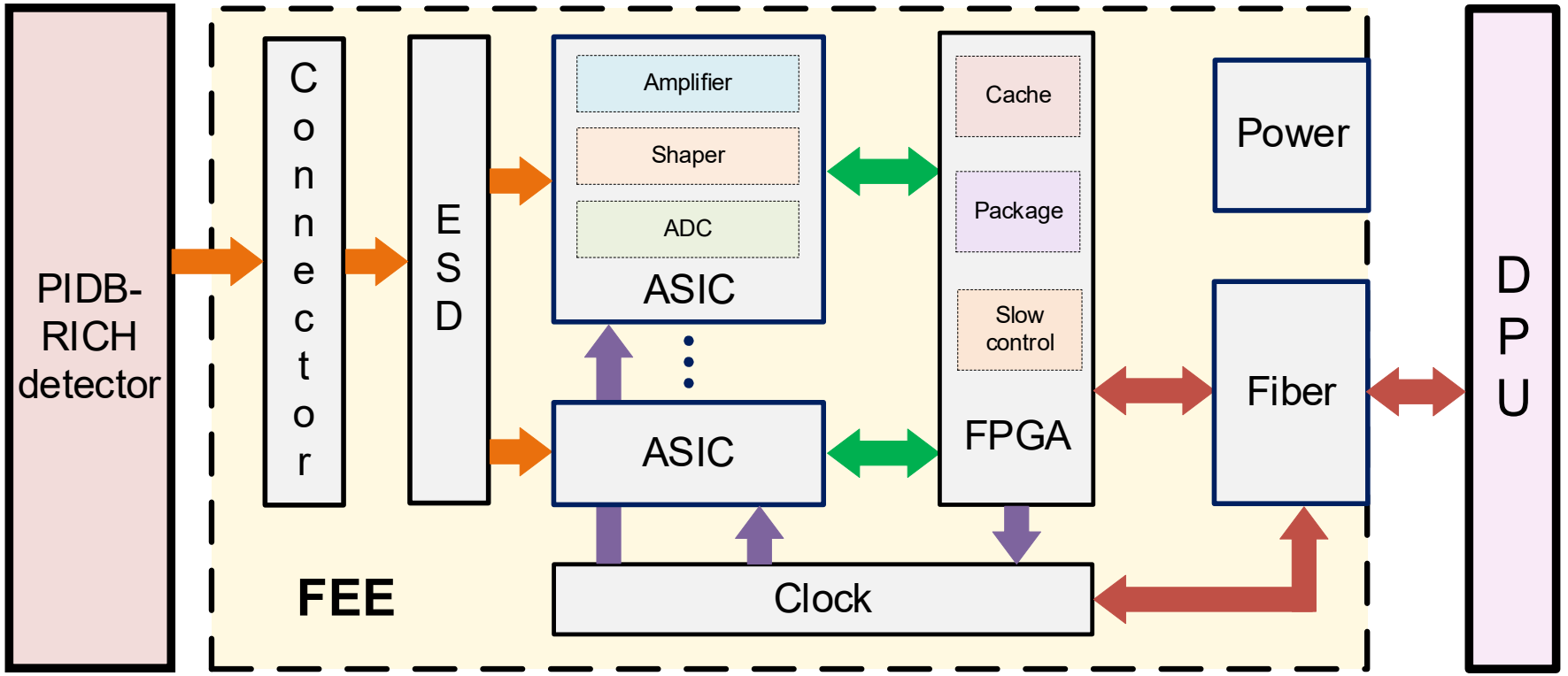
Hardware design of the FEE

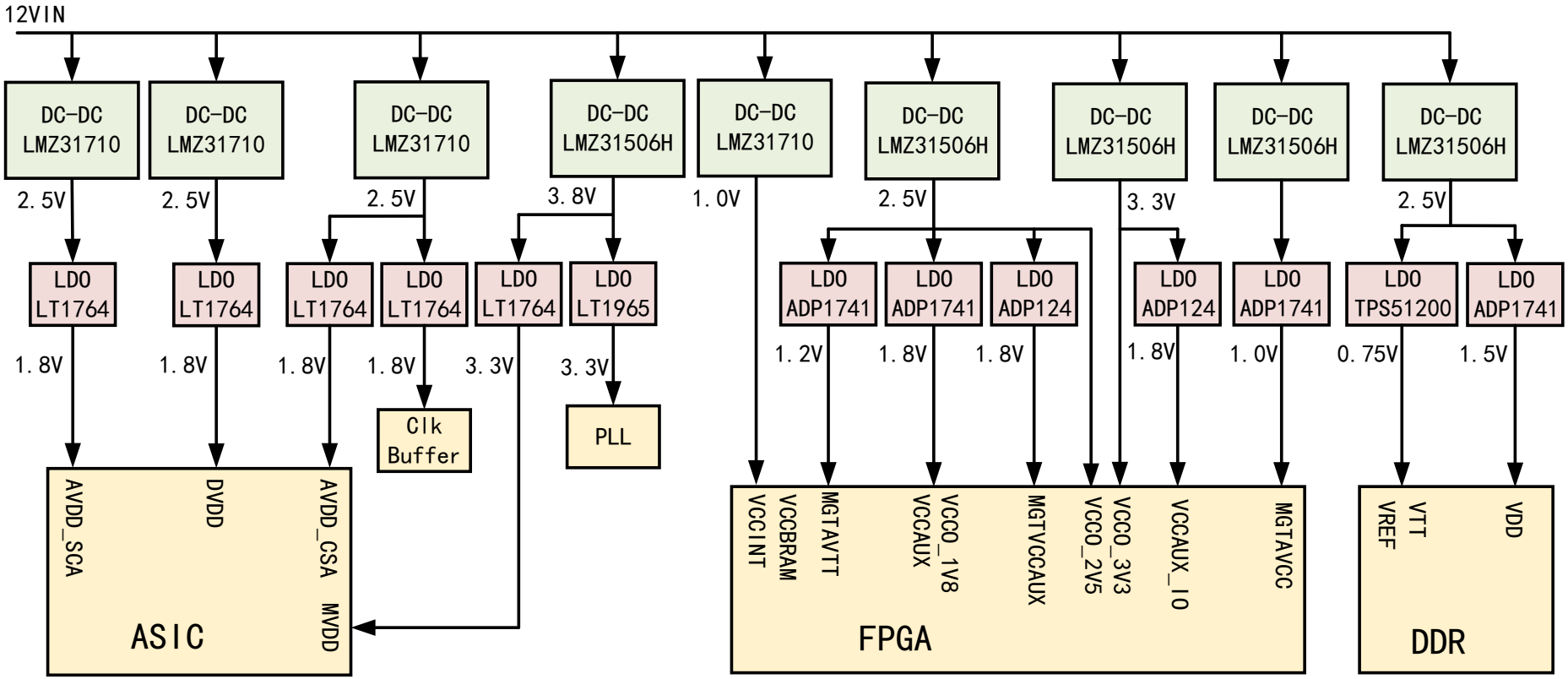
- Based on the 32-channel prototype ASIC, the FEE can be designed with high readout density.



Signal processing chain of the readout electronics

Power supply circuits

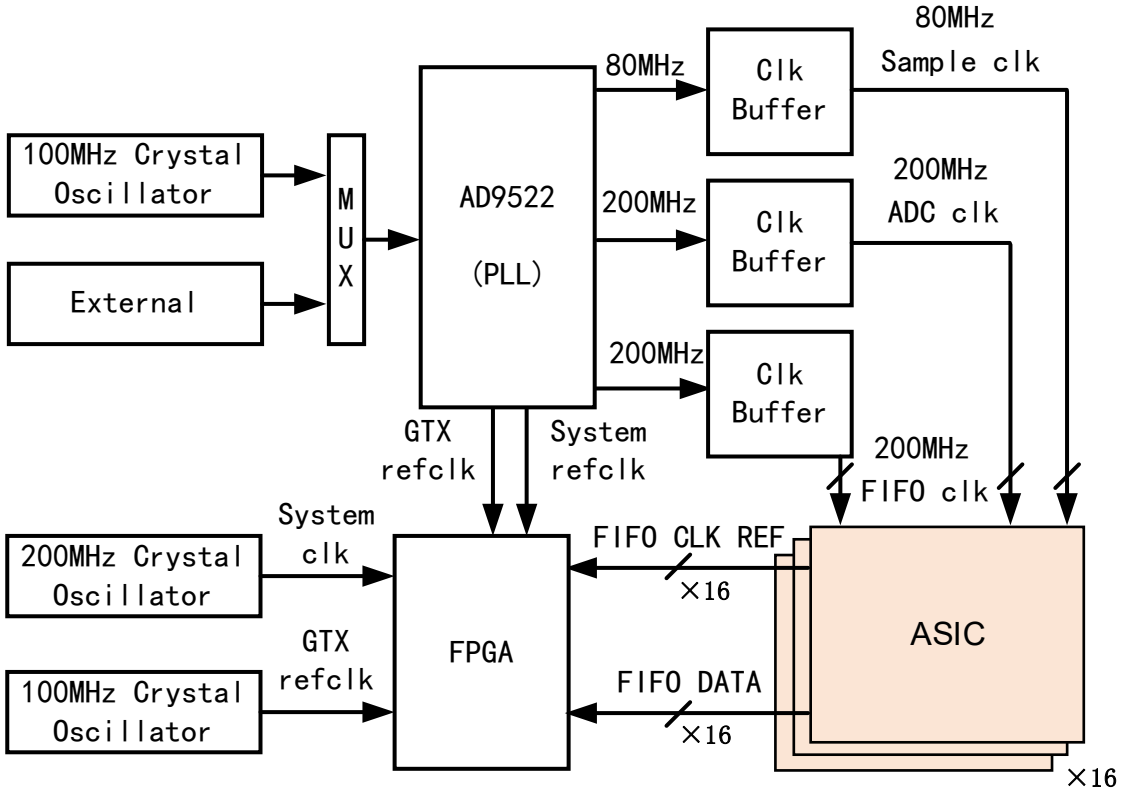
- The power supply circuit incorporates both DCDCs and LDOs to ensure high efficiency and low noise.



Block diagram of the power supply circuit

Clock circuits

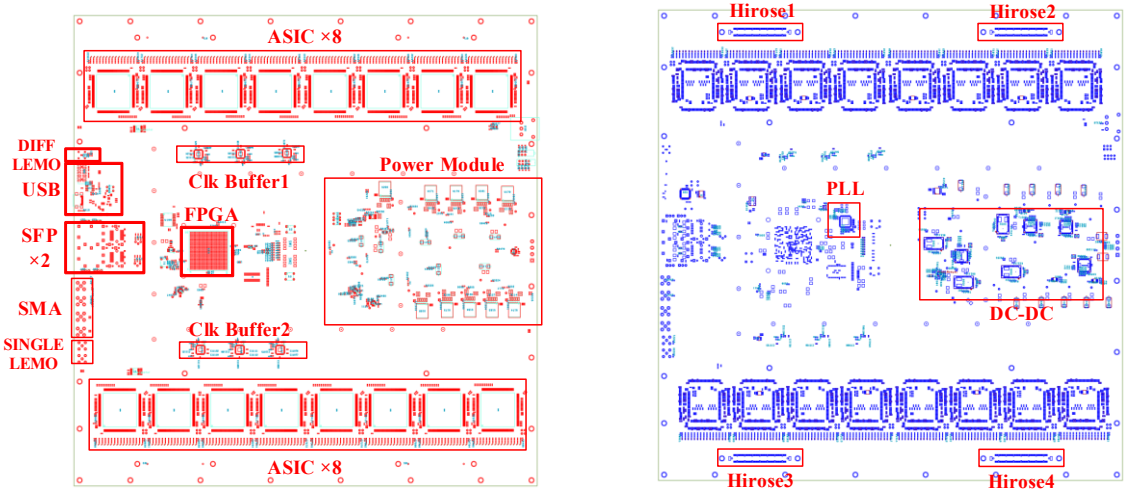
- 100MHz on-board Crystal Oscillator or LEMO interface can be selected as the reference clock.
- PLL generates low-jitter clocks for ASIC.



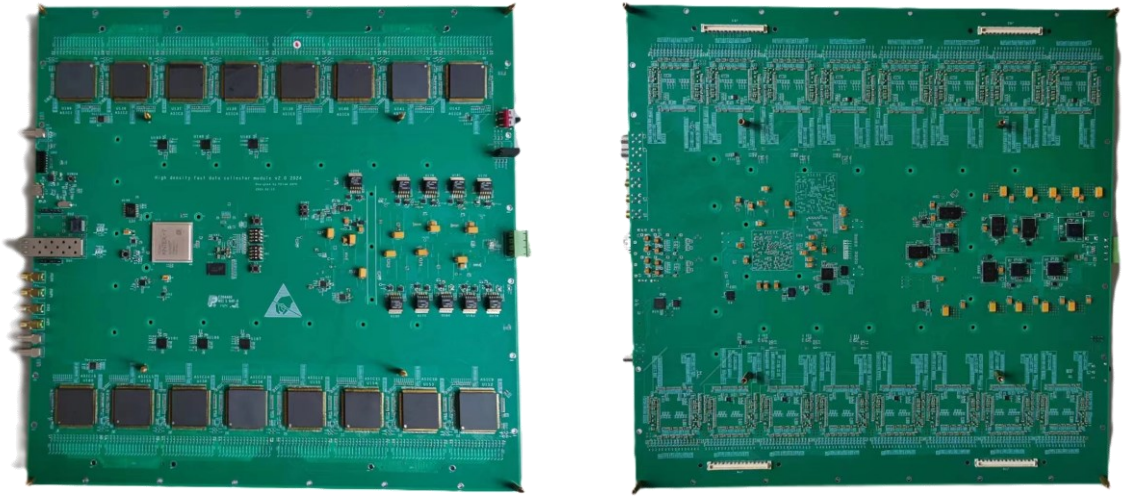
Block diagram of the clock circuit

Hardware Design of FEE

- The DC-DCs and PLLs are located on the rear panel to minimize the effect of EMI on noise performance.



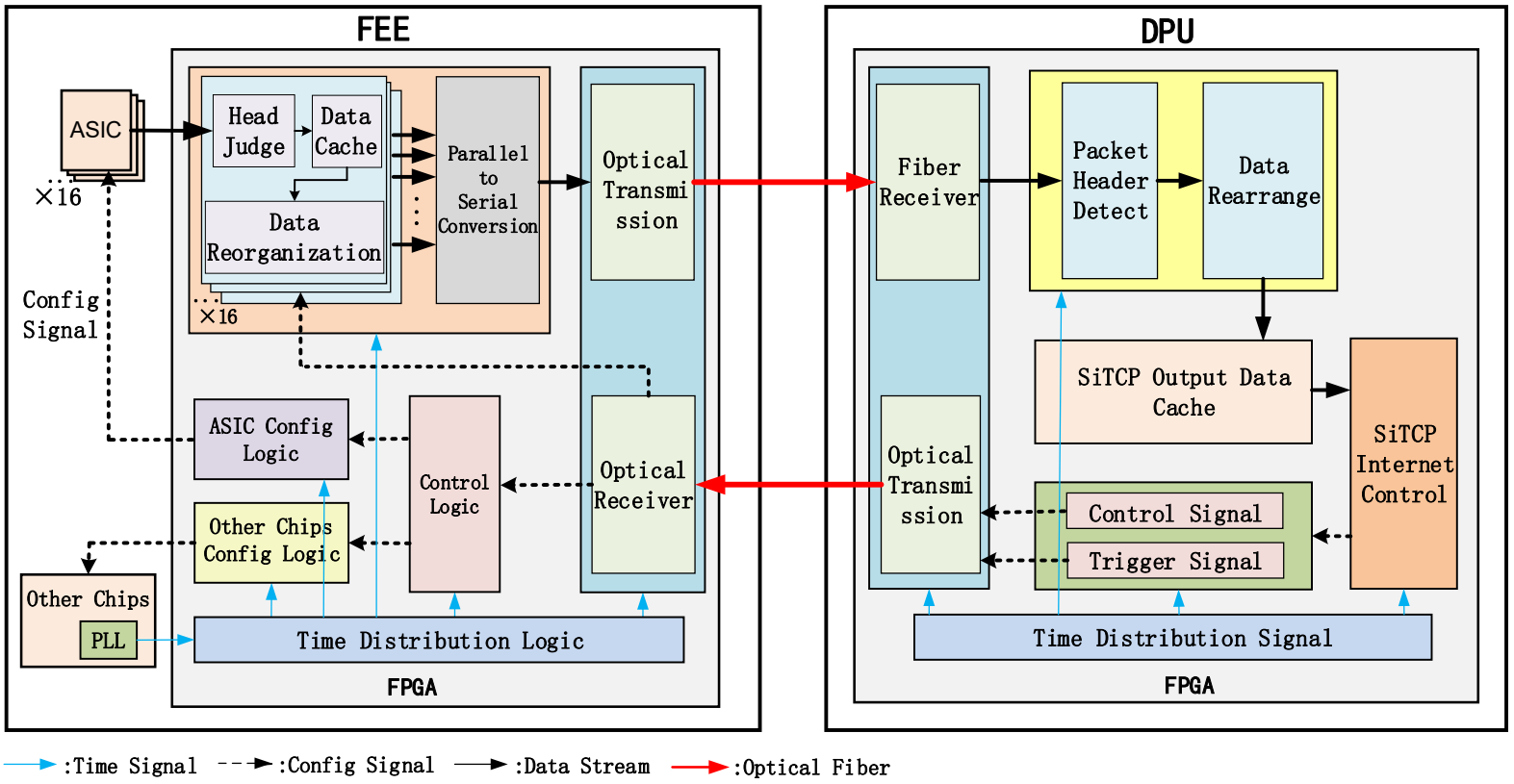
Layout of the FEE



Photograph of the FEE

Logic Design of the FEE

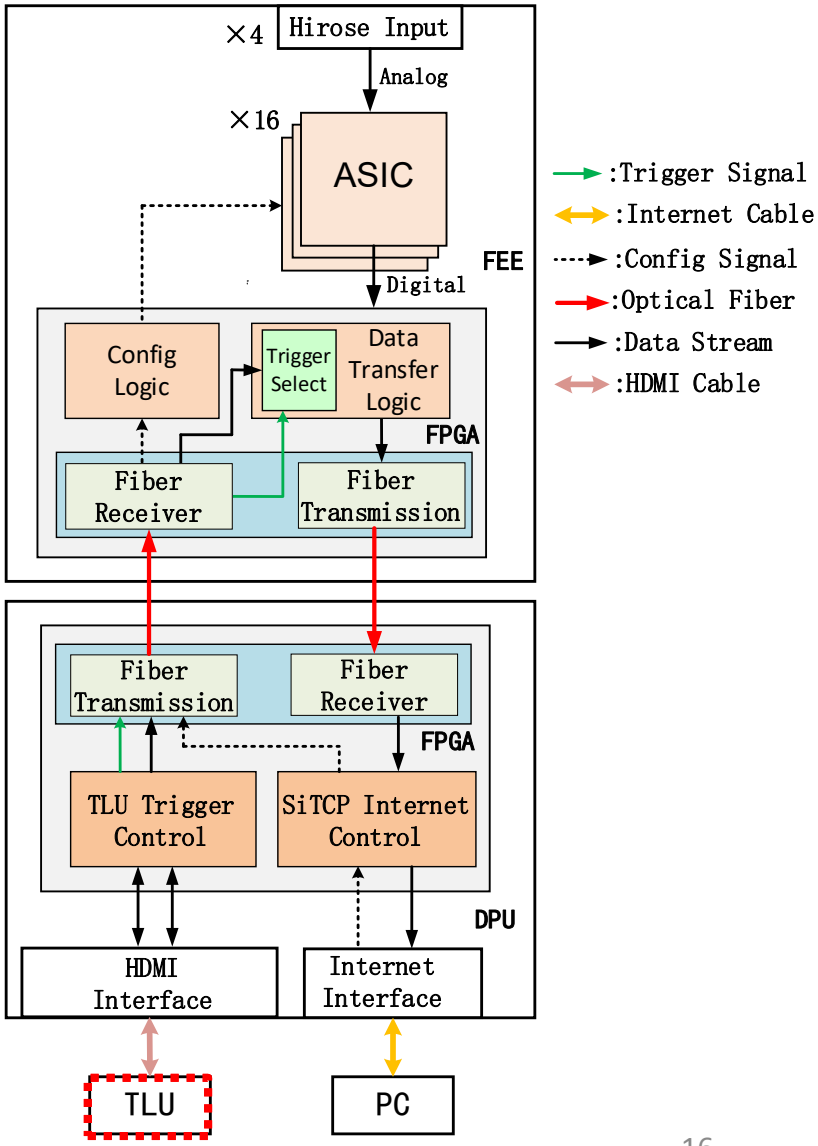
- DPU (Digital Process Unit) is a digital data processing board used to facilitate data exchange between FEE and PC.
- FEE transfers the data from the ASICs to the DPU and configures the ASICs according to the commands from the DPU.



Block diagram of data processing

Trigger match

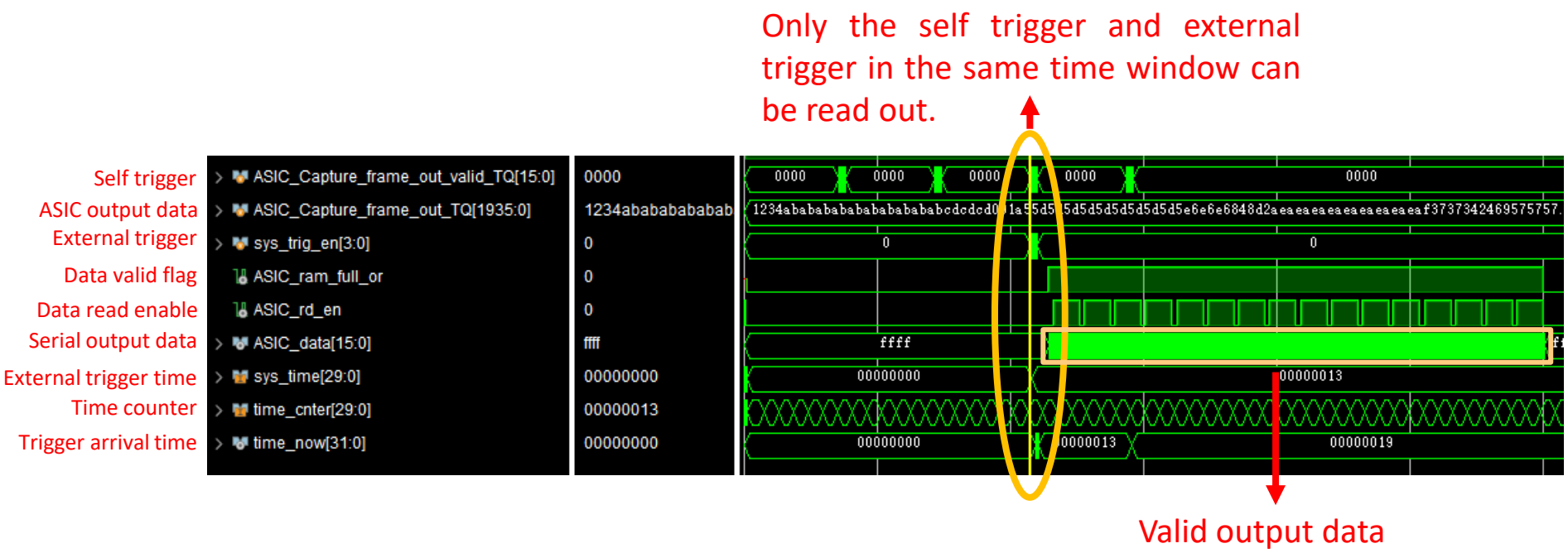
- Trigger matching logic is used to find valid data based on external trigger signals, while eliminating invalid hits.
- TLU (Trigger Logic Unit) is a circuit that generates a trigger signal and sends it to DPU via HDMI cable.
- DPU transmits trigger and control signal to FEE.



Block diagram of trigger match

Trigger match

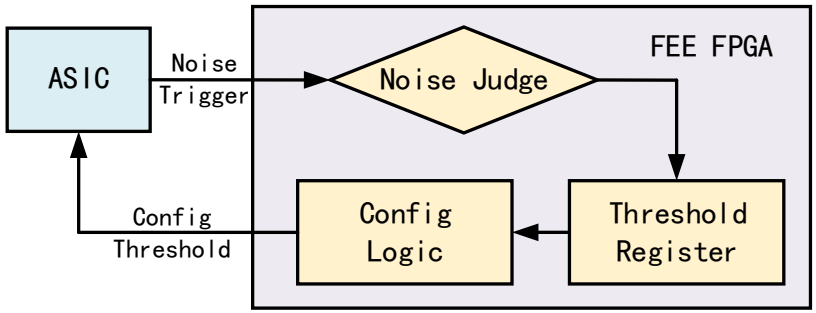
- Trigger match is processed by comparing the time information.
- When the FEE receives the external trigger signal, it filters the data storage with the time information of the trigger signal with a suitable time window.
- Time window can be adjusted according to the requirements.



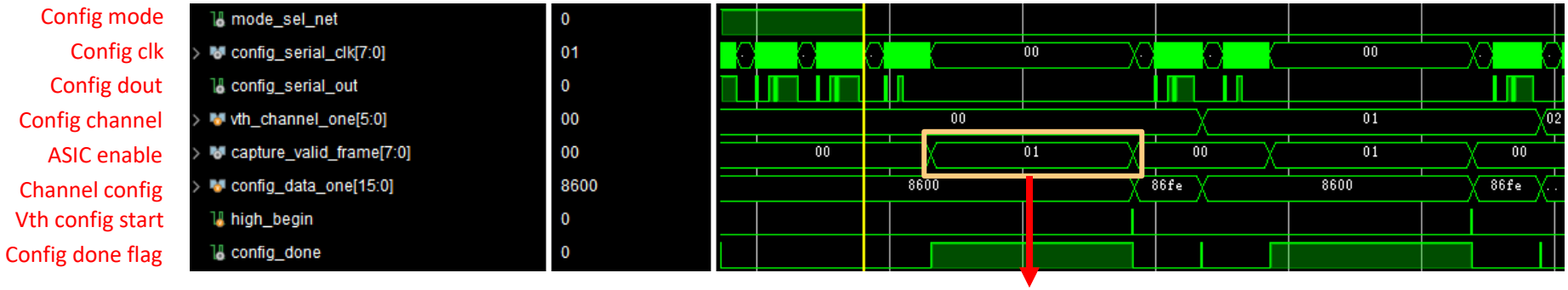
Timing diagram of the trigger match logic

Threshold automatic calibration

- Due to the inconsistencies in gain and noise between each channel, the optimal threshold for each channel can be different.
- This logic can automatically search and configure the optimal threshold for each channel.



Block diagram of the logic



Timing diagram of the logic

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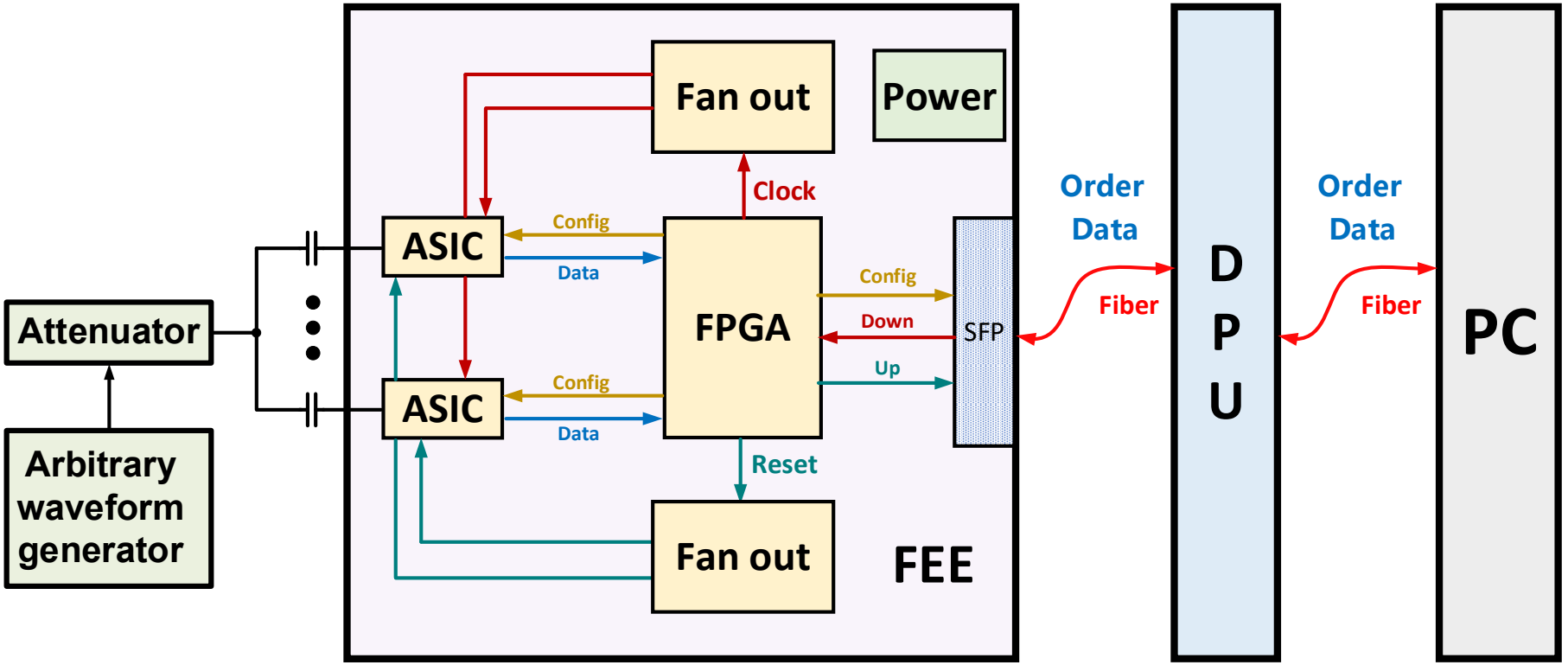
Test setup

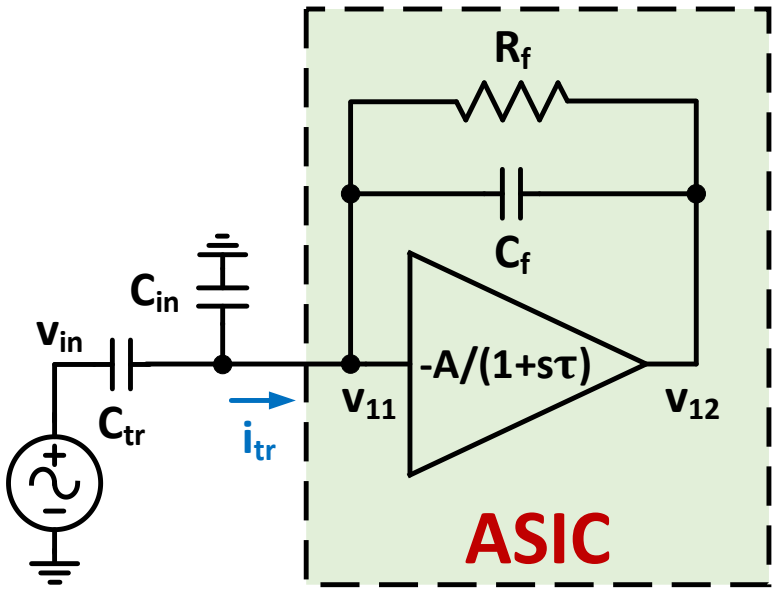
• After the FEE was fabricated and soldered, the evaluation in the laboratory was first conducted.



Block diagram of the test in laboratory

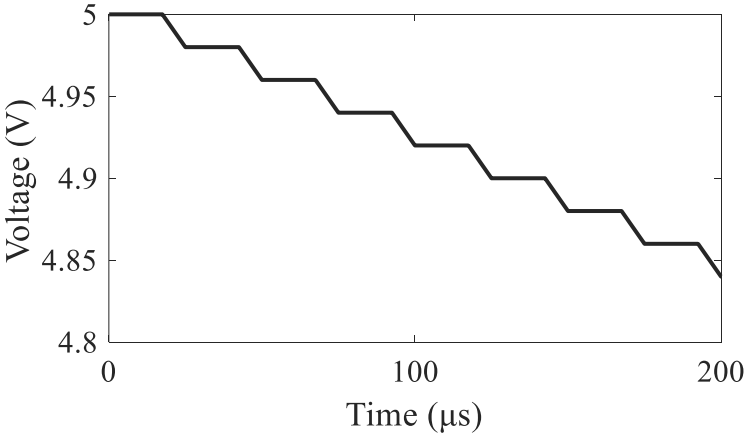
Test setup

- Considering that the AWG in the lab outputs voltage signal and the detector outputs current signal, a capacitor is used for voltage-to-current transfer.

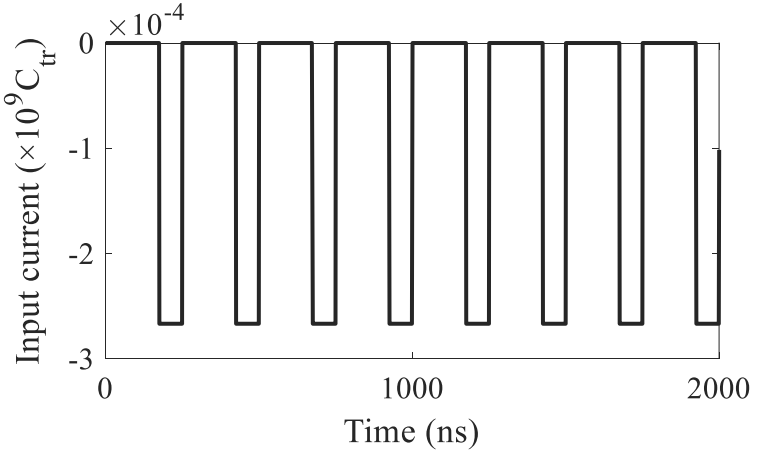


$$i_{tr} = v_{in} \cdot sC_{tr}$$

Schematic of the voltage-to-current transfer



Output voltage signal from AWG



Current signal after transfer

Test setup

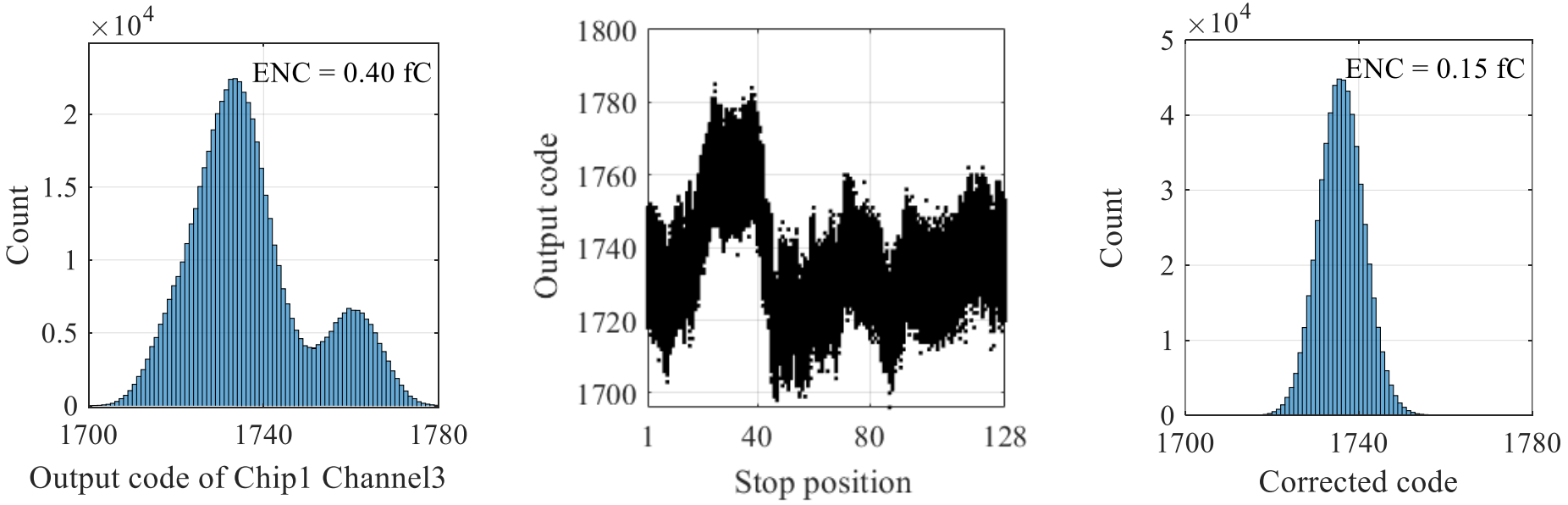
Photo of the test setup in laboratory

Correction for mismatch between cells

- The mismatch in output code for the same signal amplitude can be corrected by the stop position.

Association with the stop position

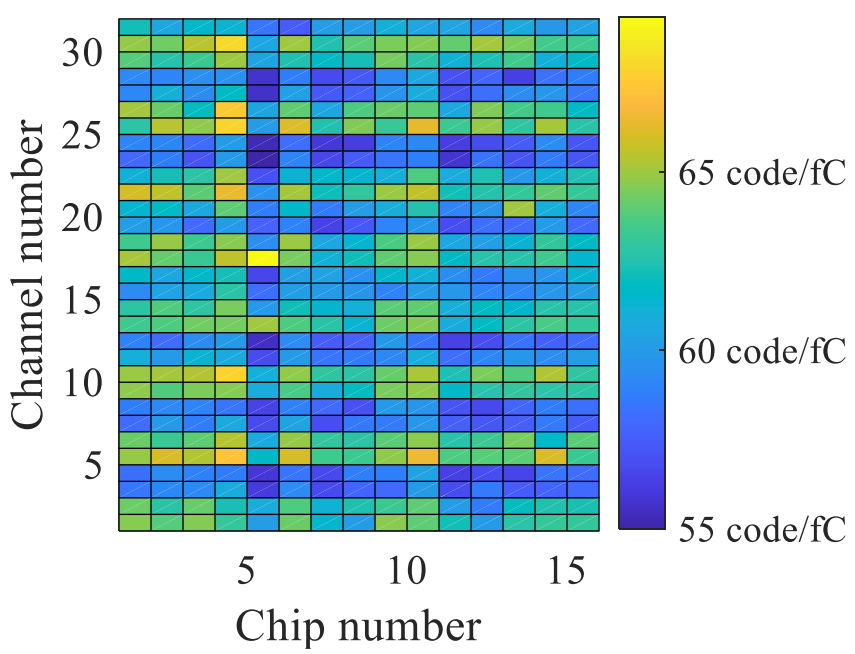
Correction



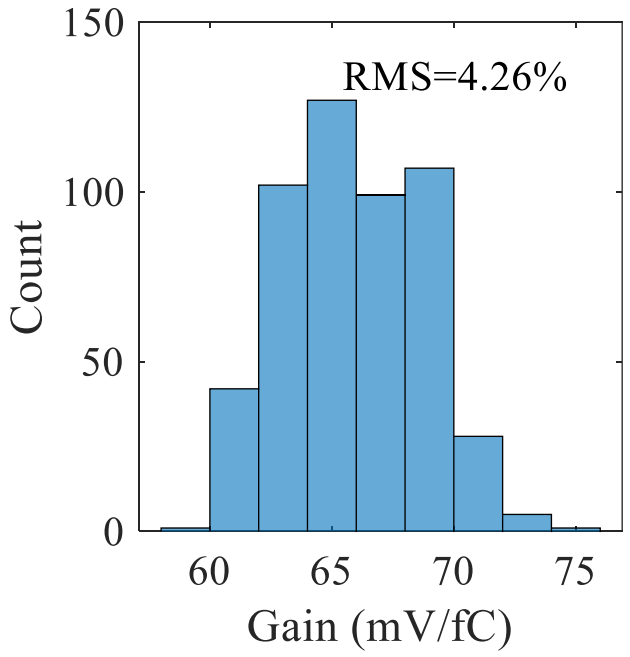
Improve the amplitude resolution based on the stop position

Test of gain non-uniformity

- A test was conducted on the gain uniformity, and the results show that the non-uniformity among all channels on the board is better than 5%.



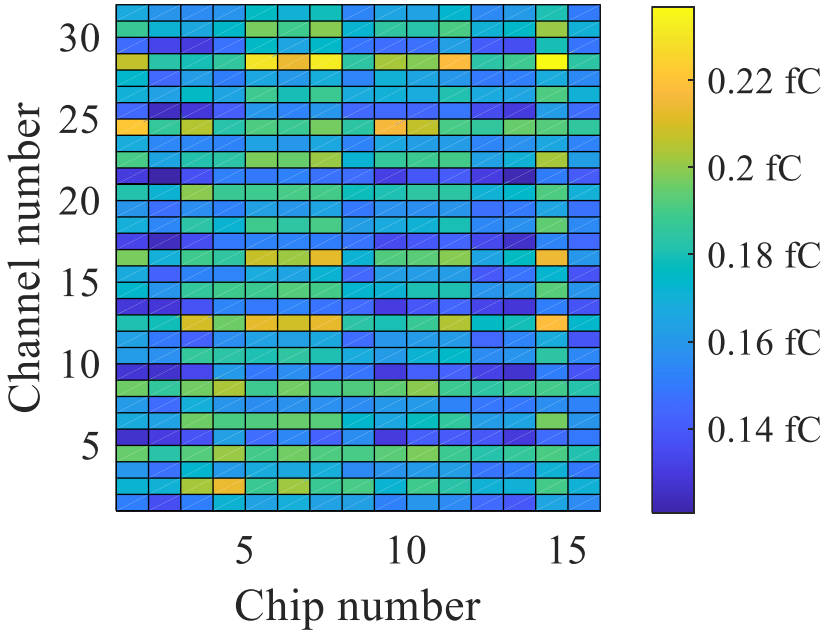
Gain non-uniformity among channels



Gain distribution

Test of charge resolution

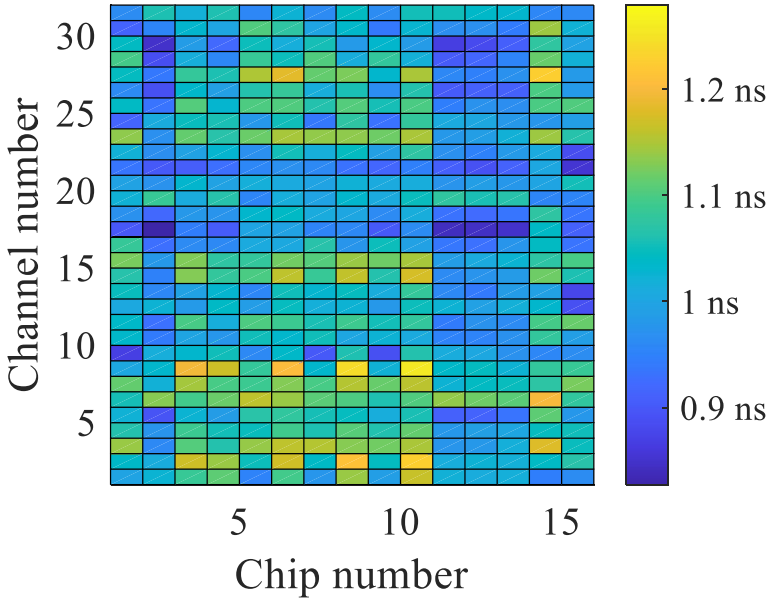
- The charge resolution among all channels are better than 0.24 fC, meeting the design requirement.



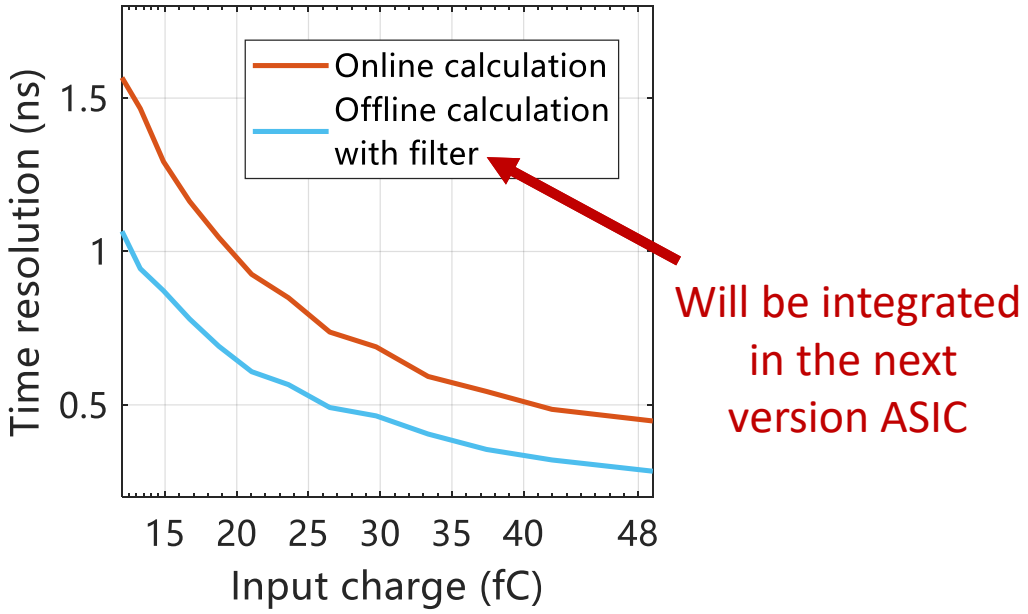
Charge resolution among channels

Test of time resolution

- The time resolution is around 1 ns RMS.
- Offline calculation results in a better resolution with a digital shaper, which will be also integrated in the next version ASIC.



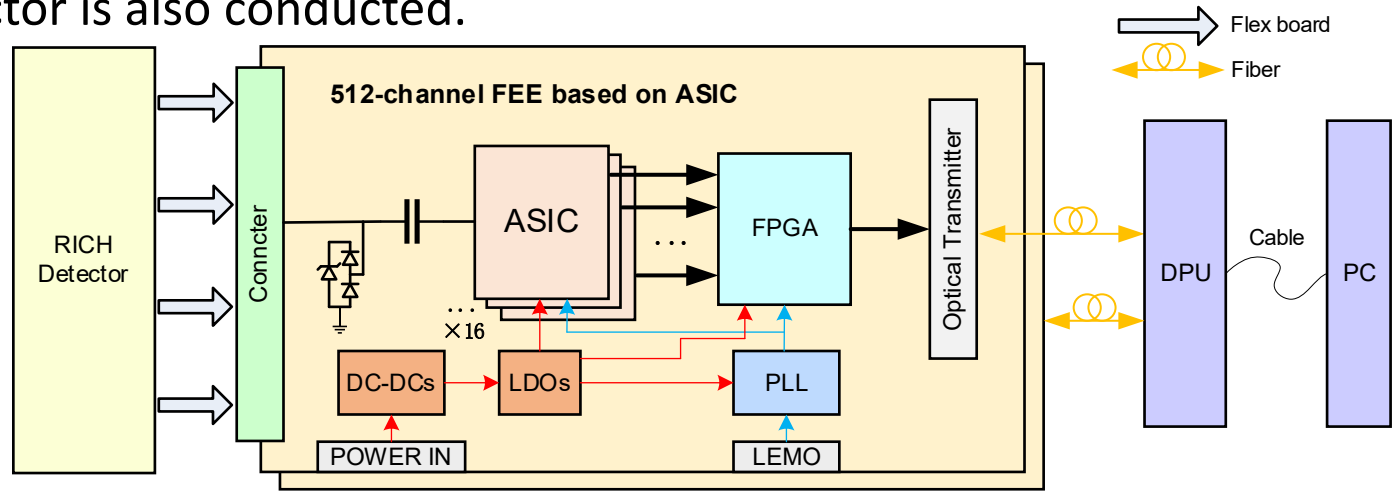
Time resolution od FEE @ 16 fC



Time resolution of ASIC

Test with prototype Detector

- After the validation testing in the laboratory, a joint test with the prototype detector is also conducted.

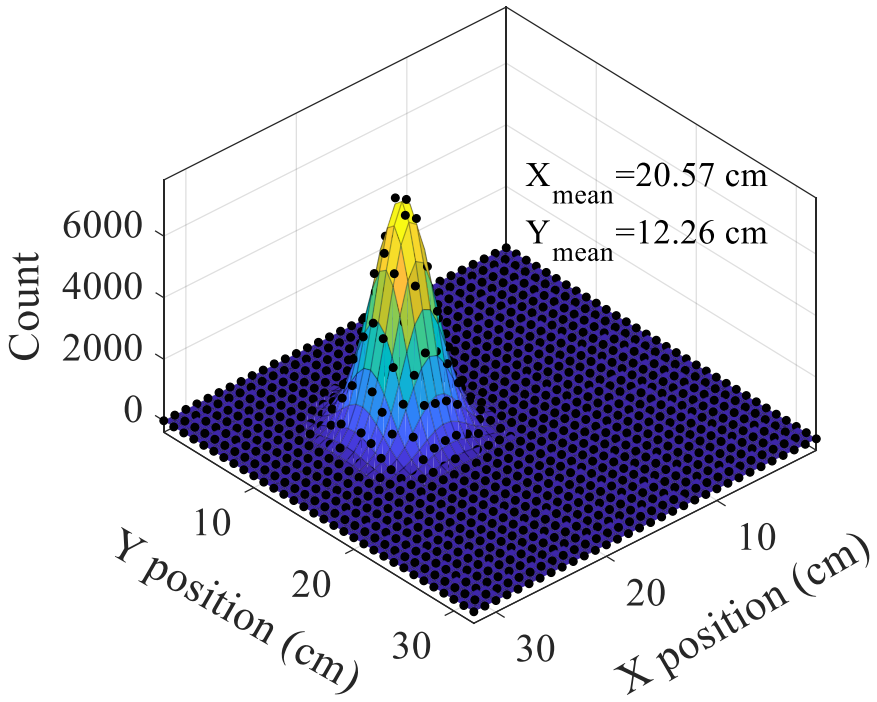


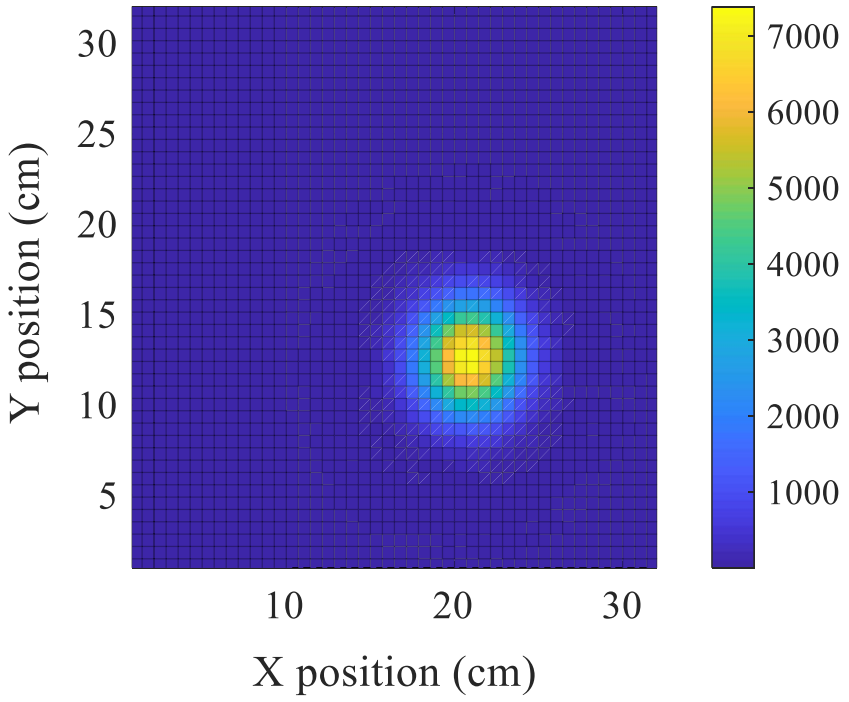
Schematic diagram of the joint test

Photograph of the joint test

Test with ^{55}Fe

- Test condition
  - Gas mixture: Ar:CO_2=93:7
  - Radiation source: ^{55}Fe
  - Effective area: 32 cm × 32 cm
  - Voltage: 470 V - 1120 V

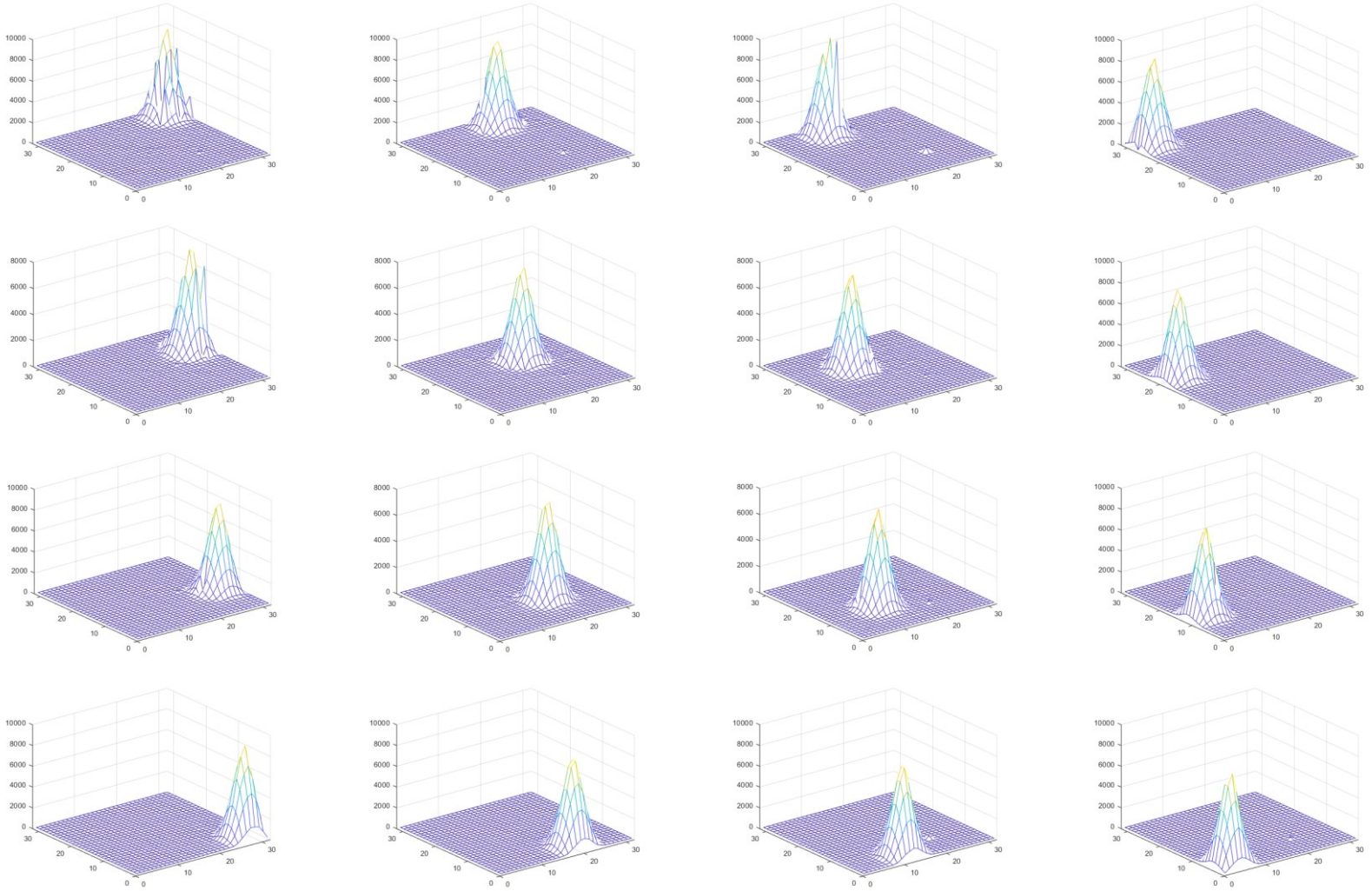




Test with ^{55}Fe

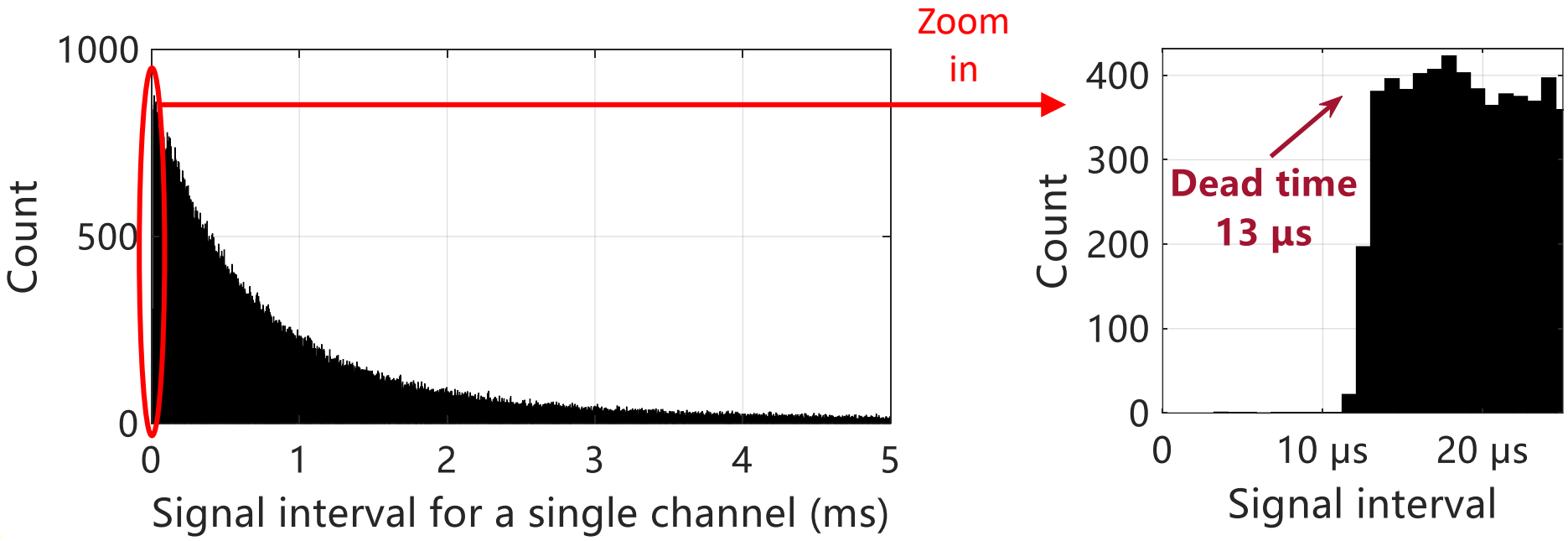
Test with ^{55}Fe

- Test with different hit position.



Test with ^{55}Fe

- By analyzing the time information output from each channel, we can find out the minimum hit interval that a single channel can process.



Time resolution @ 16 fC

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Conclusion

- A 512-channel FEE prototype based on the custom ASIC has been developed to read the MPGD.
- The charge resolution and the time resolution is around 0.24 fC RMS and 1.2 ns RMS respectively, which can be further improved by integrating the digital filter inside the ASIC.
- Dead time per channel is about 13 μs, resulting in a maximum counting rate per channel to be 76 kHz.

Ongoing:

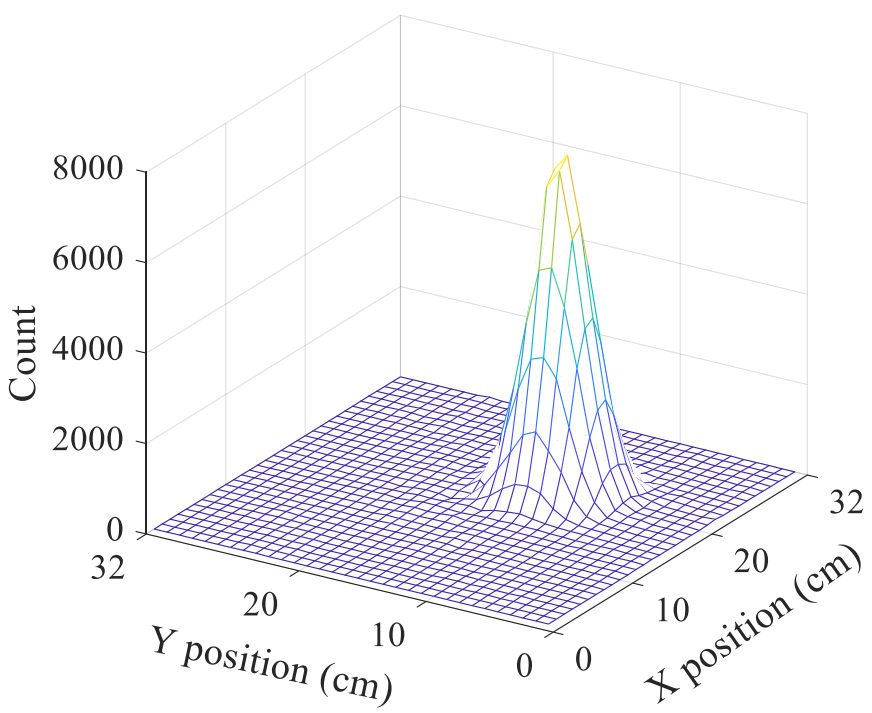
- Next version ASIC development.
- Preparing for the beam test.

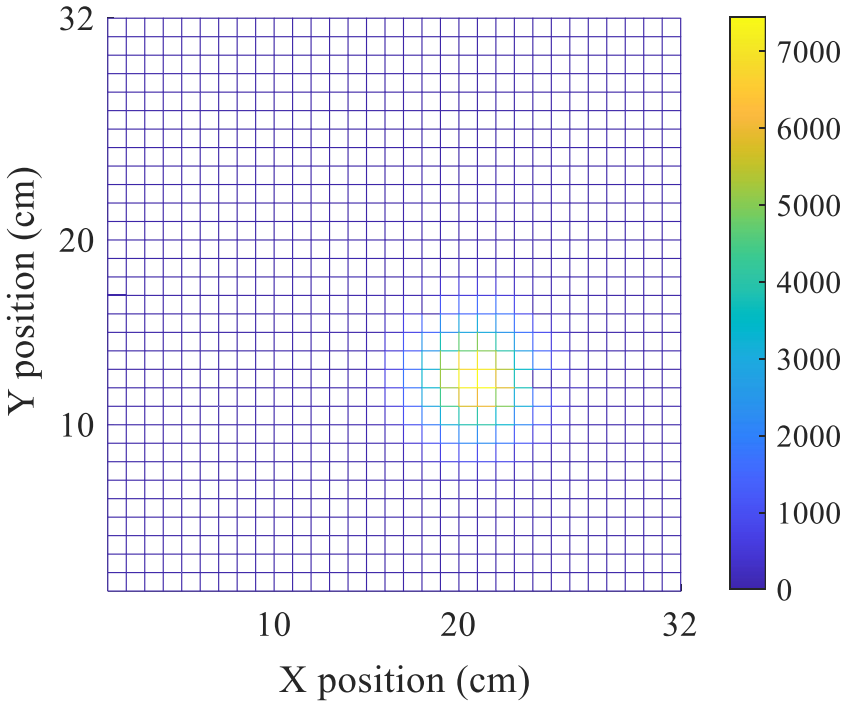
Thanks!

Backup

Test with prototype detector

- Test condition
  - Gas mixture: Ar:CO2=93:7
  - Radiation source: ^{55}Fe
  - Effective area: 32 cm × 32 cm
  - Voltage: 470 V - 1120 V





Test with ^{55}Fe