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# High Spatial Resolution Time Projection Chamber Technology R&D for Future e+e- Collider

## Huirong Qi on behalf of CEPC TPC Study Group and some inputs from LCTPC international collaboration

Institute of High Energy Physics, CAS October 16, 2024, Hefei, China

- Motivation and physics requirements
- High spatial resolution TPC R&D
- Updated pixelated readout TPC R&D
- Summary

## • Motivation and physics requirements

### **Motivation and physics requirements on e+e- collider**

- A TPC is the main track detector for **some candidate experiments at future e+e- colliders** 
  - Baseline detector concept of ALICE, STAR, CEPC CDR and ILD at ILC
  - TPC is a promised candidate as the main track detector in CEPC TDR
- TPC technology can be of interest for other future colliders (EIC, FCC-ee, KEKb...)
- Pixelated readout TPC is potential to **improve PID requirements of Flavor Physics** at e+e- collider.



https://arxiv.org/abs/1811.10545 Huirong Qi

### **Physics requirements on future circular e+e- collider**

- Operation stages in CEPC TDR: 10-years Higgs  $\rightarrow$  2-years Z pole  $\rightarrow$  1-year W
- Physics Requirements of tracker
  - Thousands of hits with high spatial resolution compatible with PFA algorithm (low  $X_0$ )
  - Beneficial for the lower momentum resolution
  - PID of charged hadrons improvement to flavor physics and jet substructure



• High spatial resolution TPC R&D

### • Pixelated readout TPC (Baseline)

- Material budget at endcape/barrel  $\sqrt{}$
- Occupancy and hit density at Tera-Z  $\sqrt{}$

Critical key issues

- Ion backflow suppression  $\sqrt{}$
- Running at 2 Tesla  $\sqrt{}$
- Improved PID for flavor physics  $\sqrt{}$
- **Reasonable channels(ongoing)**
- Reasonable power consumption (ongoing)

### **Roadmap of CEPC TPC detector R&D**

- **CEPC TPC detector prototyping roadmap:** 
  - From TPC module to **TPC prototype R&D for Higgs and Tera-Z**
  - Easy-to-install modular design of Pixelated readout TPC for CEPC TDR
- Achievement by far:
  - **IBF × Gain ~1** @ **G=2000** validation with hybrid TPC module
  - Spatial resolution of  $\sigma_{ro} \leq 100 \ \mu m$  and dE/dx resolution of 3.6%
  - FEE chip: reach ~3.0mW/ch with ADC and the pixelated readout R&D •

TPC prototype with integrated 266nm UV laser



Achievement



-150 -100 -50

50

### Highlights of TPC prototype integrated with 266nm UV laser tracks

### • Highlights of CEPC TPC R&D and toward reasonable pixelated readout TPC

- Massive production and assemble MPGD lab has been setup at IHEP
- TPC prototype integrated 266nm UV laser tracks has been studied and analyzed the UV laser signal, all are pretty good to Higgs run.
- Track reconstruction and the spatial resolution of Pad readout TPC prototype are analyzed.





#### Publications by CEPC TPC group in 2018-2024:

- https://doi.org/10.1088/1748-0221/18/08/E08002
- https://doi.org/10.22323/1.449.0553
- https://doi.org/10.1016/j.nima.2022.167241
- https://doi.org/10.1109/NSS/MIC44867.2021.9875566
- https://doi.org/10.1109/NSS/MIC44845.2022.10399097
- https://doi.org/10.1088/1748-0221/15/09/C09065
- https://doi.org/10.1088/1748-0221/15/05/P05005
- <u>https://dx.doi.org/10.1142/S0217751X20410146</u>
  <u>https://doi.org/10.1088/1674-1137/41/5/056003</u>
- https://doi.org/10.1088/1748-0221/15/02/T02001
- https://doi.org/10.1088/1748-0221/12/07/P07005

### Activity international collaboration

- Activity collaboration: Pixelated readout and Pad readout from IHEP and LCTPC collaboration
  - Large Prototype setup have been built to compare different detector readouts for Tera-Z
  - PCMAG: B < 1.0T, bore  $\emptyset$ : 85cm, Spatial resolution of  $\sigma r\phi \leq 100 \mu m$
  - Collaboration implement improvements in a **pixelated readout TPC for CEPC TDR**

















**Huirong Qi** 

### **Track detector system in CEPC Phy.&Det. TDR**

- Tracker detector system: Silicon combined with gaseous chamber as the tracker and PID
  - Pixelated readout TPC as the **baseline technology** in CEPC ref-TDR.
    - Radius of TPC from 0.6m to 1.8m
  - DC as an **alternative** option at Tera-Z.



### **Detailed design of mechanics**

| TPC detector         | Key Parameters                       |
|----------------------|--------------------------------------|
| Modules per endcap   | 248 modules /endcap                  |
| Module size          | 206mm×224mm×161mm                    |
| Geometry of layout   | Inner: 1.2m Outer: 3.6m Length: 5.9m |
| Potential at cathode | - 62,000 V                           |
| Operation gases      | T2K: Ar/CF4/iC4H10=95/3/2            |
| Maximum drift time   | 34μs @ 2.75m                         |
| Detector modules     | Pixelated Micromegas                 |
|                      |                                      |





Detailed design of TPC detector in ref-TDR

### **Ultra-light barrel and FEA analysis**

- Consideration of new Carbon Fiber barrel instead of the honeycomb barrel (~2% X<sub>0</sub>)
- Ultra-light material of the TPC barrel (QM55 CF) : 0.59%  $X_0$  in total, including
  - FEA preliminary calculation: 0.2mm carbon fibber barrel can tolerant of OTK (~200Kg)
- Optimization of the connection back frame of the endcap (on going)



| Layer of the barrels | D[cm] | X <sub>0</sub> [cm] | d/X <sub>0</sub> [%] |  |
|----------------------|-------|---------------------|----------------------|--|
| Copper shielding     | 0.001 | 1.45                | 0.07                 |  |
| CF outer barrel      | 0.020 | 25.28               | 0.08                 |  |
| Mirror strips        | 0.003 | 1.35                | 0.19                 |  |
| Polyimide substrate  | 0.005 | 32.65               | 0.02                 |  |
| Field strips         | 0.003 | 1.35                | 0.19                 |  |
| CF inner barrel      | 0.010 | 25.28               | 0.04                 |  |
| Sum of the r         | 0.59  |                     |                      |  |

Material budget of TPC barrel

#### Low material of the TPC endcap

| 15%                               | X <sub>0</sub> in total, including |
|-----------------------------------|------------------------------------|
| Readout plane, front-end-electror | nics 4%                            |
| Cooling                           | 2%                                 |
| Power cables                      | 9%                                 |

### **Optimization of Gas flow in Chamber**

- Requirement: Gas uniformity of **99% or more** in large TPC chamber
  - 8 Ø10mm gas inlets + 8 Ø10mm gas outlets (opposite, 90°/endcap)
  - Working Gas Flow: 0.3 0.5 L/min
  - **Online monitoring system**: O<sub>2</sub> (ppm) and H<sub>2</sub>O (ppm)
  - Friendly the gases recycle system also considered





Optimized inlet and outlet in Chamber



Simulation of gas flow and uniformity distribution in TPC Chamber

## • Updated pixelated readout TPC R&D

### **Pixelated readout TPC technology for CEPC TDR**

- A pixelated readout TPC is **a good option to provide realistic physics requirements** of Higgs Physical and Tera-Z Physics also (2E36) at CEPC.
  - Pixelated readout  $\rightarrow$  better resolution  $\rightarrow$  low gain  $\rightarrow$  less distortion
- **Highlights** of Pixelated readout TPC technology for CEPC TDR
  - Can deal with high rates (MHz/cm<sup>2</sup>)
  - High spatial resolution  $\rightarrow$  better momentum resolution
  - PID: dE/dx + dN/dx (**In space**)
  - Excellent two tracks separation





### **Operation on high luminosity Tera-Z at 2 Tesla**



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### Improved dE/dx+dN/dx in space

- Full simulation framework of pixelated TPC developed using Garfied++ and Geant4 at IHEP
- Investigating the  $\pi/\kappa$  separation power using reconstructed clusters, a  $3\sigma$  separation at 20GeV with 120cm drift length can be achieved
- dN/dx has significant improved PID resolution





#### DOI: 10.22323/1.449.0553 EPS-HEP 2023 talk by Yue Chang Huirong Qi

Simulation of TPC detector under 3T/2T and T2K mixture gas

### **Optimization concept option: Pixelated readout TPC** $@\cos\theta \approx 0.98$

| Parameters   | Higgs run                                 | Z pole run   |  |
|--|---|--|--|
| B-field  | 3.0 T                                     | 2.0 T  |  |
| Readout size (mm)/All channels   | 0.5mm×0.5mm/2×3×10 <sup>7</sup>           | 0.5mm×0.5mm/2×3×10 <sup>7</sup>                          |  |
| Layers per track in rφ   | 2300                                      | 2300   |  |
| Material budget barrel (X <sub>0</sub> )                                   | 0.59 %                                    | 0.59 %   |  |
| Material budget endcap (X <sub>0</sub> )                                   | 15 %                                      | 15 %   |  |
| $\sigma_{r\phi}$ (cluster level)   | 120μm (full drift)                        | 400µm (full drift) w. distortion                         |  |
| σ <sub>z</sub> (cluster level)   | ≃ 0.6 - 1.0 mm<br>(for zero – full drift) | $\simeq 0.6 - 1.0 \text{ mm}$<br>(for zero – full drift) |  |
| 2-hit separation in rq   | 0.5 mm                                    | 0.5 mm   |  |
| K/ $\pi$ separation power @20GeV   | 3σ  | 3σ   |  |
| dE/dx  | < 3.0 %                                   | < 3.0 %  |  |
| Momentum resolution normalized:<br>$\sigma_{1/pT} = \sqrt{a^2 + (b/pT)^2}$ | a = 1.9 e -5                              | a = 3.3 e -5   |  |
|  | b = 0.8 e -3                              | b = 1.5 e -3   |  |

### **Reasonable channels and power consumption**

- Power consumption relative with the high granularity readout
  - Pad readout TPC@1mm×6mm pad size
    - Total channels:  $10^6$ ; Total power: <10 kW using 2-phase CO<sub>2</sub> cooling
  - Pixelated readout TPC at the endcap
    - Total power: <10 kW
      - 2-Phase CO<sub>2</sub> cooling
      - <100mW/cm<sup>2</sup>
  - ASIC chip and TPC prototyping R&D



| DOI: 10.1088/1748-                  | 0221/15/02/T02001 |  |
|-------------------------------------|-------------------|--|
| DOI: 10.1088/1748-0221/15/05/P05005 |                   |  |
| Huirona Oi                          |                   |  |

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|----|--|

|                       | PASA+ALTRO            | Super-ALTRO          | SAMPA                 | WASA_v1             |
|-----------------------|-----------------------|----------------------|-----------------------|---------------------|
| TPC                   | ALICE                 | ILC                  | ALICE upgrade         | CEPC                |
| Pad Size              | 4x7.5 mm <sup>2</sup> | 1x6 mm <sup>2</sup>  | 4x7.5 mm <sup>2</sup> | 1x6 mm <sup>2</sup> |
| No. of Channels       | 5.7× 10 <sup>5</sup>  | $1-2	imes10^6$       | $5.7	imes10^5$        | 2 x×10 <sup>6</sup> |
| Readout Detector      | MWPC                  | GEM/MicroMegas       | GEM                   | GEM/MicroMegas      |
| Gain                  | 12 mV/fC              | 12-27 mV/fC          | 20/30 mV/fC           | 10-40 mV/fC         |
| Shaper                | CR-(RC) <sup>4</sup>  | CR-(RC) <sup>4</sup> | CR-(RC) <sup>4</sup>  | CR-RC               |
| Peaking time          | 200 ns                | 30-120 ns            | 80/160 ns             | 160-400 ns          |
| ENC                   | 370+14.6 e/pF         | 520 e                | 246+36 e/pF           | 569+14.8 e/pF       |
| Waveform Sampler      | Pipeline ADC          | Pipeline ADC         | SAR ADC               | SAR ADC             |
| Sampling Rate         | 10 MHz                | 40 MHz               | 10 MHz                | 10-100 MHz          |
| Sampling Resolution   | 10 bit                | 10 bit               | 10 bit                | 10 bit              |
| Power: AFE            | 11.7 mW/ch            | 10.3 mW/ch           | 9 mW/ch               | 1.4 mW/ch           |
| Power: ADC            | 12.5 mW/ch            | 33 mW/ch             | 1.5 mW/ch             | 0.8 mW/ch@40 MHz    |
| Power: Digital Logics | 7.5 mW/ch             | 4.0 mW/ch            | 6.5 mW/ch             | 2.7 mW/ch@40 MHz    |
| Total Power           | 31.7 mW/ch@10MHz      | 47.3 mW/ch@40 MHz    | 17 mW/ch@10 MHz       | 4.9 mW/ch@40 MHz    |
| CMOS Process          | 250 nm                | 130 nm               | 130 nm                | 65 nm               |

### **Prototype validation of pixelated TPC for CEPC TDR**

- Pixelated Readout Electronics: TEPix development
  - Multi-ROIC chips + Interposer PCB as RDL
  - Four-side buttable
- TEPix: Low power Energy/Timing measurement
  - Low power consumption: 0.5mW/ch@2nd Chip
  - Timing: 1 LSB(<10ns)
  - Noise: 300e- (high gain)





FEE ASIC: TEPIX—Test Results in May

### **Prototype validation of pixelated TPC for CEPC TDR**

- R&D on Pixelated TPC readout for CEPC TDR.
  - ASIC chip developed and 2<sup>nd</sup> prototype wafer has been done and tested.
  - The TOA and TOT can be selected as the initiation function in the ASIC chip
- Beam test of the pixelated readout TPC prototype in preparation in 2024. (December before)



Photos TPC modules assembled for the beam test ILD conference 2024 January by Zhi Deng Huirong Oi







Amplitude (left) and Uniformity/ch (right)

• TPC detector prototype R&D using pad readout towards pixelated readout for the future e+e- colliders, even the high luminosity Z pole running. DC will be as the alternative detector at Tera-Z.

• Pixelated TPC is choose as the baseline gaseous tracker in CEPC ref-TDR. The simulation results show the good performance of PID, momentum resolution and tracks. Some validation of TPC prototype have been studies.

• Synergies with CEPC/FCCee/EIC/LCTPC allow us to continue R&D and ongoing with the significant international collaboration. All will input to CEPC ref-TDR in next few months.

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