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SALSA: a new versatile readout chip for MPGD detectors

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MPGD 2024 conference

18/10/2024

Context

SALSA specifications and architecture

Timeline and recent results

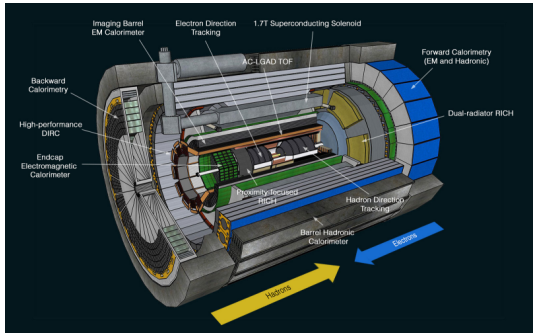
Prospects

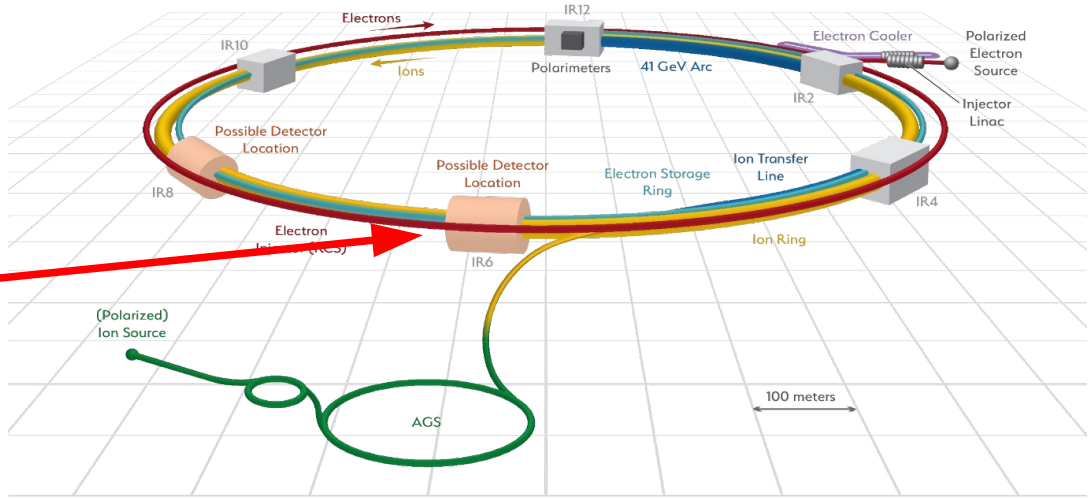
THE EIC PROJECT

EIC collider

- Hadron physics: nucleon structure, quarks and gluons spins, gluon saturation, etc...
- High luminosity electron-ion collider (all nuclei from p to U) at BNL (USA), also with polarized beams: e, p, d, ^{3}He
- 5-18 GeV e^- vs 40-275 GeV p, 20-100 GeV in CoM
- First beam ~ 2034
- 2 experiments: EPIC (already financed) and "Detector 2"

EPIC experiment





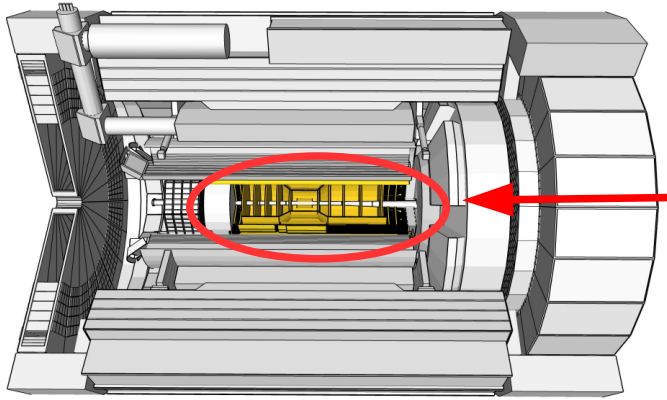
THE MPGD TRACKERS OF EPIC EXPERIMENT

MPGD detectors foreseen in EPIC

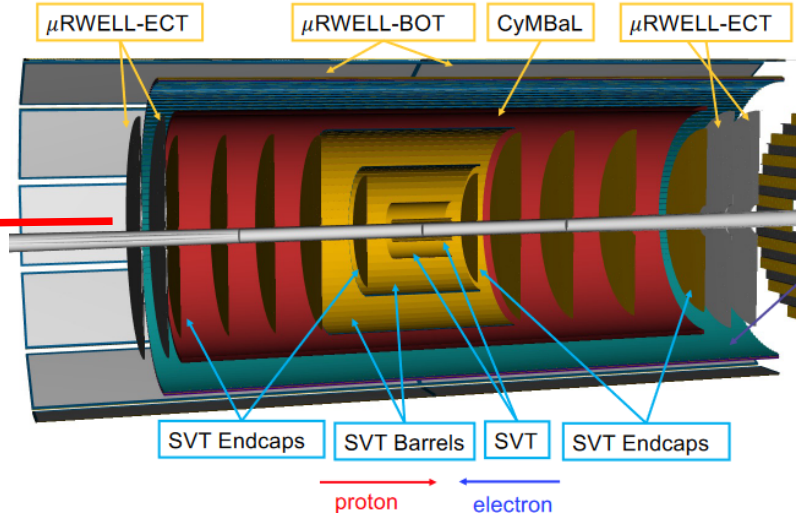
- Cylindrical Micromegas barrel layer (CyMBaL) → ~30 k.channels
- µRWell barrel outer tracker (µRWell-BOT) → ~100 k.channels
- µRWell end cap tracker (µRWell-ECT) → ~30 k.channels

- Same readout ASIC to read all MPGD trackers → **SALSA**

EPIC detector



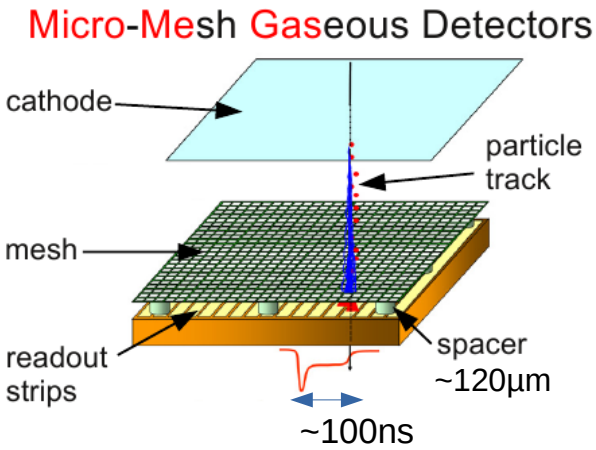
Central trackers



EXPECTATIONS ON MPGD DETECTOR READOUT

Micro-Pattern Gaseous Detector characteristics

- Detection of gas ionization from charged particles
- Small gaseous amplification gap → short signals ~ 100 ns
- Gain 5-10k → typical signal amplitude ~35 fC, max ~200-250 fC

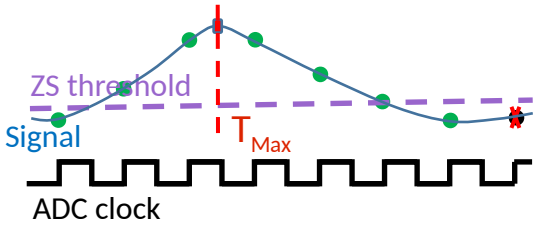


Required readout performance

- Threshold ~3 fC to get factor 10 on signal / threshold
- Noise level ~0.5 fC
- Readout time resolution << detector resolution (~10 ns)
- Stand channel occupancy ~10 kHz
- Resistant to mild radiation (10 krad, 10^{11} n_{eq}/cm^2) and magnetic field (1.8 T)

Readout strategy

- No trigger from DAQ, continuous readout
- Analog amplification and shaping, ADC sampling signals at ~50 MS/s
- Digital processing of samples (baseline, shaping corrections)
- Zero-suppression: selection of samples above threshold + neighbors
- Samples surviving ZS sent to DAQ continuously
- + Integrated reconstruction of signal amplitudes and times



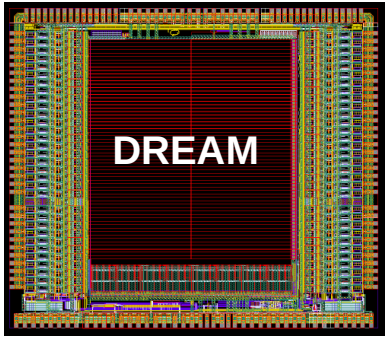
SALSA specifications and architecture

SALSA : VERSATILE READOUT CHIP FOR MPGD

Motivations of the SALSA project

- To develop a new versatile multi-channel readout chip in the framework of the EPIC MPGD trackers and beyond
  - for MPGD trackers, but also for MPGD TPCs, photon detectors,...
  - with possible future developments for other kinds of detectors (calorimeters, non-MPGD photon detectors) and/or specific constraints
  - adapted to streaming readout and triggered DAQs
- Integrated per-channel sampling ADC at high rate, and digital processing (DSP)
- Large ranges of signal amplitudes, electrode capacitances, peaking times, signal rates
- TSMC 65nm technology for improved performances and sustainability

Common initiative of Sao Paulo Universities and CEA Saclay IRFU



- Sao Paulo University (USP) + associated institutes designed the **SAMPA** chip (ALICE TPC), experts in on-chip ADC and digital processing
- IRFU developed several MPGD front-end chips (**AFTER**, **AGET**, **DREAM**,...) and other kinds of chips (**SAMPIC** and **HGCROC** TDC,..), experts in low-noise radiation-hard generic front-ends
- Complementary competences on front-end, digitization and digital processing
- Blocks developed by CERN in TSMC 65nm technology also reused

SALSA CHIP TARGET SPECIFICATIONS, COMPARED TO EPIC MPGD REQUIREMENTS

Versatile front-end characteristics → EPIC MPGD needs

- 64 channels
- Large input capacitance range, optimized for 50-200 pF, reasonable gain up to 1 nF → **200 pF**
- Large range of peaking times: 50-500 ns → **100-200 ns**
- Large choice of gain ranges: 0-50, 0-250, 0-500 fC or 0-5 pC → **0-250 fC**
- Large range of input rates, up to 100 kHz/ch with fast CSA reset → **< 25 kHz**
- Both polarities (depends on kind of detector) → **negative**

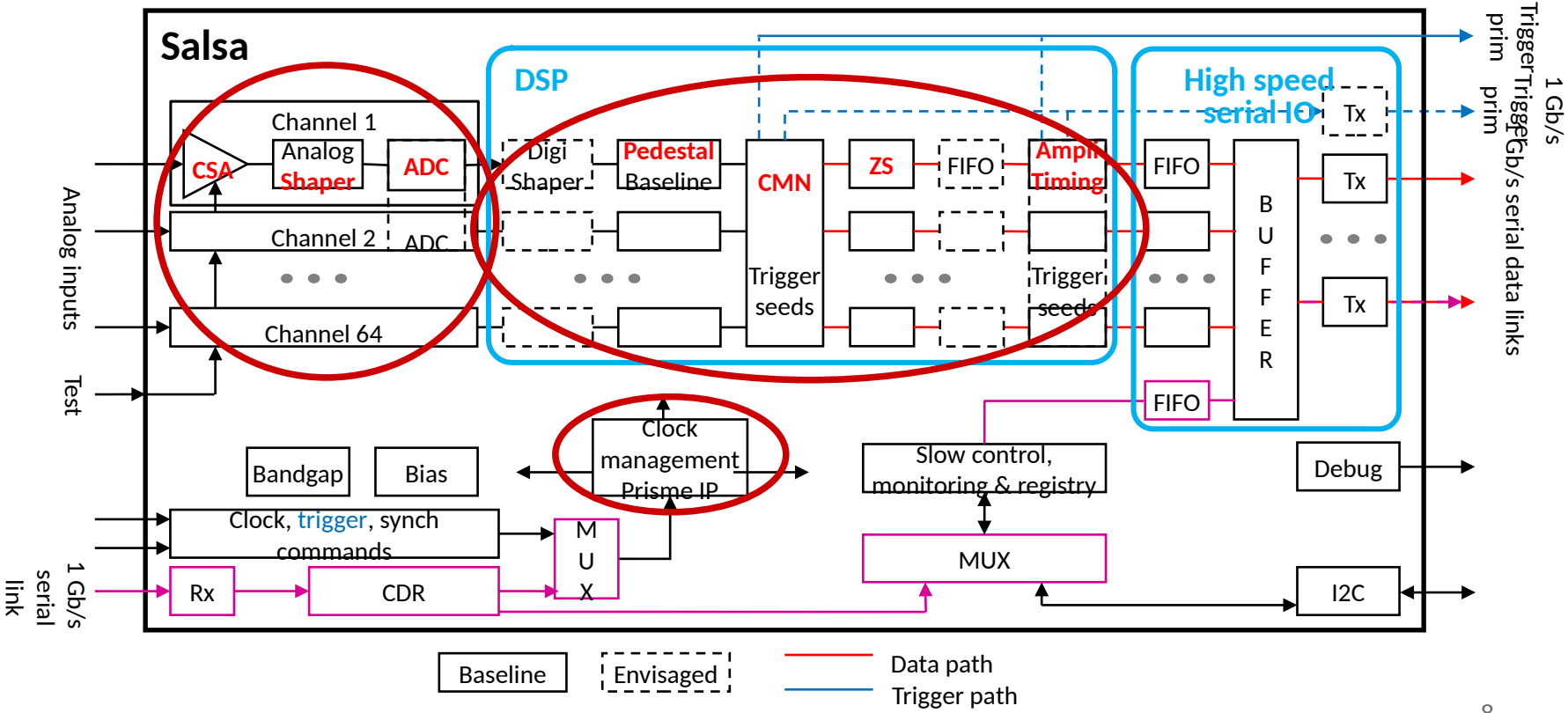
Digital stage

- Fast sampling ADC for each channel on 12 bits (> 10 effective bits) at up to 50 MS/s → **50 MS/s**
- Integrated DSP for internal data processing and size reduction, configurable treatment processes → **all processes**
- Continuous readout, triggered readout → **continuous readout**
- Four 1 Gb/s output data links → **1 (or 2) gigabit link used at EPIC**

General characteristics

- ~1 cm^2 die size, implemented on modern TSMC 65nm technology
- Low power consumption ~ 15 mW/channel at 1.2V
- Radiation hardened (SEU, > 300 Mrad, > 10^{13} n_{eq}/cm^2) → **10 krad, 10^{11} n_{eq}/cm^2**

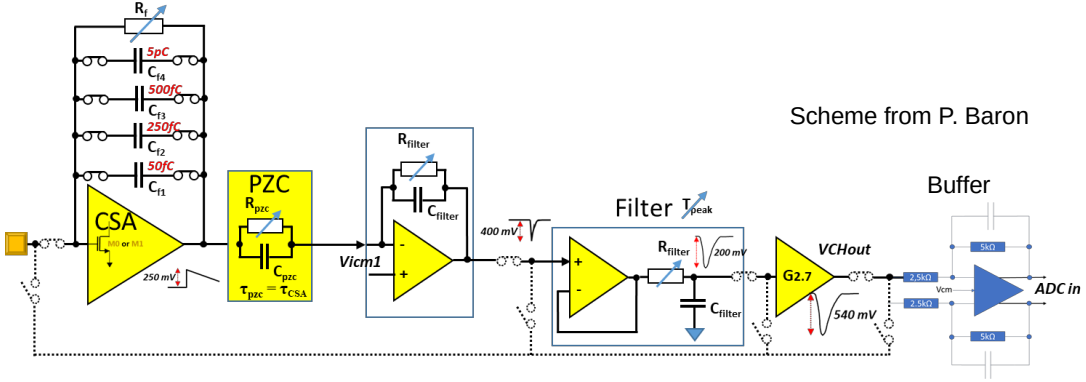
SALSA CHIP PRELIMINARY ARCHITECTURE



SIGNAL AMPLIFICATION AND DIGITIZATION

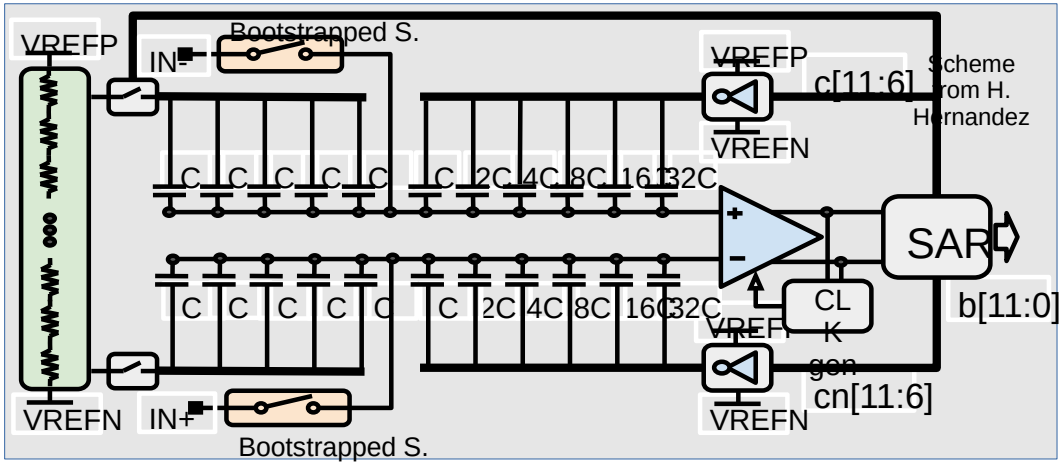
Front-end stage

- Charge Sensitive Amplifier + Pole-Zero Cancellation + shaper
- 4 gain ranges: 0-50 fC, 0-250 fC, 0-500 fC and 0-5 pC
- 8 peaking times 50 to 500ns
- 2 polarities
- Integrated anti-saturation circuit
- Front-end elements can be by-passed
- Integrated test pulses



ADC block

- 12 bits 5-50 MS/s SAR ADC
- Expected 10-11 ENOB bits
- Also evaluation of new ADC developed at IRFU for DRD7



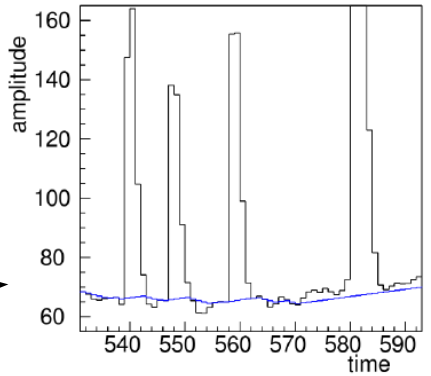
DSP DATA PROCESSING, PRELIMINARY VERSION

General remarks

- ADC data processing, reduction and formatting
- Each process can be configured and deactivated individually by user
- Most of DSP features determined, details still under study
- Part of codes from SAMPA chip

Baseline corrections

- Pedestal subtraction with fixed value per channel
- Correction of common mode noise, based on median value of samples of all channels for each sample time
- Baseline slope following algorithm



Plot from SAMPA doc

Digital shaping

- Cancellation of signal tail or peaking time correction with cascade of 4 first order IIR filters
- Algorithm from SAMPA, 2 x 4 parameters

$$y[n] = a_1 y[n-1] + b_0 x[n]$$

DSP DATA PROCESSING, PRELIMINARY VERSION

Zero suppression

- Keep samples above fixed thresholds
- Tunable algorithm (add neighbor samples, drop too short set of samples, keep 1 sample over N, etc...)

Feature reconstruction

- To further reduce data flux by extracting reconstructed data → peak finding algorithm, with extraction of amplitude + time + width
- Peak finding and data extraction algorithms under study

External trigger management

- Samples kept when trigger signals received, configurable latency
- Associated or not with zero suppression, feature reconstruction, etc…

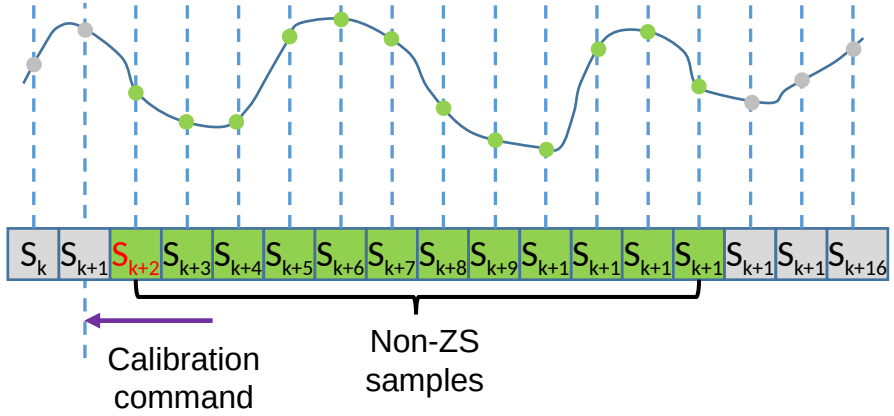
Trigger generation

- Trigger primitives generated when samples above threshold, with conditions on number of samples, multiplicity, etc...
- Latency reduction by placing trigger generation early in the processing chain
- Trigger primitives to be defined (logic signal, data on specific fast link, etc…)

DSP DATA PROCESSING, PRELIMINARY VERSION

Calibration data

- Generated on demand with specific synchronous commands
- Calibration data of several types
  - non-ZS data
  - test pulses injected at front-end on one or several channels



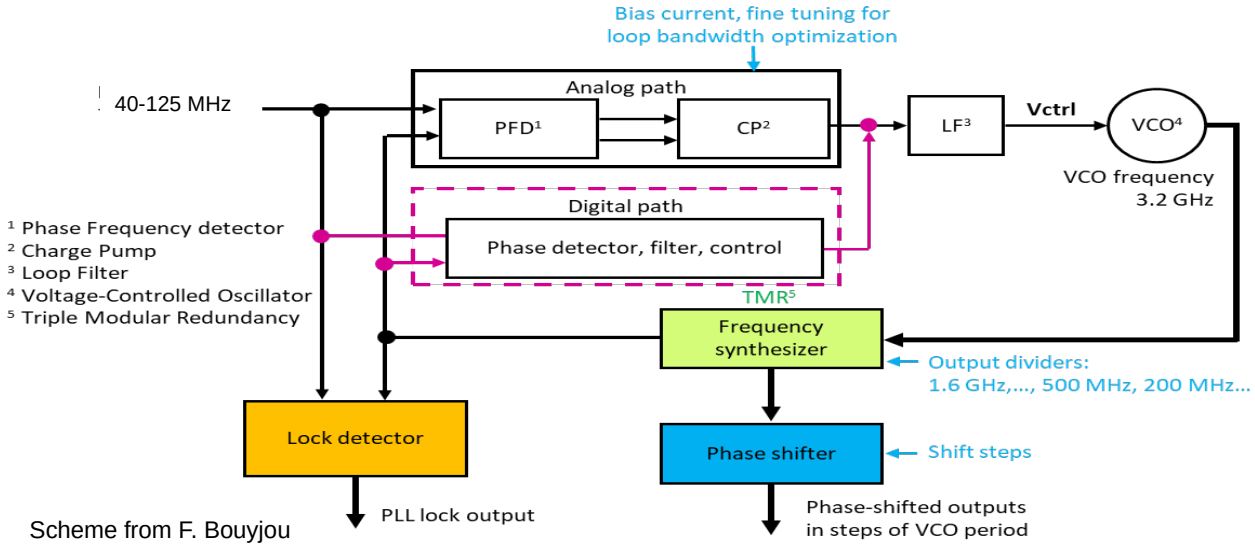
Information data

- Monitoring data: chip configuration, internal chip status (currents, voltages), environmental data (temperature, radiation, etc...)
- Slow-control responses
- Software scaler histogram to evaluate occupancy per channel
- Generated on specific synchronous commands and/or slow-control

SALSA PLL BLOCK FOR CLOCK GENERATION

Development of the "PRISME" 65nm PLL IP block for clock generation

- No existing PLL block fitting our requirements in TSMC 65nm technology
- Hybrid PLL mixing analog and digital paths, with 3.2 GHz VCO frequency
- Large frequency ranges for input (40-125 MHz) and outputs (up to 1.6 GHz)
- 4 clock outputs each with programmable frequency and phase
- Very low internal time jitter: ~3 ps RMS up to 1 GHz
- Low power and radiation hardness capability



Scheme from F. Bouyjou

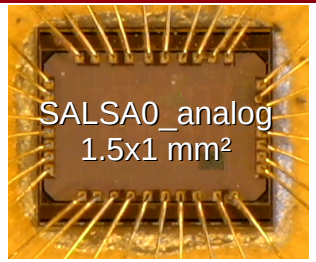
Technology	CMOS 65 nm
Power voltage	1.2V
Input reference frequency range	40-125 MHz
VCO frequency	3.2 GHz
Number of output clocks	4
Output frequency	Programmable fractions of VCO frequency, up to 1.6 GHz
Phase shifter step	< 300 ps
Time interval jitter: analog path only	< 10 ps RMS up to 1 GHz with graceful degradation beyond
Time interval jitter: with digital paths	~3 ps RMS up to 1 GHz with graceful degradation beyond
Power consumption	< 3 mW, < 6 mW with digital regulation
Size	~0.1 mm²
Radiation mitigation	TMR, SEL free, TID up to 4 MGy

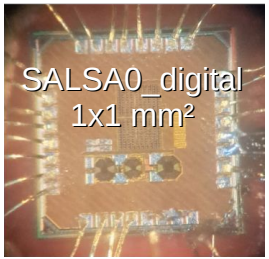
Timeline and recent results

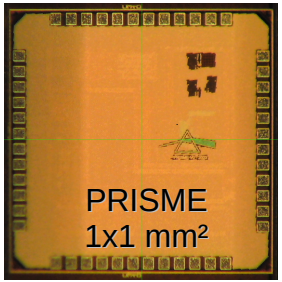
TIMELINE OF THE SALSA PROJECT

Steps of SALSA development

- 2020-22: Discussions and reflections on the project
- 2022-23: **SALSA0** prototypes to study first designs
  - **SALSA0_analog** featuring 4 front-end channels
  - **SALSA0_digital** featuring an ADC block
- 2023: **PRISME** prototype to test PLL block + first version of general services
- 2023-24: **SALSA1** prototype to test full front-end + ADC chains
- 2023-25: **SALSA2** prototype to test ASIC including DSP, but with small number of channels (≤ 32)
- 2025-26: **SALSA3** as pre-serial prototype with nominal number of channels

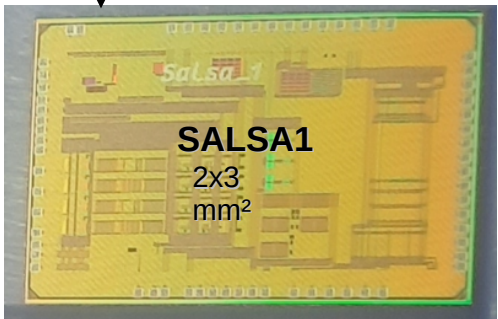






Current status

- **SALSA0** prototypes tested in 2023-2024, performance evaluation and bug fixes of frontend and ADC blocks
- **PRISME** prototype tested from early 2024, bug fixes on PLL block, performance evaluation ongoing, radiation tests in November
- **SALSA1** prototype submitted April 2024, produced, packaging ongoing
- **SALSA2** architecture and DSP design ongoing, submission foreseen ~ March 2025



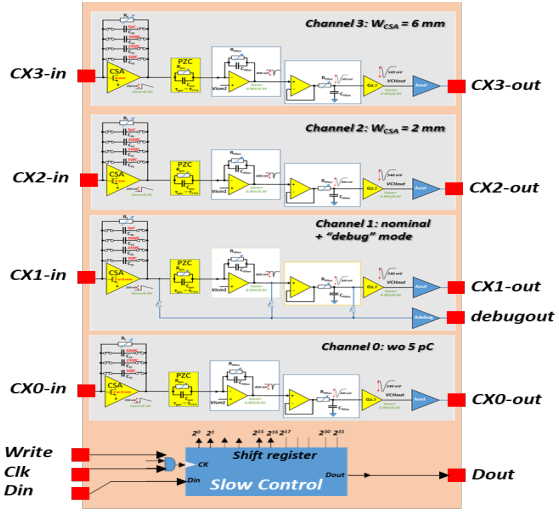
TESTS ON FRONT-END STAGE

SALSA0_analog prototype

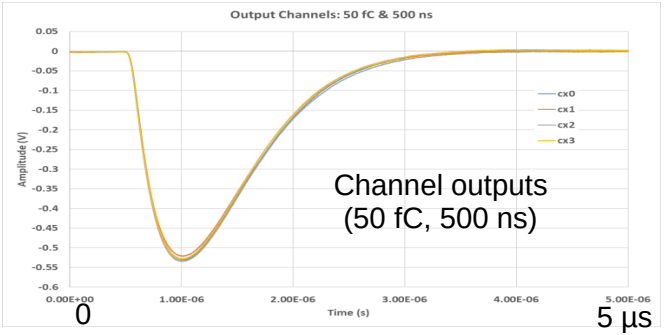
- 4 front-end channels with slight differences between them
- CX1 channel with debug output for monitoring
- CX0-2-3 with different input transistors, CX0 without 5 pC gain range

Test results

- Test-bench: configurable input capacitance, configurable input signal generation, programmable oscilloscope, etc...
- All configuration parameters (gains, peaking times, anti-saturation,...) tested ok
- Measurements in agreement with simulations: bias currents, power consumption, DC values, etc...
- However some discrepancies concerning transfer functions and noise levels especially at 50 fC gain range
- Origin due to parasitic resistances in the chip, understood and reproduced in simulations. Corrected in the CSA design for SALSA1

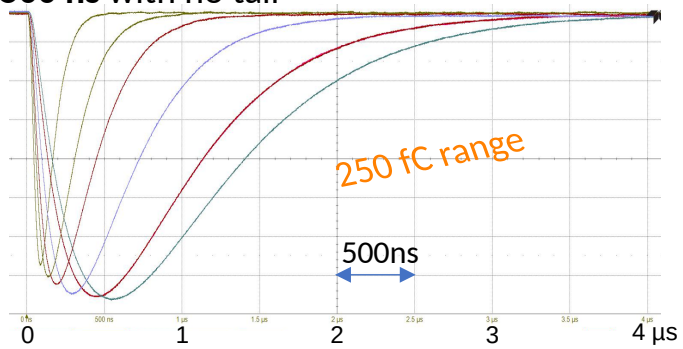


Scheme from P. Baron

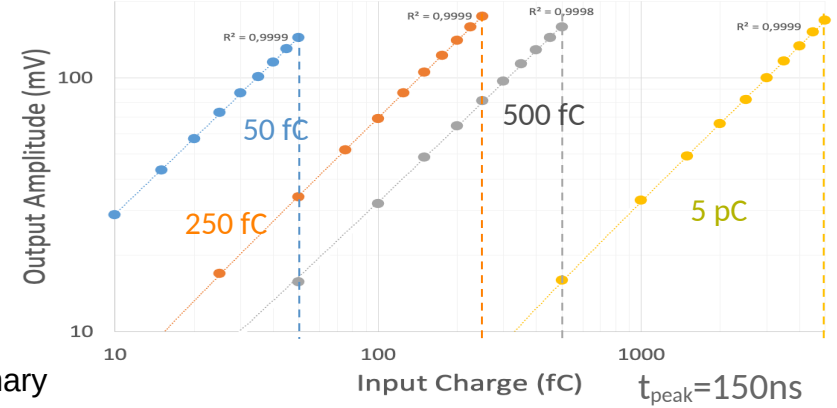


MAIN RESULTS ON SALSA0_ANALOG WITH 120 PF INPUT CAPACITANCE

Peaking time programmable from **50 ns to 500 ns** with no tail

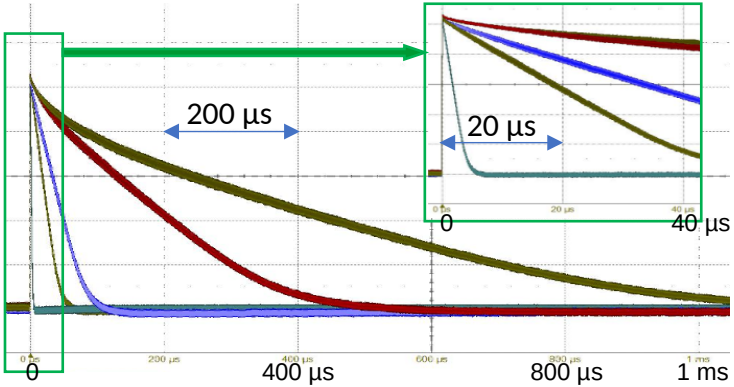


Programmable gain => dynamic range from **50 fC to 5 pC**

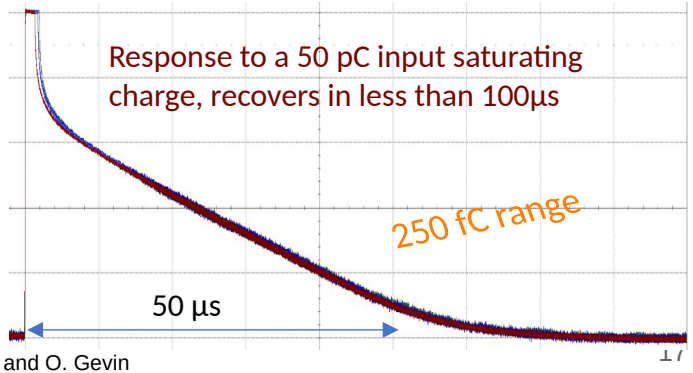


Preliminary

T_{fall} CSA programmable from 5 µs for high rate to 1 ms for low noise



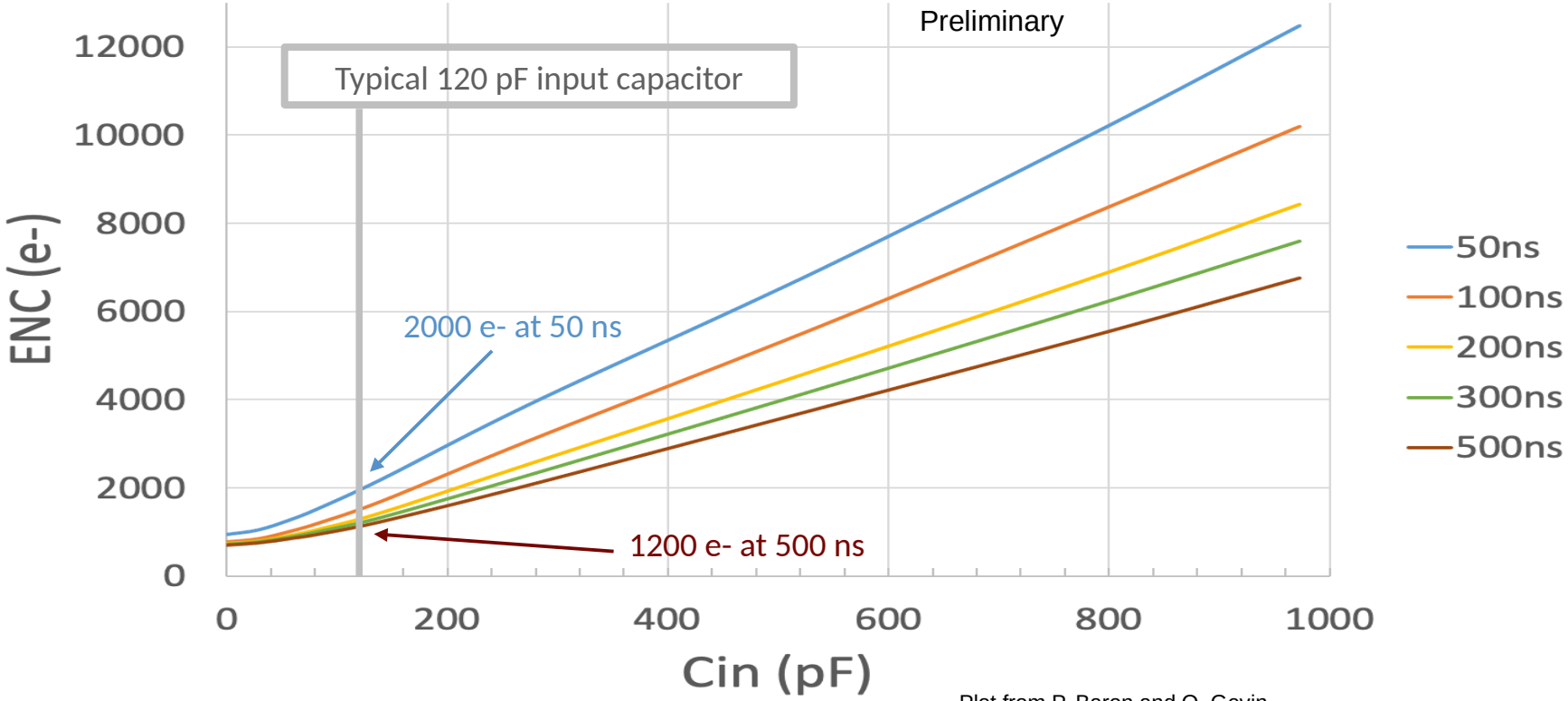
CSA anti-saturation circuit => **fast recovering**



Plots from P. Baron and O. Gevin

MAIN NOISE RESULTS ON SALSA0_ANALOG: TYPICAL CASE

Equivalent Noise Charge in the **250 fC range** at different peaking times

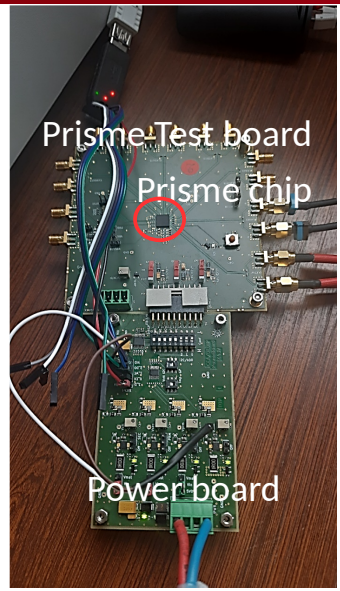


Plot from P. Baron and O. Gevin

STATUS OF PRISME PLL PROTOTYPE

Test bench

- Power boards + PRISME test boards
- Low jitter clock generator from CERN + high precision signal generator, high end 80GS/s scope and phase noise analyzer

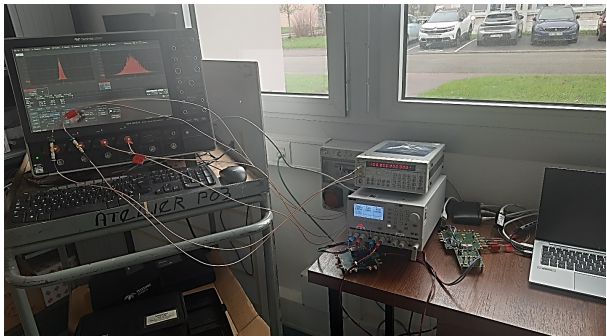


Generic results

- I2C ok, temperature probe ok, radiation probe ok
- LVDS high speed I/O interface ok up to 1.2 Gb/s
- Clock outputs with adjustable phase and frequencies ok
- Radiation TID tests foreseen in November

Tests on PLL block

- PLL block including digital branch working as expected
- Nominal internal 3.2 GHz reached with wide input frequency range achieved 80-105 MHz
- Random jitter component as low as 2.5 ps RMS
- But deterministic component too large, up to 50 ps RMS
- Origin identified in simulation (low frequency noise of 3 GHz VCO)
- Solution found, design corrected
- Possible updated chip to be submitted end of 2024



CONCLUSIONS

SALSA readout chip

- Development of a versatile readout ASIC: large range of gain, peaking time, capacitance, input rate, sampling rate,…
- Internal digitization and data processing to reduce bandwidth, continuous readout
- Rad hard, low power consumption

Present status

- Specifications of DSP almost finalized. Still open to suggestions
- SALSA0 and PRISME prototypes with promising performance measurements; helpful to fix bugs, and verify simulations
- SALSA1 prototype (front-end + ADC) produced, tests starting in November
- SALSA2 prototype (fully featured, reduced number of channels) development ongoing: DSP architecture and data processing
- Grant from EIC eRD109 R&D and Generic EIC R&D programs, and from French and Brazilian ANR and FAPESP research agencies obtained in 2024

PROSPECTS

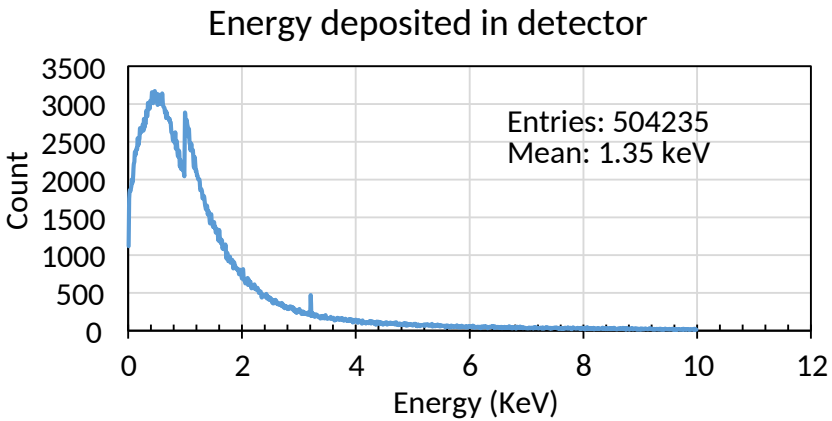
Next steps

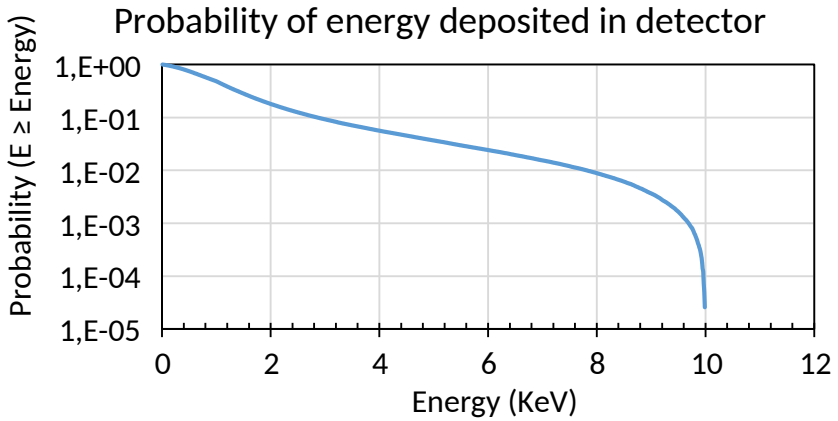
- Completion of tests on PRISME prototype, radiation tests in November
- Tests of SALSA1 from November 2024
- Submission of SALSA2 in 2nd quarter 2025
- Design of SALSA3 pre-serial ASIC in 2025, production and tests in 2026
- Full production in 2027, 5000 ASICs foreseen for EPIC, probably more for other projects, compatible with the EIC project timeline
- Expressions of interest welcome !

Spares

Energy deposit in detector

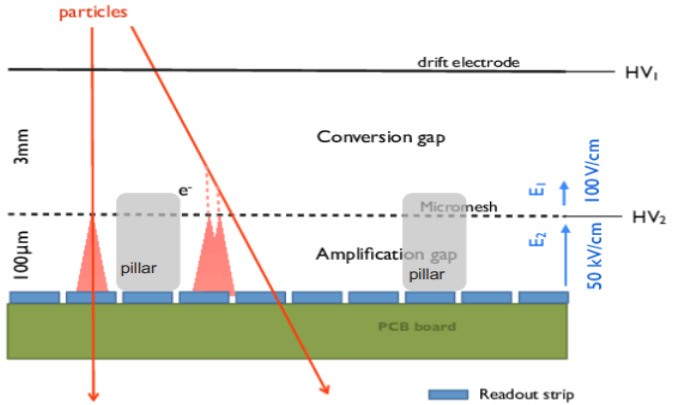
- Energy deposit simulations for physics events





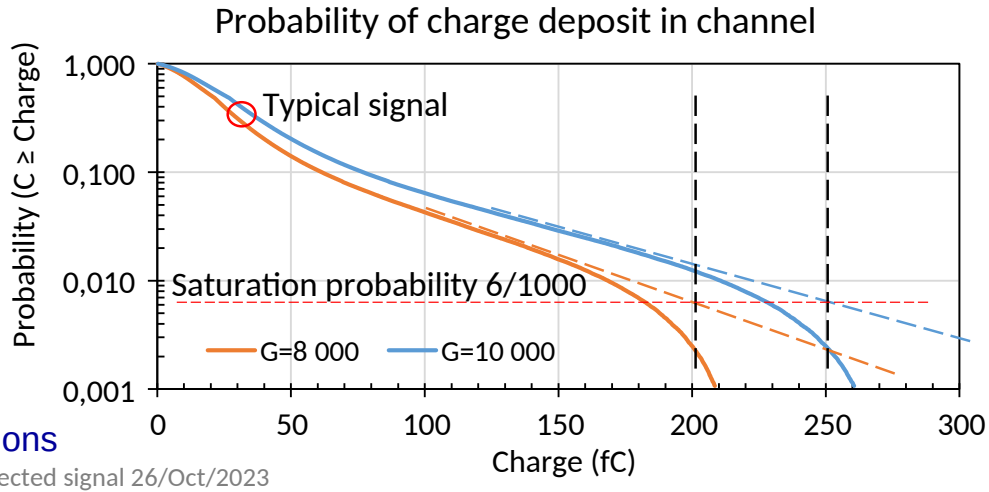
- Typical signal: ~1.35 keV

- Detector:
  - → Conversion gap: 3 mm
    - Electrons in conversion gap: ~50
  - → Amplification gain: 8 000 – 10 000
    - 400 – 500 ke

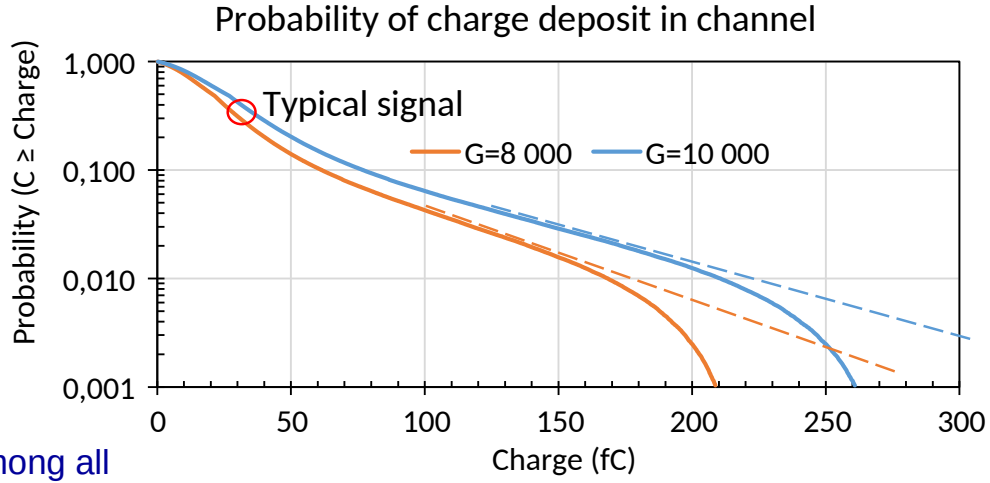


Charge on electronics channel

- Detector gain largely selectable
  - → Typical values of 8 000 – 10 000
- Hypothesis: cluster size: ~4 strips
  - → Strip with max energy: 65% of cluster energy
    - Parameters have to be known better
- Assume charge collection efficiency of the order of 70%
  - → Only this fraction reaches electronics channel
    - Due to detector capacitance, cable interconnect, cross-talk, …
      - Pessimistic estimate for the timing being
      - Will be known better with advances in detector, interconnect and frontend design
- Mean charge
  - → 30-35 fC for considered gain ranges
- Dynamic range large enough
  - → Acceptable saturation probability
    - Example only to give an idea →
  - → Acceptable loss of small charges
    - Low charge cluster members
    - Charges generated at “low end” of distributions



Targeted requirements for CyMBaL

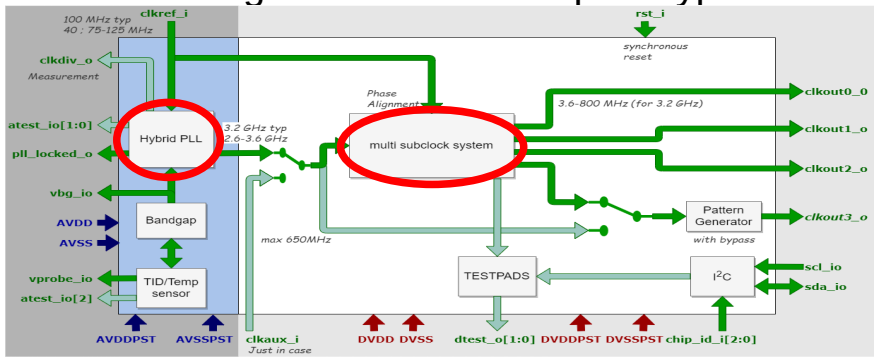


- Signal : 30 fC
  - → Detector gain of ~8 000
- Max / signal : ~10
  - → CSA range : 300 fC
    - Saturation probability ~1 / 1000
      - @ 10 kHz hit rate : ~ 100 ms
- Signal / threshold : ~10
  - → Threshold : 3 fC → ~100 eV
    - Assume charges are evenly distributed among all cluster channels but the channel with Max
      - Cluster size of 4
      - 65% of charges going to a single channel : ~19.5 fC
      - Others get ~5.2 fC > 3 fC threshold
- Threshold / noise : 6
  - → Noise : 0.5 fC
    - ENC: 3 100 e- – compatible with the envisaged detector capacitances
- Working point will be refined with better knowledge of physics / detector / electronics
  - → Configurable flexible very frontend accommodates changes

PRISME side project

- Specific budget from EIC R&D project support
- PRISME prototype to test PLL block + service blocks (bandgap, biases, I2C, I/O links,...), partly from CERN
- 4 programmable clock outputs with individual frequency and phase tuning
- Prototype submitted in July 2023, just arrived, in packaging process

Design of the PRISME prototype



Scheme from C. Flouzat

STRUCTURE OF DATA OUTPUT

Type of output packets

- Packets with different kinds of data
- Packet identification by type, numbering and optionally timestamps
- Each packet buffered and transmitted through one of the Gbit/s links

Physics data packets

- Header + ADC sample values + reconstructed values
- Includes timestamps, chip address, channel numbers, possibly flags
- Sample data structure channel by channel
- Detail of format under finalization

Calibration data packets

- Same format as physics packets + type of calibration data

Information packets

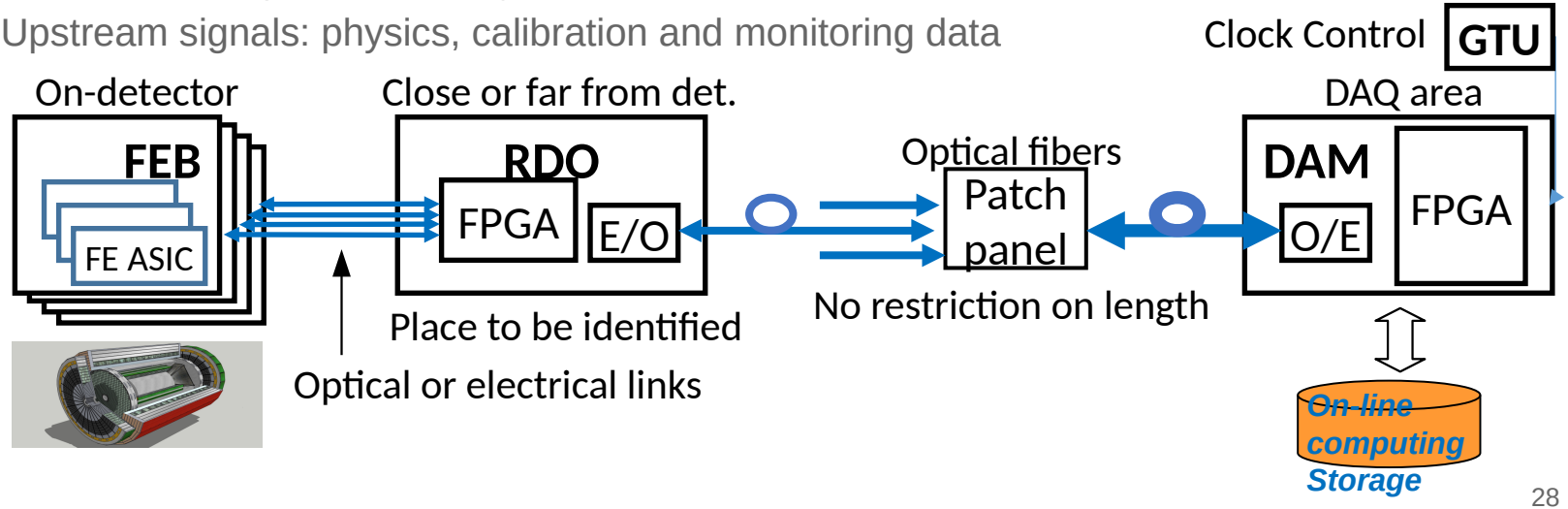
- Carry information data: ASIC configuration, slow-control feedback, environmental informations, channel counting rates, etc...

Error packets

INTEGRATION IN THE EPIC DAQ SYSTEM

EPIC data acquisition chain

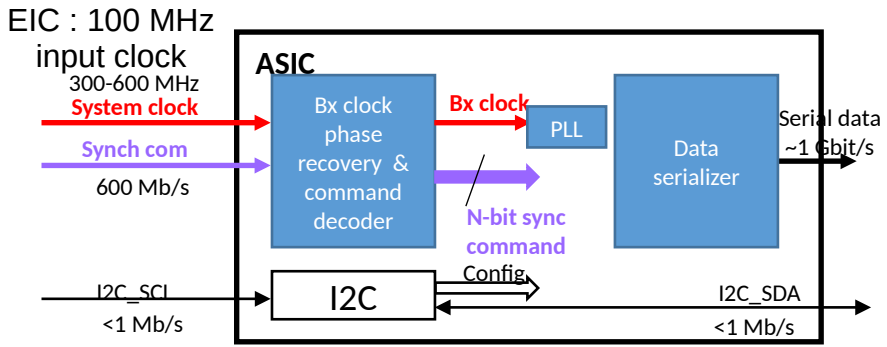
- FEB: frontend boards carrying readout ASICs, specific to sub-detectors
- RDO: readout module, 1st data aggregation, clock and control dispatch, common design framework with adaptations between sub-detectors
- DAM: data aggregation module, interface with computing and global timing and control unit, common for all sub-detectors
- Downstream signals: clock, synchronous commands, slow-control
- Upstream signals: physics, calibration and monitoring data



CLOCK, FAST COMMAND AND SLOW CONTROL INPUTS

Traditional way

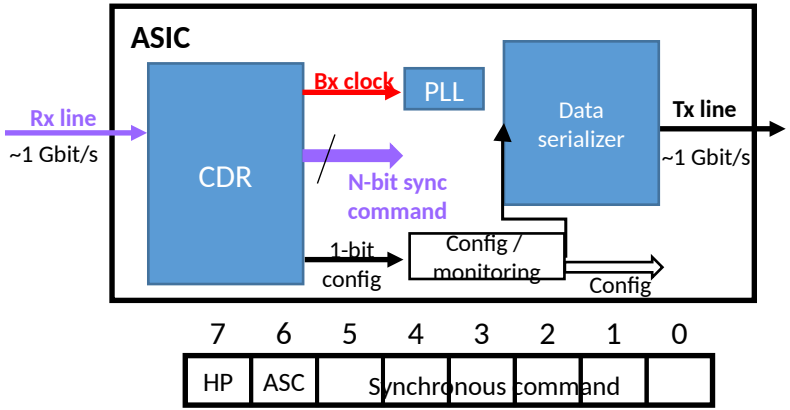
- 1 differential input for clock
- 1 differential input for fast commands
- 1 SDA + SDC I2C input for slow control and configurations
- Will be implemented in SALSA



Single encoded line grouping all inputs

- High speed 1Gb/s differential input which carry clock + fast commands + slow-control
- Internal CDR in SALSA to extract the different parts
- 8 bits every 10 ns (EIC): 6 bits for fast command ID, 1 bit for slow-control, 1 parity bit
- Simplify connectivity: 1 diff input for everything instead of 4
- Slow control output through information packets
- In parallel with the traditional way

Schemes from I. Mandjavidze



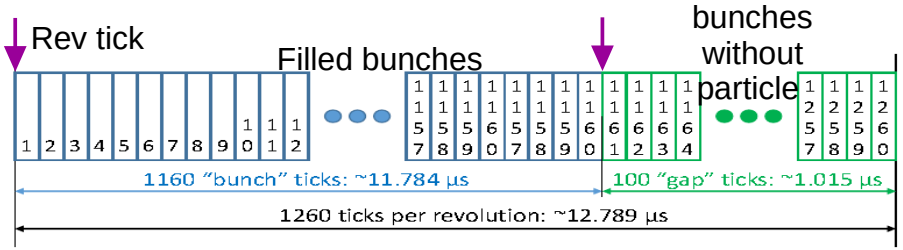
SALSA SYNCHRONOUS COMMANDS, PRELIMINARY VERSION

Context

- Commands received from DAQ in synchronization with system clock (98.5 MHz) on 6 bits
- Can be received at each clock with embedded signals, but not in case of split signals

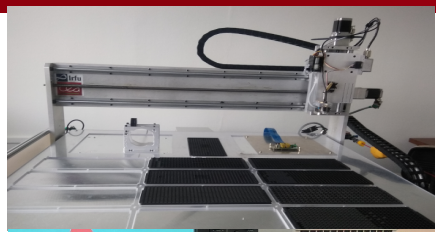
Data taking management commands (those useful for EPIC)

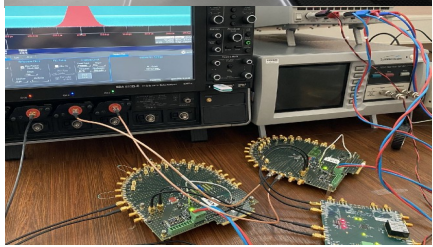
- **T0SYNC**: new time frame → reset packet and clock counters, realign clock phases, and make chip ready to read data in a new time frame
- **STARTREAD**: activate sample data generation in DSP
- **ENDREAD**: deactivate sample data generation in DSP, finish to process remaining samples in FIFOs, then send a specific packet when no more sample is remaining
- **CALIB0...N**: generate calibration data of type N
- **INFO0...N**: generate information packet of type N



QUALITY ASSURANCE

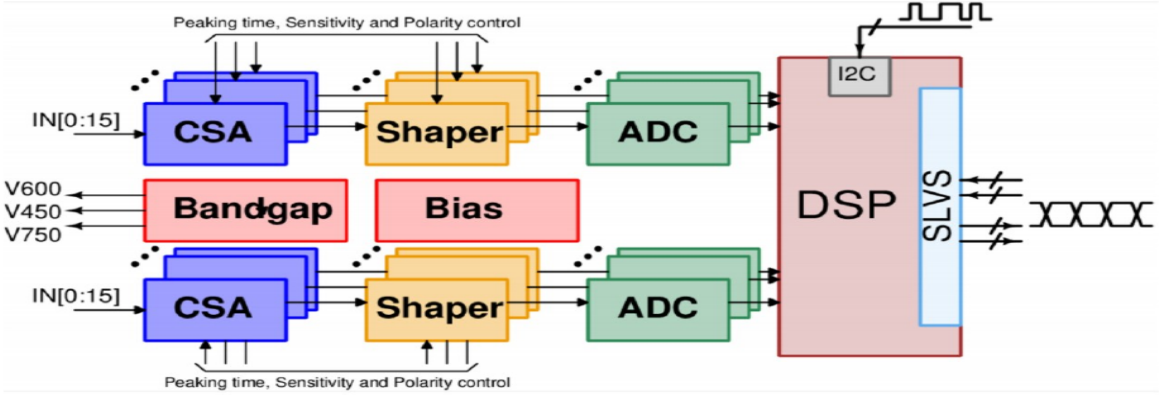
- **Expertise in ASIC development**
  - System-level design, production and commissioning
  - Readout electronics, acquisition software, analysis (CLAS12, T2K TPC, Asakusa tracker, ALICE TPC)
  - Respect of ES&H regulations of host laboratories (BNL, CERN, JLab, J-PARC)
- **Expertise in large scale ASIC production**
  - In-house at Saclay: automated ASIC tester robot, test-benches
  - In industry: development of turn-key test-benches
  - Recent experience: 40k Rafael and 80k Catia ASICs produced and tested for CMS Ph2 upgrade
- **Test equipment used for SALSA development**
  - At Saclay: high-end LeCroy and Textronic oscilloscopes
  - High performance phase noise analyzer
  - Low jitter precision clock sources
  - Climate chamber
  - Bonding machine





SAMPA Overview

- TSMC CMOS 130nm, 1.25V technology.
- 32 Channels, Front-end + ADC + DSP.
- Positive and negative polarities with 2 analog front-end modes:
  - 20 or 30 mV/fC with 160 ns shaping time.(Sensor Cap: 12 - 25 pF)
  - 4 mV/fC with 300 ns shaping time. (Sensor Cap: 40 - 80 pF)
- ADC: 10-bit resolution, up to 18.5 MSPS.



SAMPA Block Diagram

A new SAMPA version with 20/30 mV/fC and 160/80 ns shaping time was later designed, tested on silicon and it is presently available.

Parameter	AFTER	AGET	DREAM
Polarity of detector signal	Negative or Positive	Negative or Positive	Negative or Positive
Number of channels	72	64	64
External Preamplifier	No	Yes; access to the filter or SCA inputs	Yes; access to the filter or SCA inputs
Charge measurement			
Input dynamic range/gain	120 fC; 240 fC; 360 fC; 600 fC	120 fC; 240 fC; 1 pC; 10 pC /channel	50 fC; 100 fC; 200 fC; 600 fC /channel
Gain v.s Cdet (200pF)			
200 fC; tp = 230 ns	- 13%	- 13%	-0,9%
Sampling			
Peaking time value	100 ns to 2 µs (16 values)	50 ns to 1 µs (16 values) (ASTRE : 8µs)	50 ns to 900 ns (16 values)
Number of SCA Time bins	511	512	512
Sampling Frequency (WCk)	1 MHz to 100 MHz	1 MHz to 100 MHz	1 MHz to 50 MHz
Triggering			
Discriminator solution	No	Leading edge	Leading edge
HIT signal		OR of the 64 discri. outputs in LVDS level	OR of the 64 discri. outputs in LVDS level; 8 multiplicity levels
Threshold Range		5% or 17.5% of the dynamic range	5% or 17.5% of the dynamic range
Threshold value		(3-bit + polarity bit) common DAC + 4-bit DAC / channel	(7-bit + polarity bit) DAC common to all channels
Readout			
Readout frequency	20 MHz	25 MHz	Up to 20 MHz
Channel Readout mode	all channels	All, hit or selected	all channels
SCA cell Readout mode	all	1 to 512	Triggered columns only
Trigger rate			Up to 20kHz (4 samples read/trigger).
Counting rate	< 0.3 Hz / channel	< 1 kHz / channel	< 50 kHz / channel
Power consumption	< 10 mW / channel	< 10 mW / channel	< 10 mW / channel
Status	Production	Production	Production
Noise 120 fC; 200 ns peaking time	370 e- + 14.6 e- / pF (measured)	580 e- + 9 e- / pF (measured)	
Noise 200 fC; 200 ns peaking time	700 e- + 8.5 e- / pF (measured)		610 e- + 9 e- / pF (measured)
Electronics	T2K (AFTER + FEC + FEM) AFTER + FEC + evaluation kit AFTER + FEC + STUC AFTERSED	GET AGET + AsAd + rCoBo FEMINOS	DREAM + FEU + SSP DREAM + FEU + TCM