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SALSA: a new versatile readout ASIC for MPGD detectors

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The Sao Paulo University and the CEA Saclay IRFU teams are developing a new readout ASIC for MPGD detectors, named SALSA. This ASIC is meant to be versatile and adapted to different kinds of MPGD applications like tracking, time projection chambers or photon detection. This 64-channel chip, designed in the TSMC 65nm technology, will integrate preamplifier and shaper frontends with 12-bit per channel ADC able to reach 50 MS/s sampling rate. The frontend part will be able to manage large capacitance readout electrodes up to 1 nF, with four configurable amplitude ranges from 0-50 fC to 0-5 pC, and 12 peaking times up to 500 ns. An integrated data processing block will take in charge baseline correction, zero-suppression and feature extraction before to format the data in packets to be transmitted by up to four gigabit links.

The SALSA project was launched in 2020 in the framework of the EIC project, and has produced in 2022-23 different prototypes to evaluate a first version of the frontend and ADC blocks, as well as the phase-locked loop (PLL) block that generates internal clocks. A larger prototype, SALSA1, is currently under production to validate and measure the performance of the frontend-ADC chain, as well as of some service blocks. The SALSA2 prototype, which will include all the data processing functionalities of the final ASIC but with a limited number of channels, is presently under development. It will be submitted for production within the first months of 2025. The final pre-series prototype is expected during 2026, for a series production in 2027. After a presentation of the project and the target specifications of the ASIC, its architecture and its features will be detailed, and results will be given from the tests of the prototypes. The next major steps of the project will be then described.

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