清華大學工程物理系
Department of Engineering Physics, Tsinghua University

The 8th International Conference on Micro-Pattern Gaseous Detectors

Development of Readout Electronics for CEPC TPC

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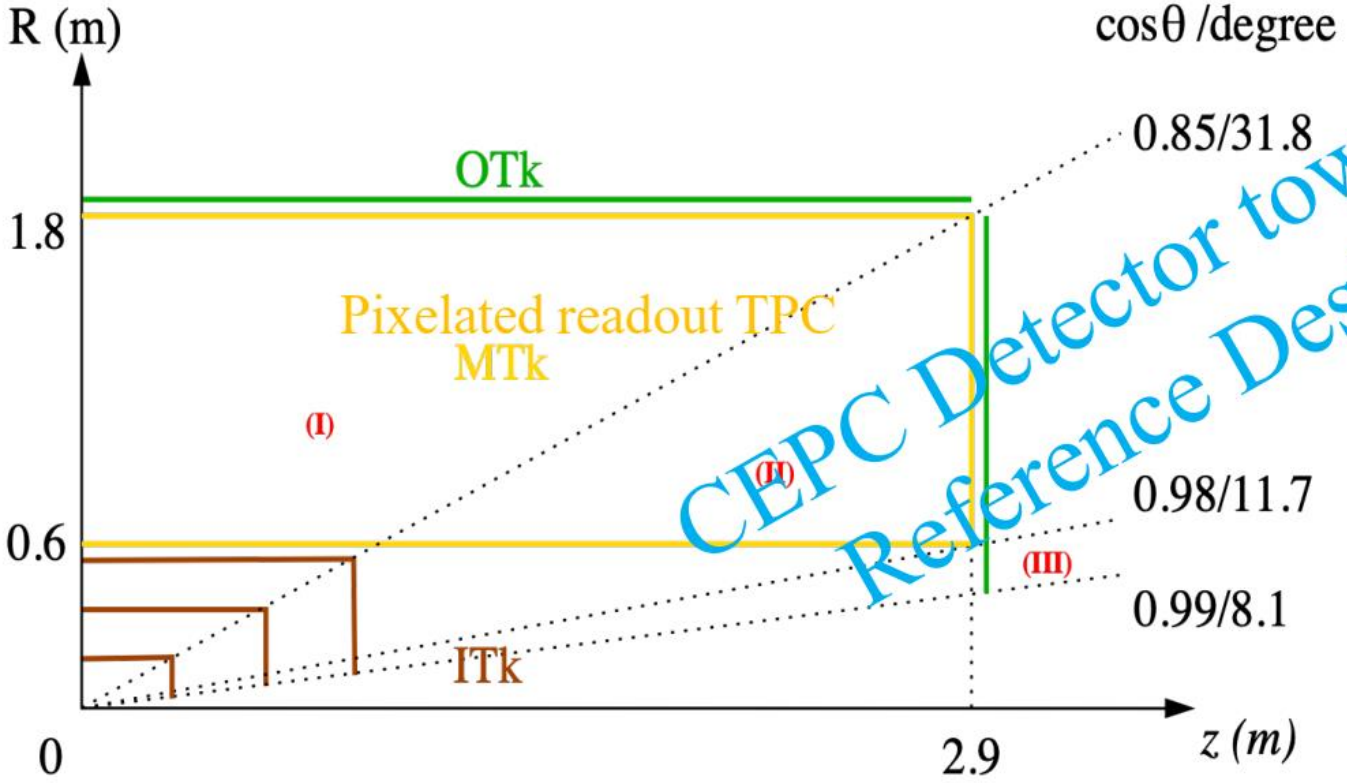
Oct. 14 – 18 2024 USTC Hefei, China

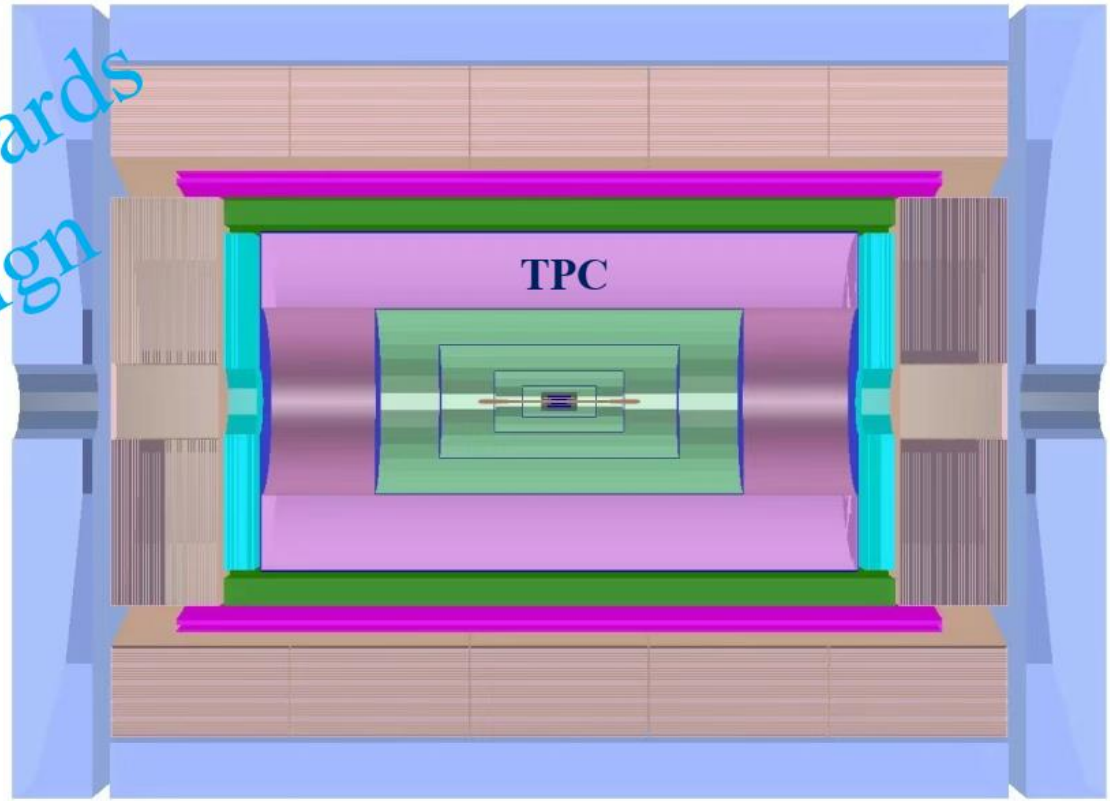
OUTLINES

01 | TPC and its readout electronics

CEPC TPC

- CEPC track detector system: silicon combined with gaseous chamber as the tracker and PID
- TPC is as the **baseline** main tracker in CEPC ref-TDR, achieving good **momentum resolution** and **particle identification**

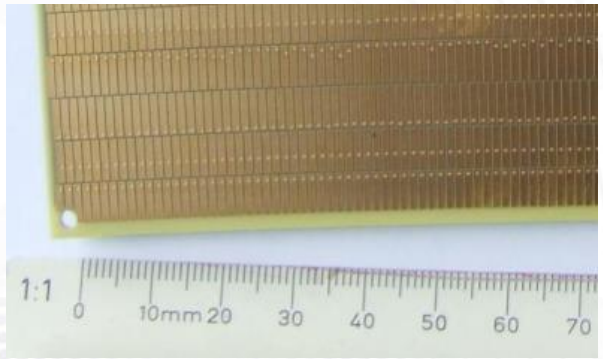




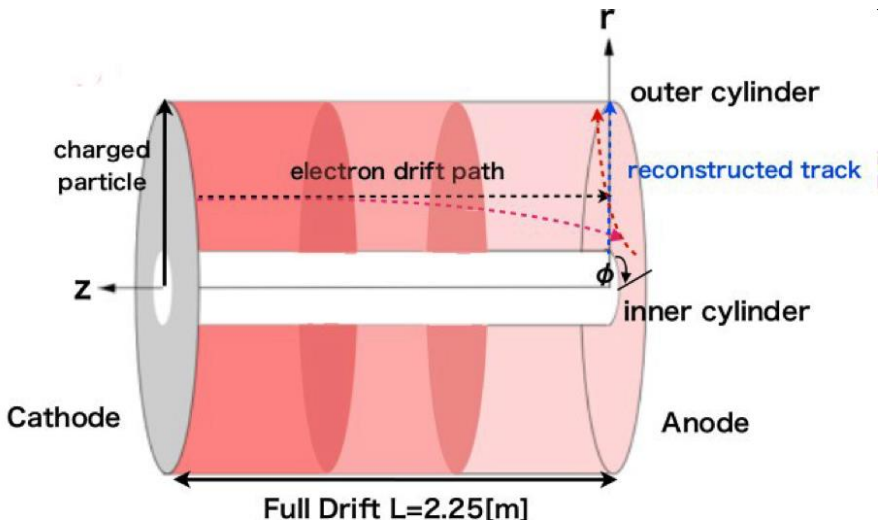
CEPC Detector towards Reference Design

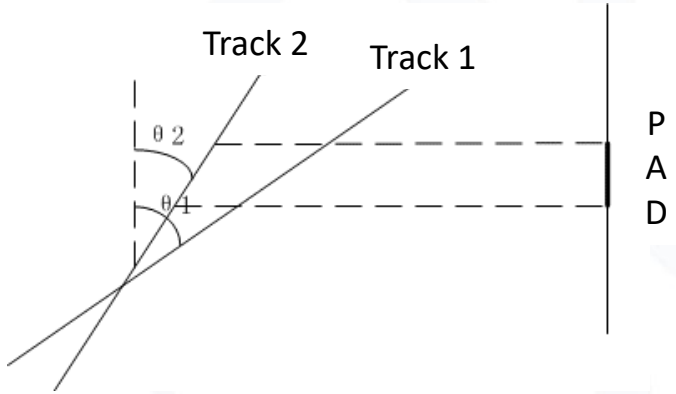
Pad Readout for TPC as in ILC

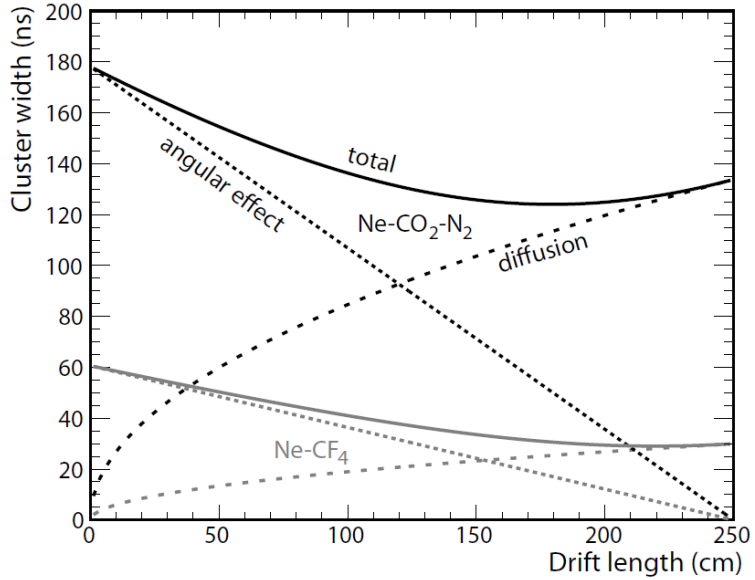
- Signals induced in readout pads **in mm²**: ~1mm x 6mm
  - More parallel to the collection plane ~ short duration
  - More perpendicular to the collection plane ~ long duration
- **Ballistic Loss** vs signal pileup
- Acquire amplitude and time information at the same time



Waveform Sampling

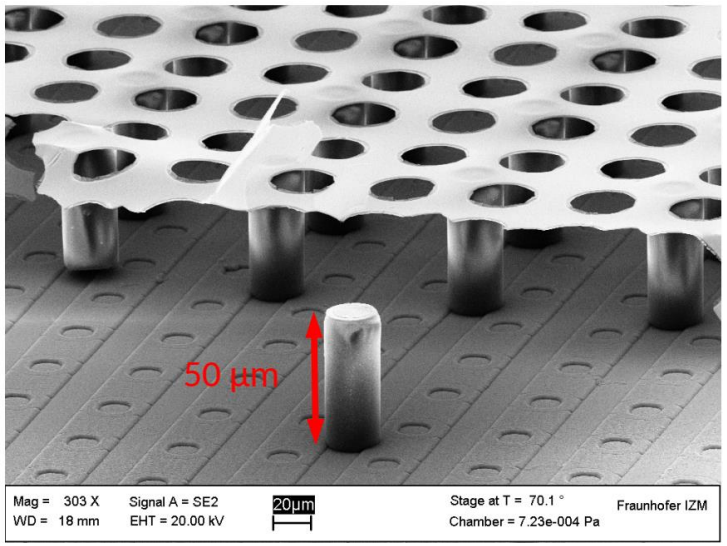


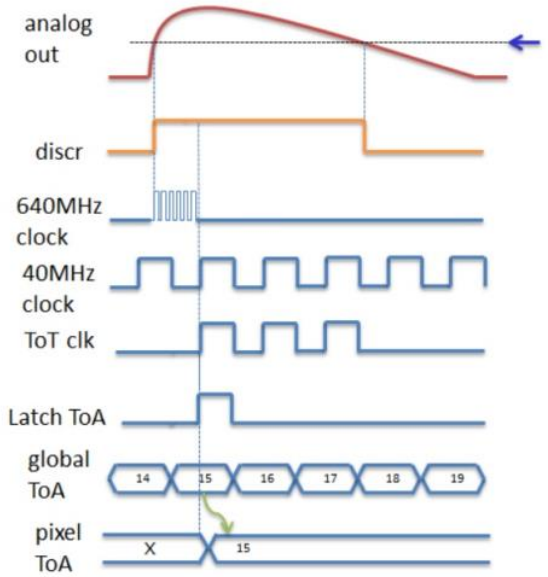


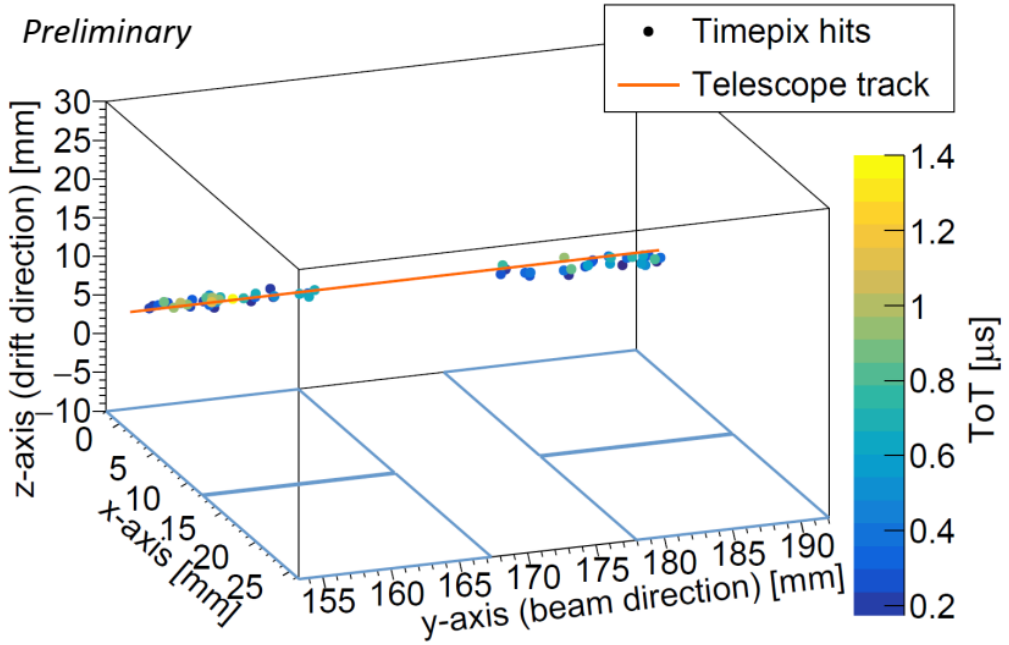


Pixel readout for TPC

- Combination of a pixel ASIC with TPC, e.g., **55 um** using TPX3/4
- The signal duration variation reduces as the pixel size
  - no need for waveform, only charge and arrival timing
- PID improvement: dE/dx → **dN/dx**







02 | Progress on pad readout for TPC

Current ASICs for pad TPC readout

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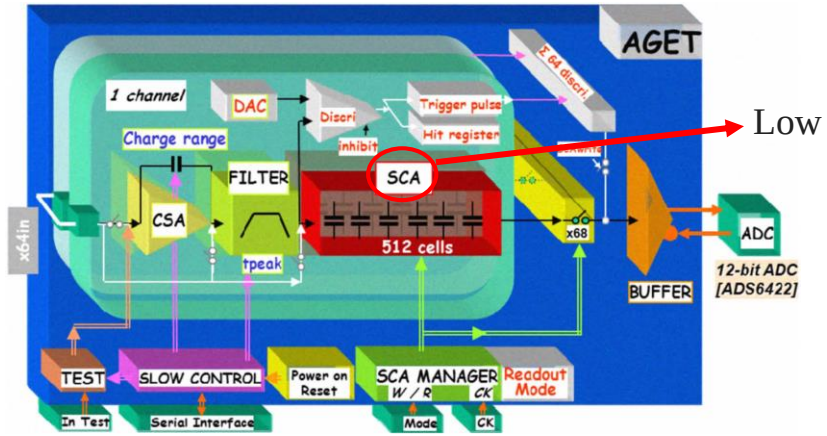
AGET（T2K)

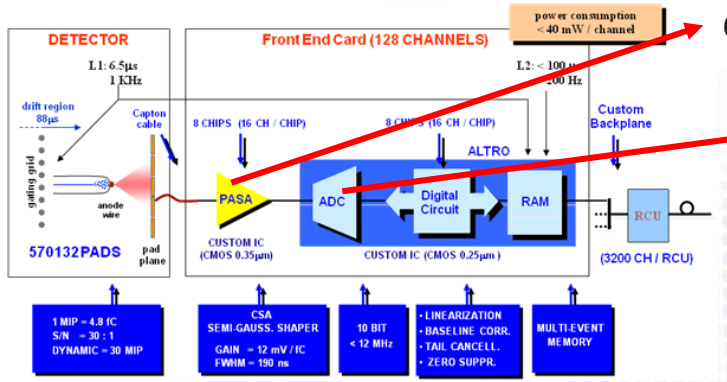
Anvar S, et al. IEEE NSS，2011



Low count rate

PASA+ALTRO（ALICE）

Musa L, et al. IEEE NSS，2003

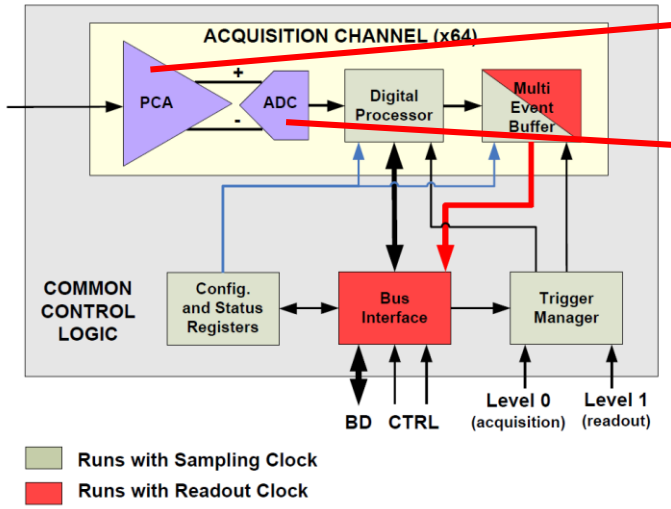


CR-RC^4

Pipeline ADC

Super-ALTRO（ILC）

Aspell P, et al. TNS，2013

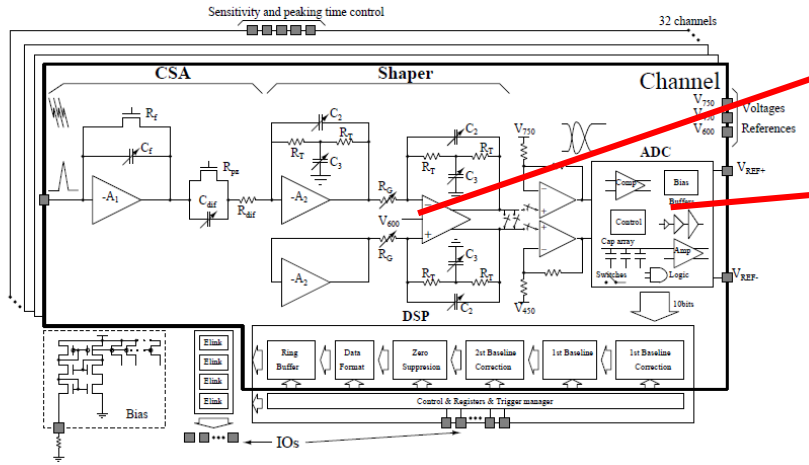


CR-RC^4

Pipeline ADC

SAMPA（ALICE Upgrade）

Barboza, et al. JINST，2016

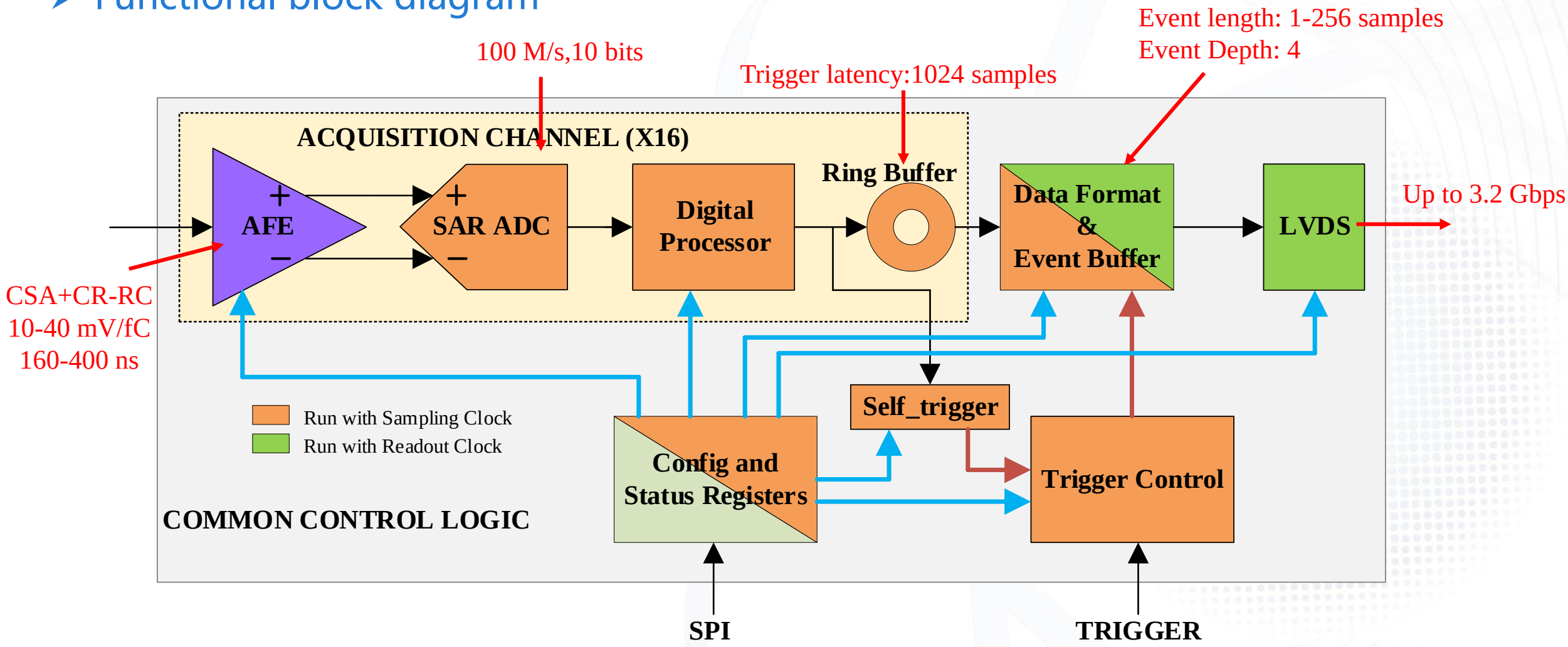


CR-RC^4

SAR ADC

Development of the WASA chip

Functional block diagram



Development of the WASA chip

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➢ Main Specifications

	PASA+ALTRO	Super-ALTRO	SAMPA	WASA
TPC	ALICE	ILC	ALICE upgrade	CEPC
Pad size	4x7.5 mm^2	1x6 mm^2	4x7.5 mm^2	1x6 mm^2
Number of channels	5.7× 10^5	1-2 × 10^6	5.7 × 10^5	2 x×10^6
Detector	MWPC	GEM/MicroMegas	GEM	GEM/MicroMegas
Gain	12 mV/fC	12-27 mV/fC	20/30 mV/fC	10-40 mV/fC
Analog shaper	CR-$(RC)^4$	CR-$(RC)^4$	CR-$(RC)^4$	CR-RC
Peaking time	200 ns	30-120 ns	80/160 ns	160-400 ns
ENC	370+14.6 e/pF	520 e	246+36 e/pF	569+14.8 e/pF
Waveform sampling	Pipeline ADC	Pipeline ADC	SAR ADC	SAR ADC
Sampling rate	10 MHz	40 MHz	10 MHz	10-100 MHz
Sampling accuracy	10 bit	10 bit	10 bit	10 bit
Power consumption of AFE	11.7 mW/ch	10.3 mW/ch	9 mW/ch	1.4 mW/ch
Power consumption of ADC	12.5 mW/ch	33 mW/ch	1.5 mW/ch	0.8 mW/ch@40 MHz
Power consumption of DSP	7.5 mW/ch	4.0 mW/ch	6.5 mW/ch	2.7 mW/ch@40 MHz
Power consumption of all	31.7 mW/ch@10MHz	47.3 mW/ch@40 MHz	17 mW/ch@10 MHz	4.9 mW/ch@40 MHz
CMOS process	250 nm	130 nm	130 nm	65 nm

Some Test Results of the WASA chip

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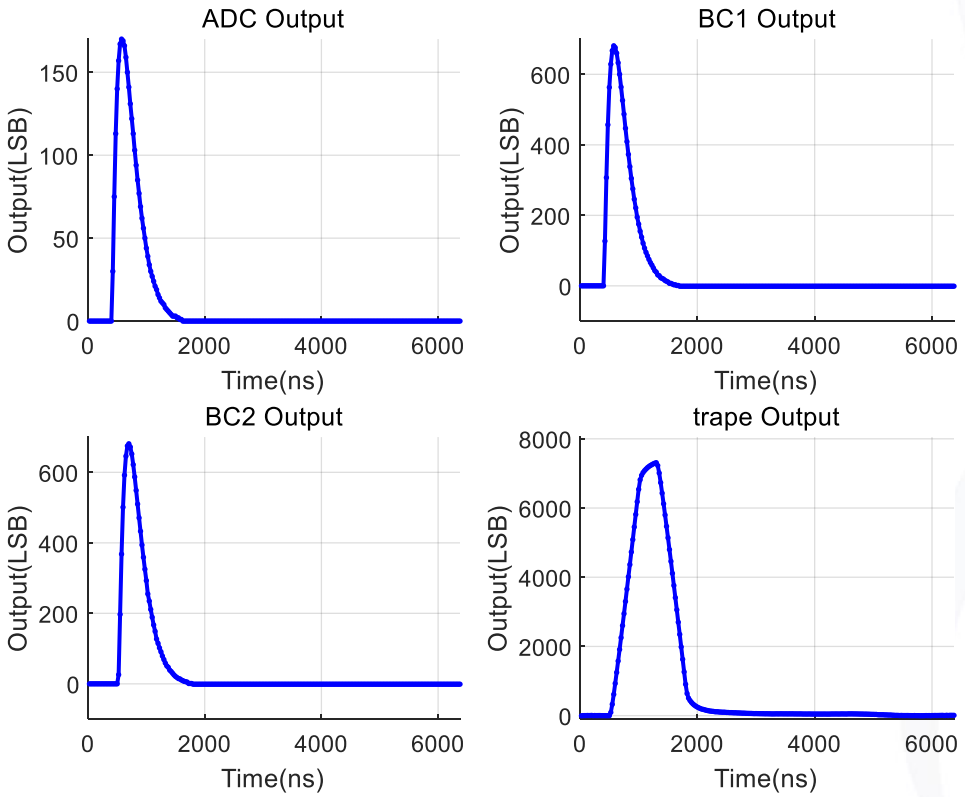
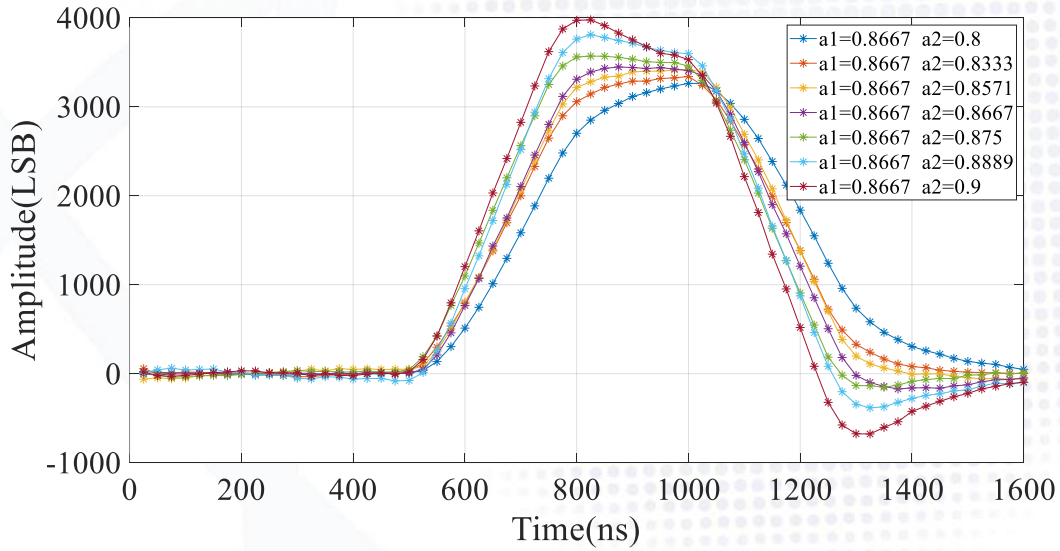
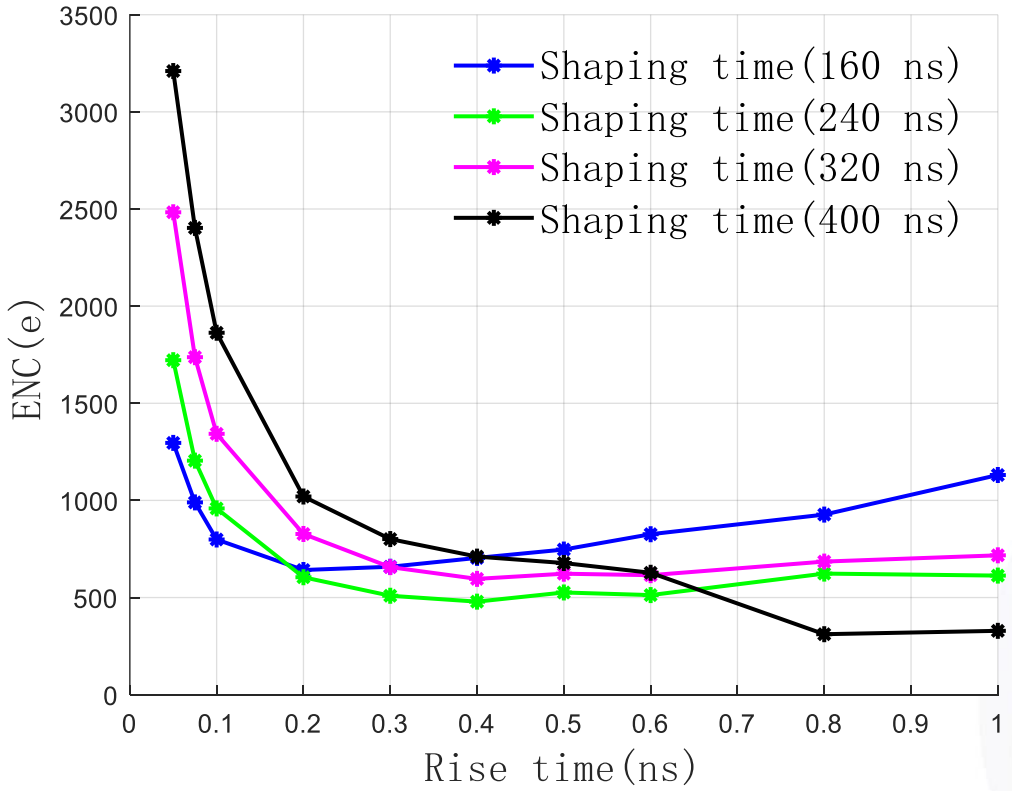
- Response of the digital filters:
  - AFE: gain~10 mV/fC, peaking time~160 ns, Qin=120 fC
  - Sampling rate of ADC: 40 MHz
  - Digital trapezoidal filter : Rise time~600 ns, Flat time 200 ns

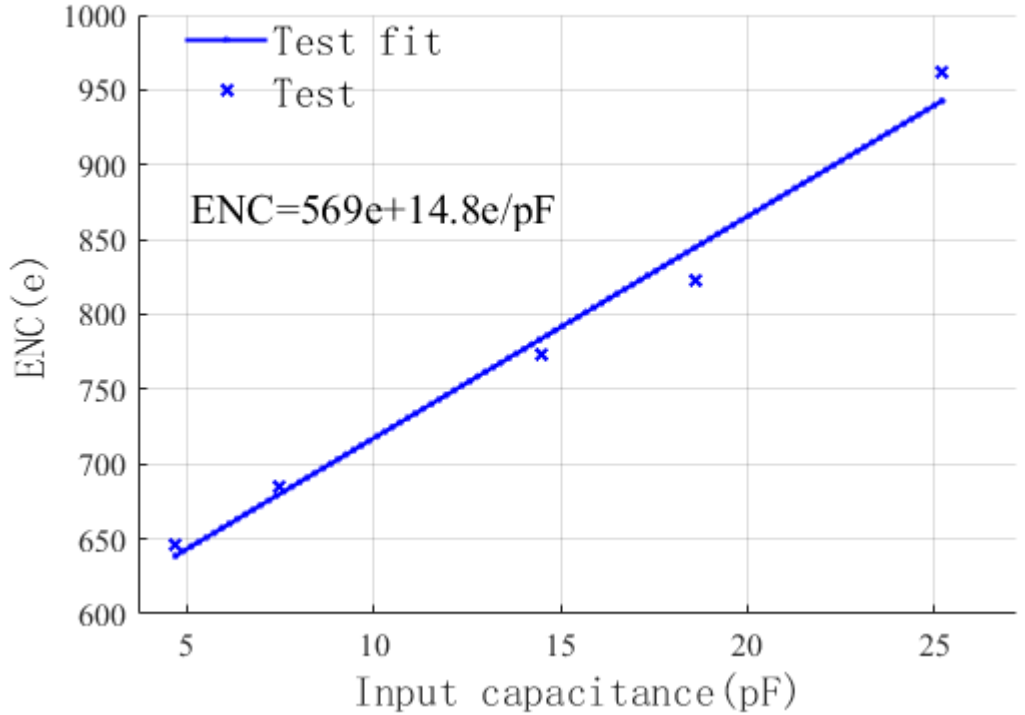




Some Test Results of the WASA chip

- Noise
  - AFE：gain~10 mV/fC，peaking time~160 ns
  - Sampling rate of ADC：40 MHz
  - Digital trapezoidal filter： Flat time 200 ns

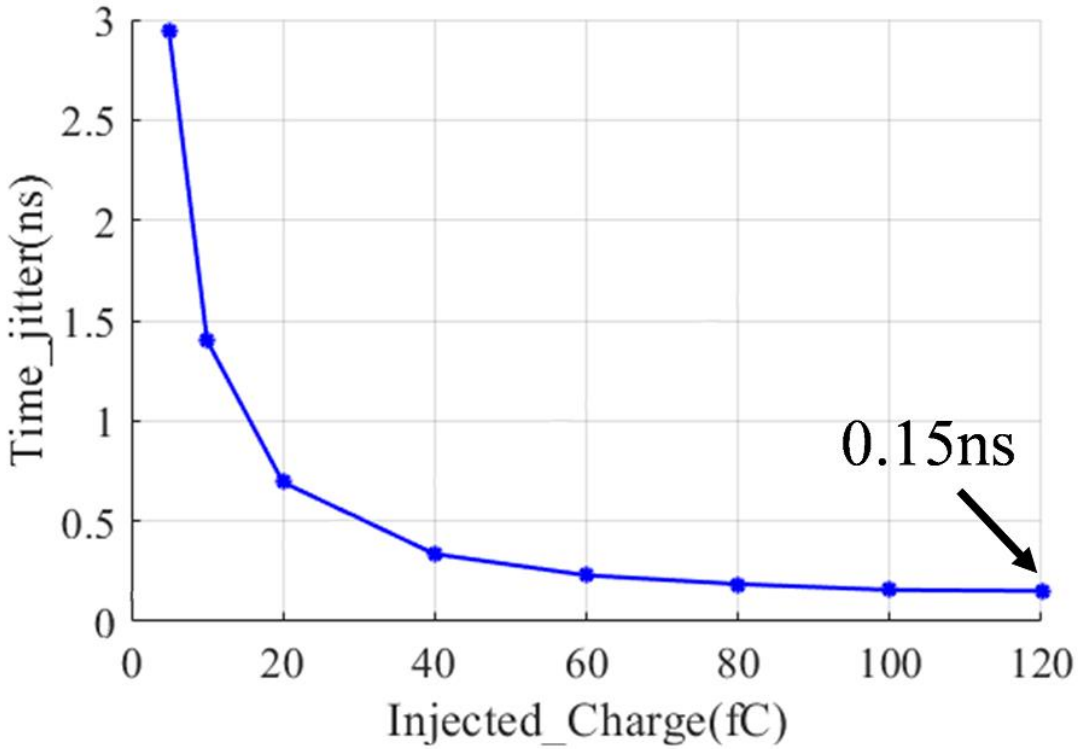


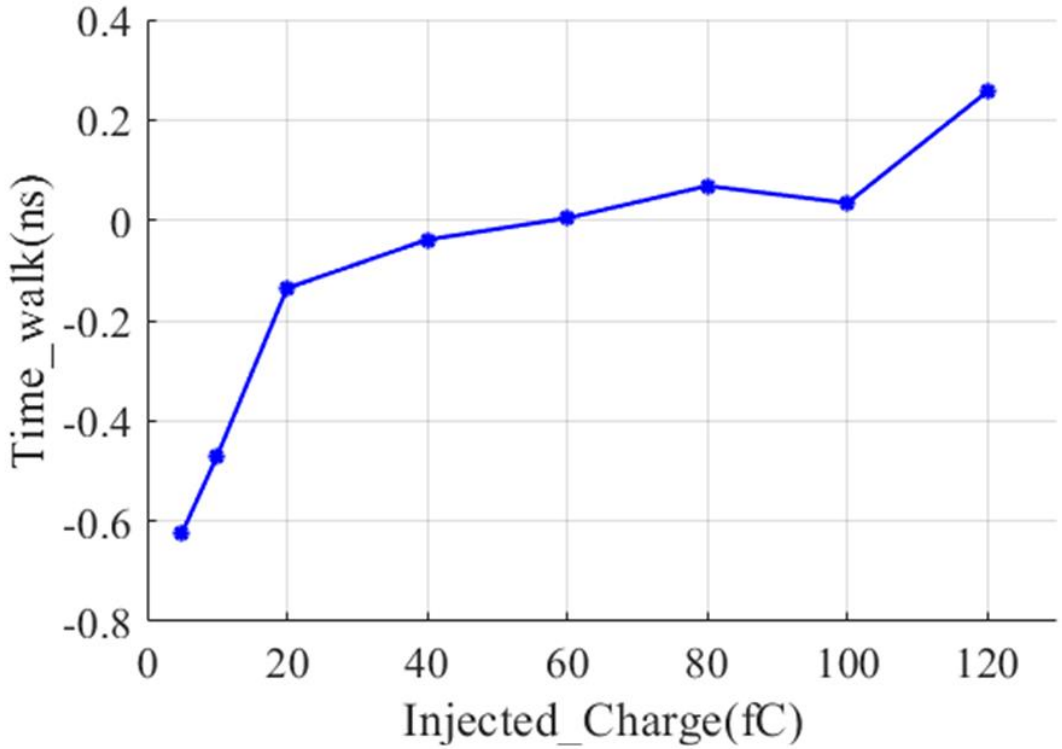


Some Test Results of the WASA chip

- Timing performance
  - AFE：gain~10 mV/fC，peaking time~160 ns
  - Sampling rate of ADC：40 MHz
  - Digital trapezoidal filter： Rise time~600 ns， Flat time 200 ns
  - Timing algorithm: Time center of gravity method

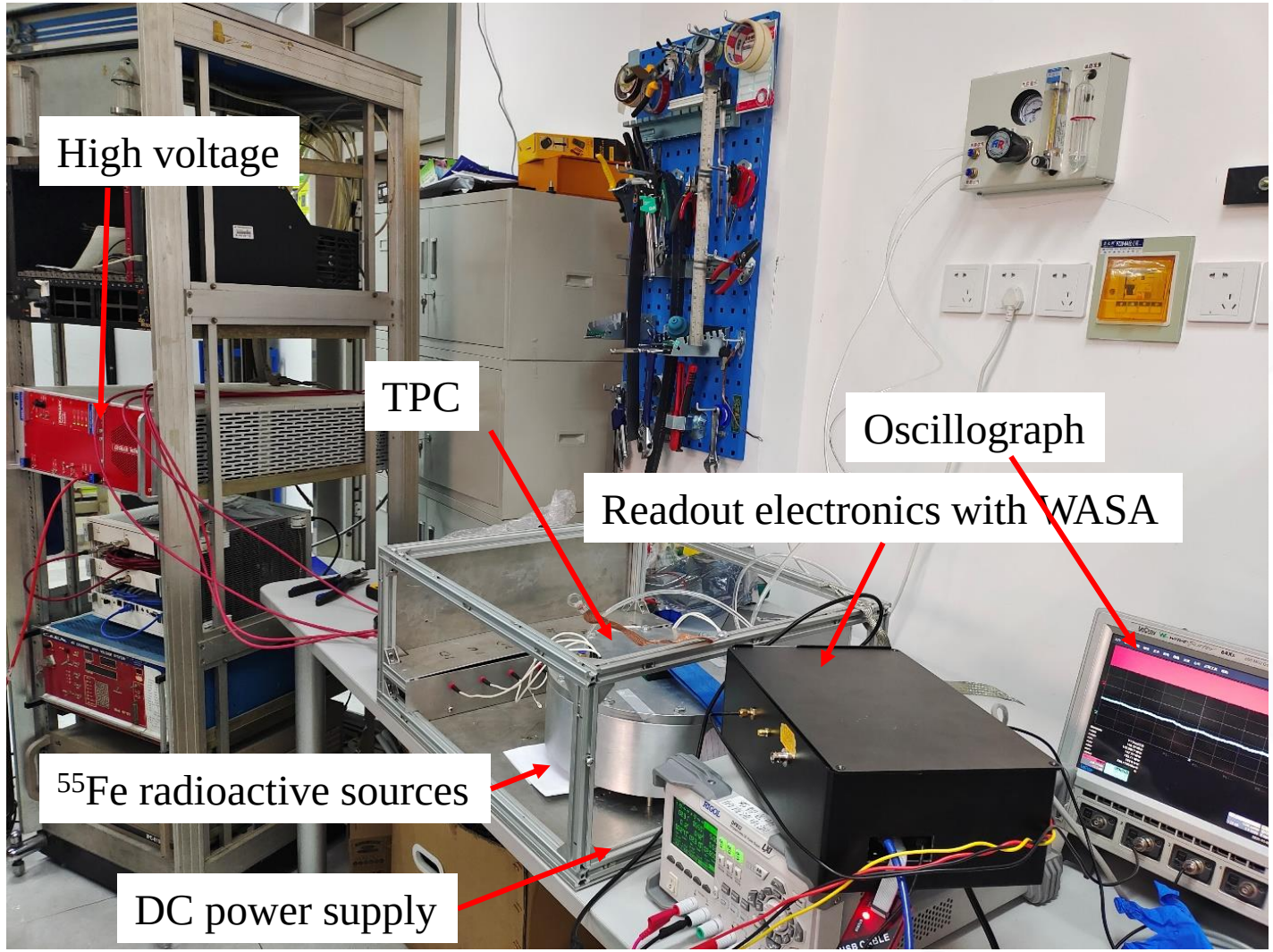
$$Time\ center: t = \frac{\sum t_i \times f(t_i)}{\sum f(t_i)}$$





Some Test Results of the WASA chip

➢ Test with TPC：Fe-55



Working conditions of TPC：

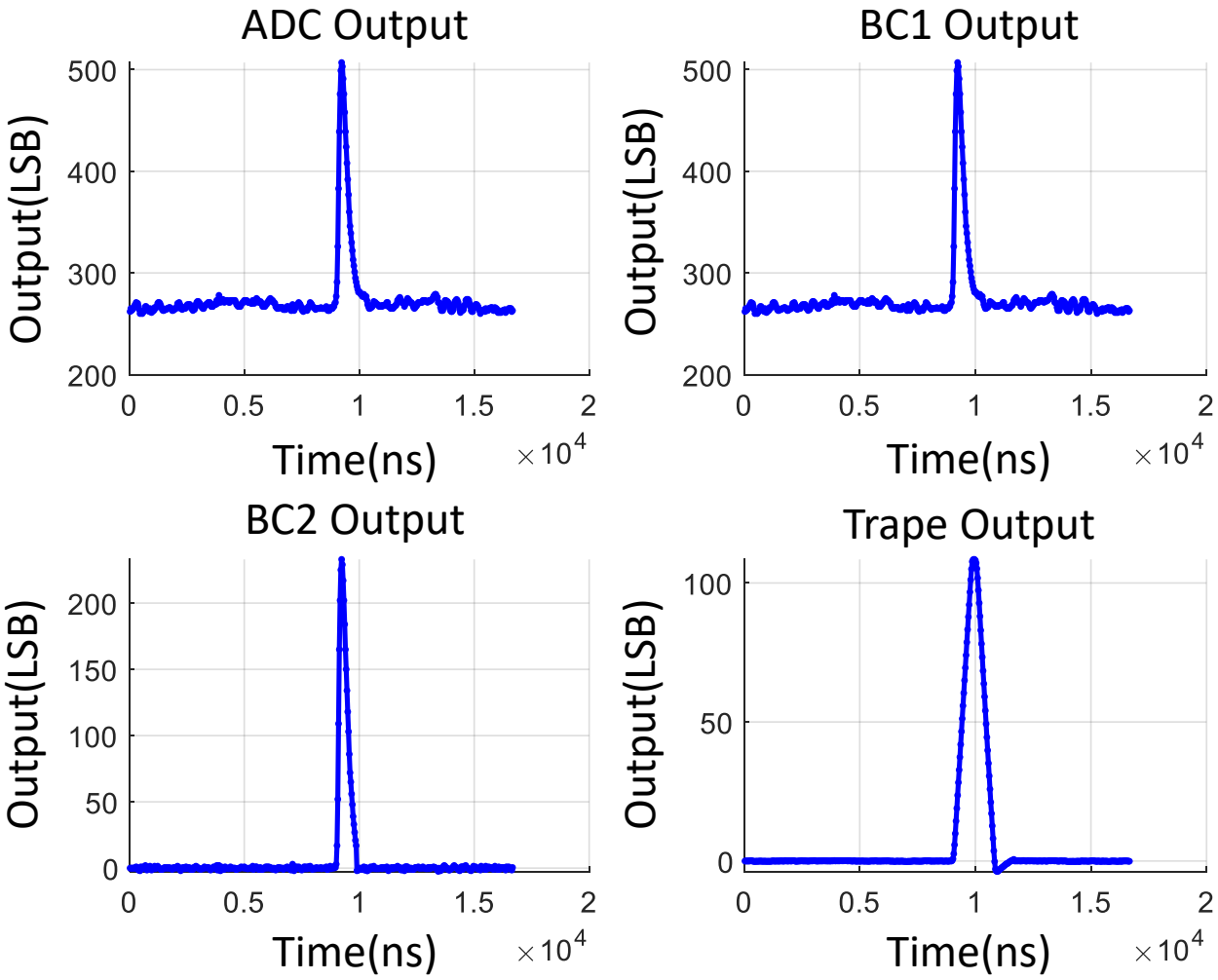
- GEM voltage: 310 V
- Drift electric field：3.23×10^4 V/m
- Gas： T2K ($Ar/CF_4/iC_4H_{10}$ 95/3/2)

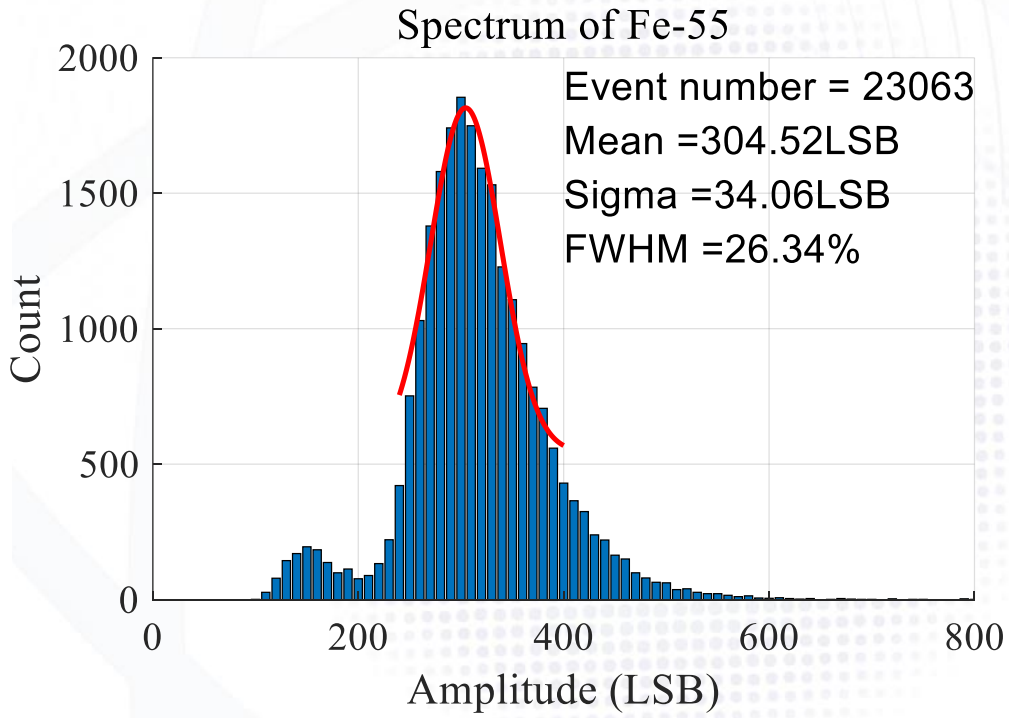
Working conditions of electronics：

- Gain：20 mV/fC
- Sampling rate ： 30 MHz
- Self-triggered mode

Some Test Results of the WASA chip

➢ Transient waveforms and Fe-55 Spectrum





Some Test Results of the WASA chip

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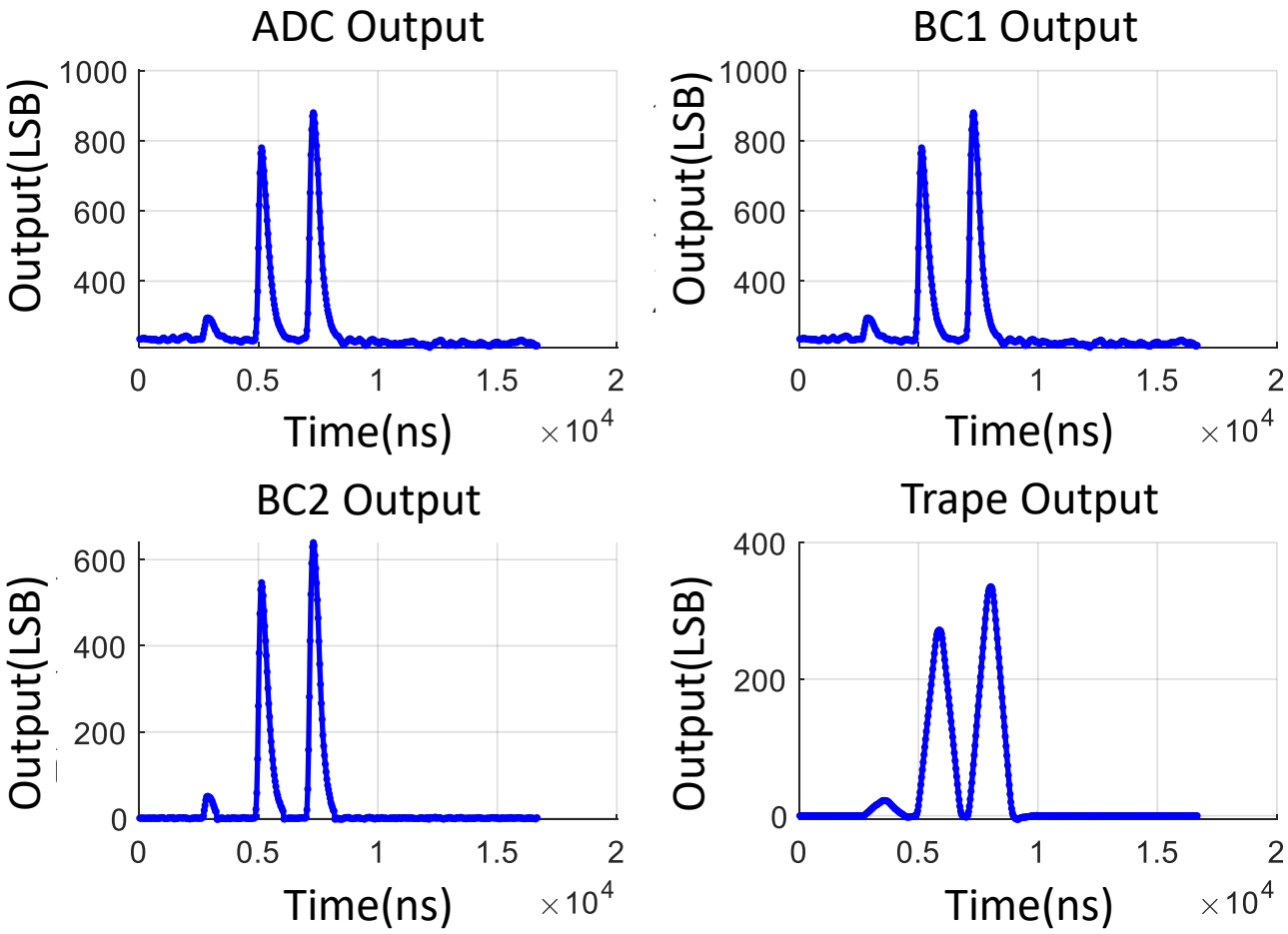
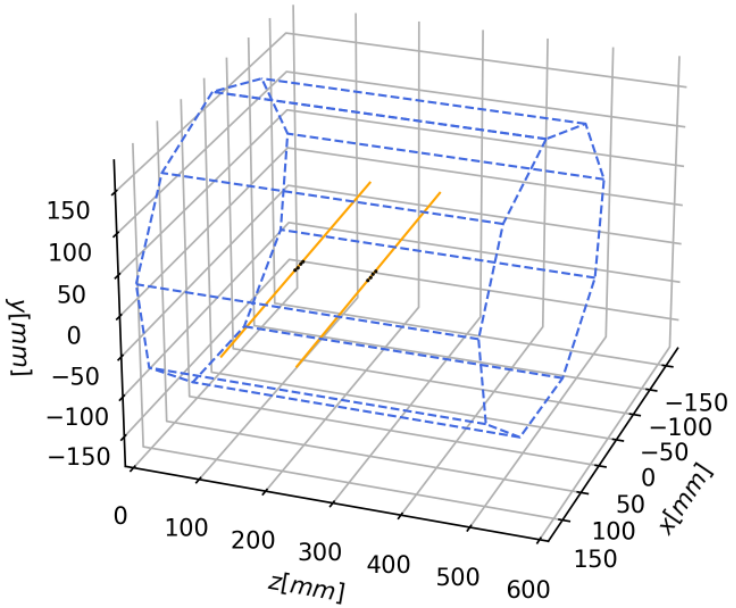
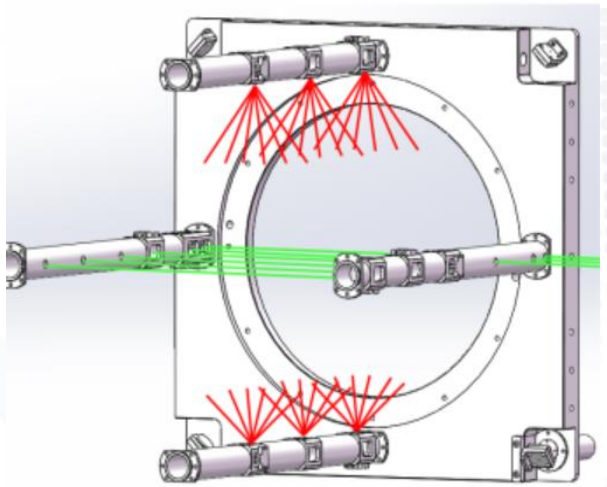
➢ Tracking performance

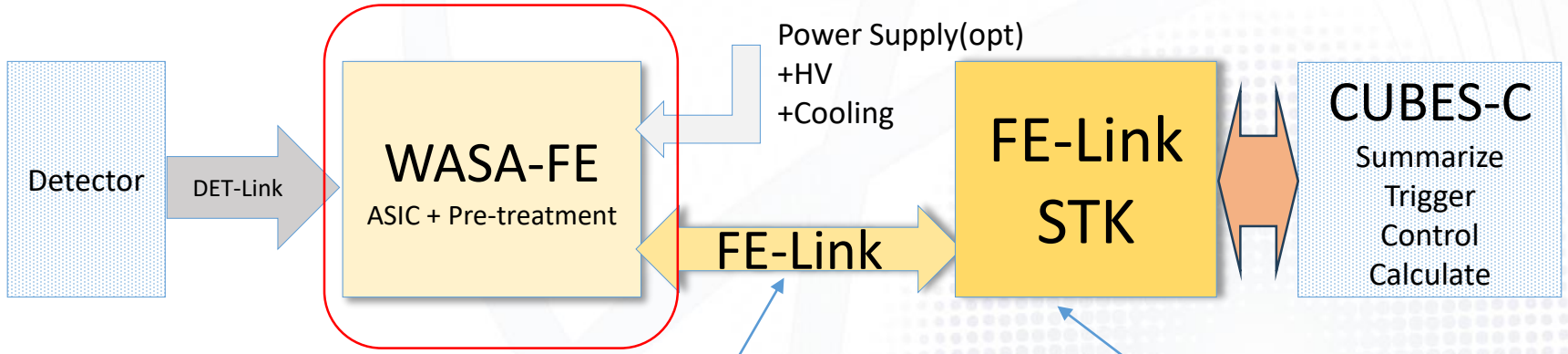


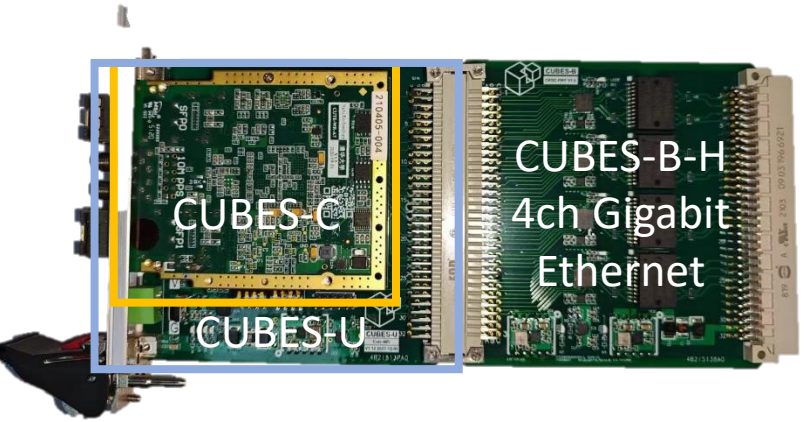




TPC readout electronics system

➢ CUBES：Common Unit Based Electronics System



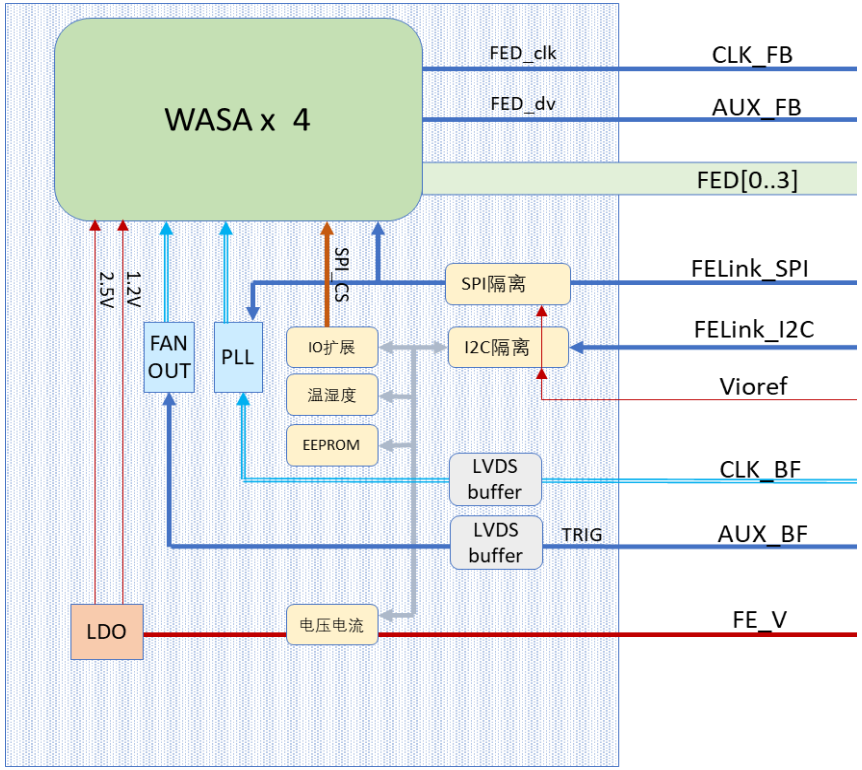


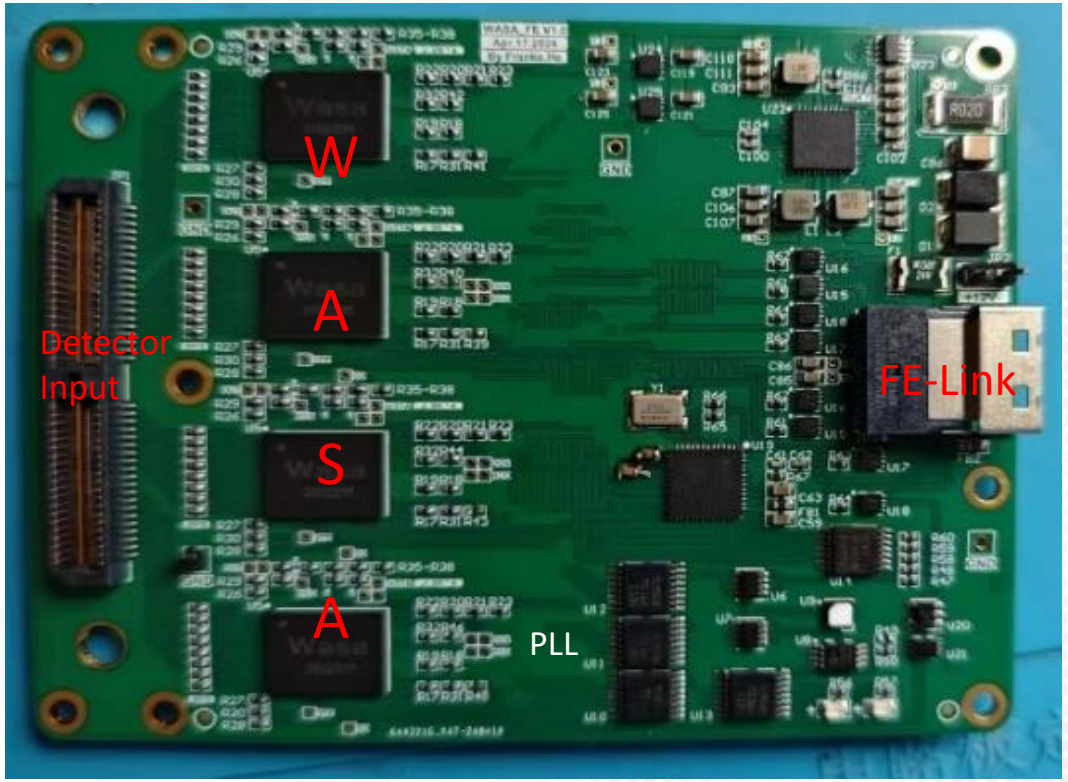
- **Physical channels for ASIC**
  - Data, Clock, Control, Trigger, Power
- **SFF-8654 SlimLine cable assembly**
- **Multiple working modes**
  - Pass-through mode
  - Edge mode
  - Distribution mode

- **Actual connection of WASA-FE and CUBES**
- **3 FE-Links and additional power supply terminals**
- **Line driver & receiver, fan-out**
- **FMC stacked structure**
- **Multiple back-end processing modes**

TPC readout electronics system

➢ WASA-FE prototype





- 4 WASA chip: 64 channels
- Analog input ~ SAMTEC QTE socket
- Onboard PLL CDCM6208~ADC clock and data clock
- DC 12V from FE-Link， DC-DC→LDO→WASA

TPC readout electronics system

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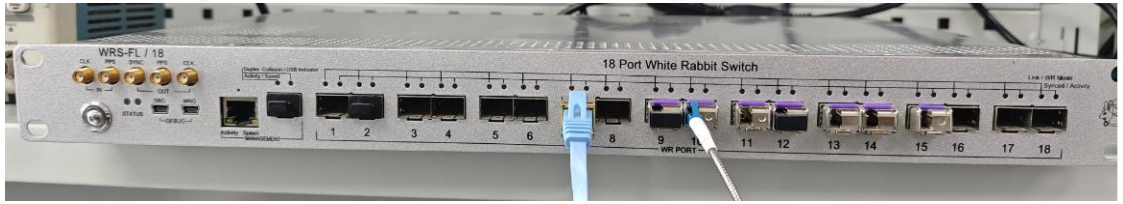
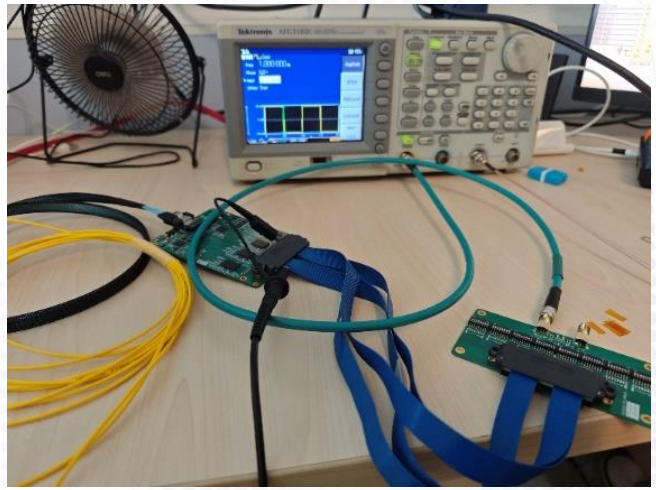
➢ WASA-FE test setup



1 WASA-FE
1 CUTE-WR-A7
1 FELink_STK
1 WRS



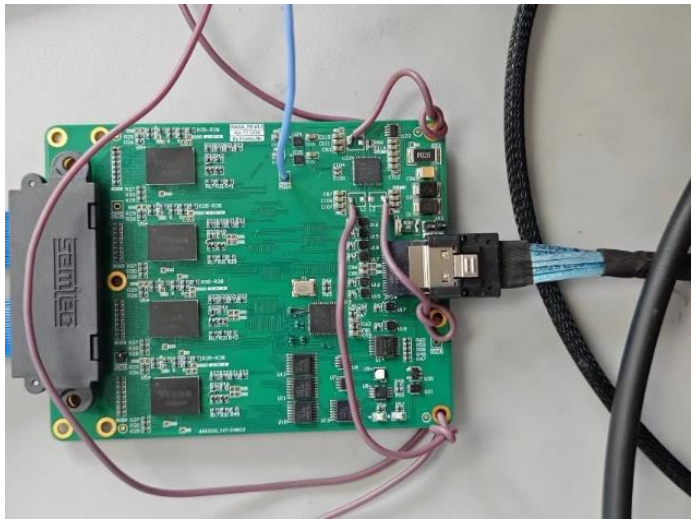
Signal source: The signal generator generates a square wave signal
Signal injection: 1pF capacitor is connected in series at the input
Trigger mode: external trigger

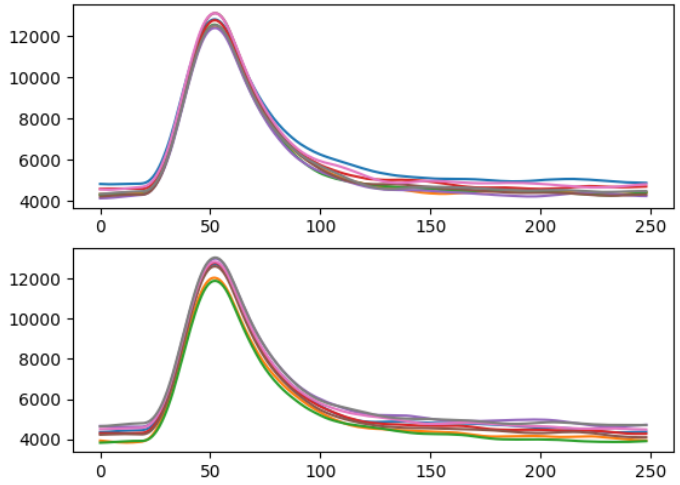
The host computer obtains the data and saves the disk

```
def main():
    hostIP = "192.168.10.10"
    sock = socket.socket(socket.AF_INET, socket.SOCK_STREAM)
    sock.connect((hostIP, 5000))
    print("Link connected!")
    filename = datetime.datetime.now().strftime('%Y_%m_%d_%H_%M_%S')+".dat"
    with open(filename, "wb") as file:
        while True:
            data = sock.recv(2048)
            file.write(data)
            file.flush()
```

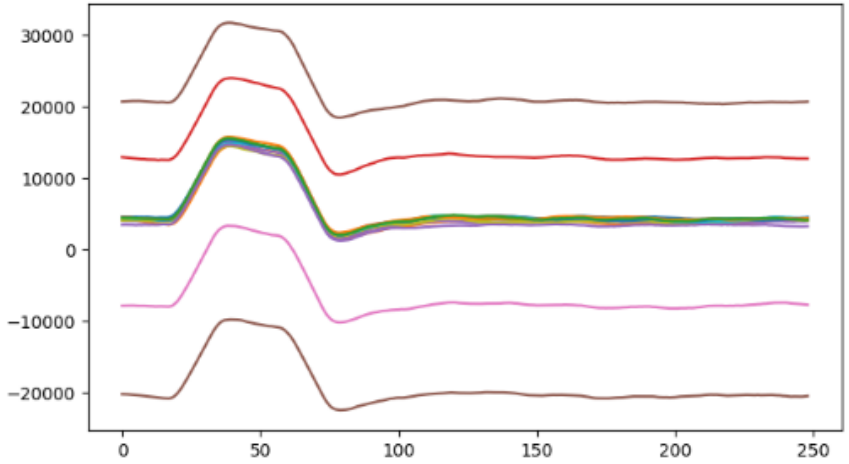
TPC readout electronics system

- WASA-FE test results





CR-RC Output



Digital trapezoidal filter Output

- Ongoing:
  - Engineering run: ~1000 WASA chip
  - More stable WASA-FE boards will be built

03 | Progress on pixel readout for TPC

Why pixel readout for CEPC TPC

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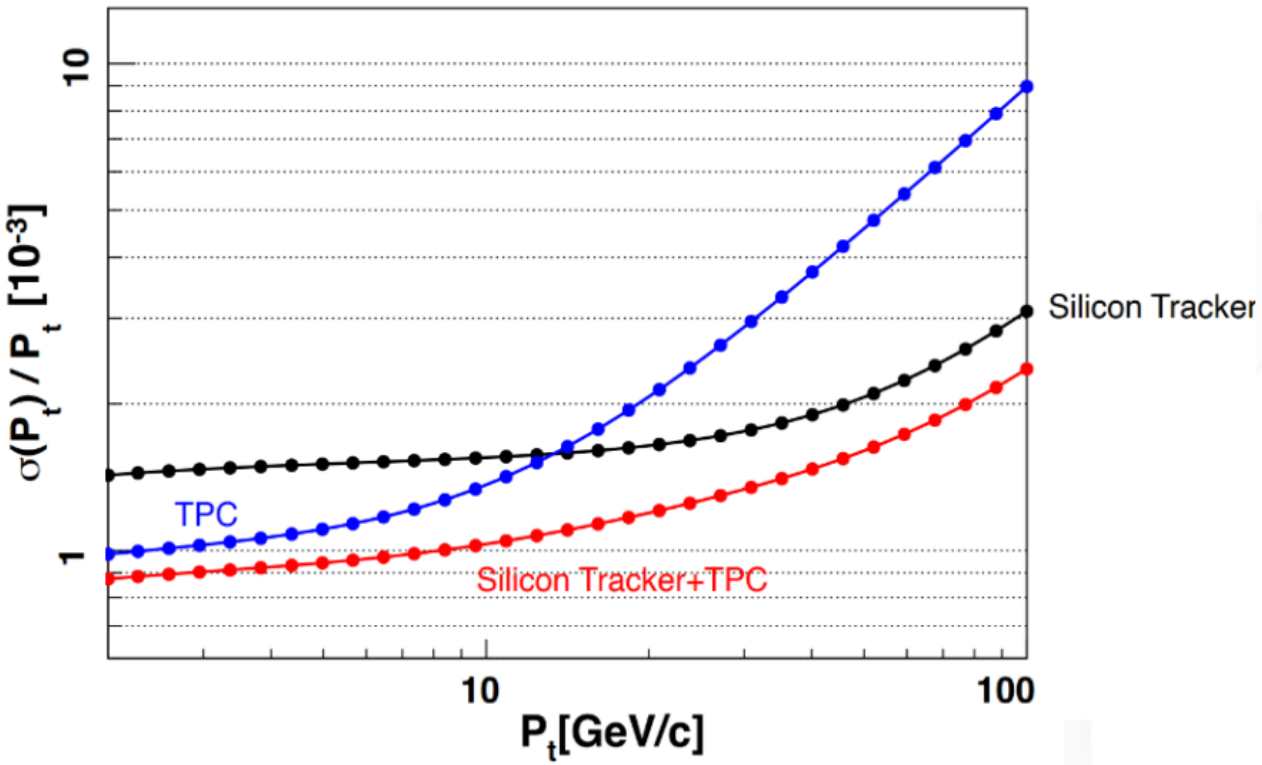
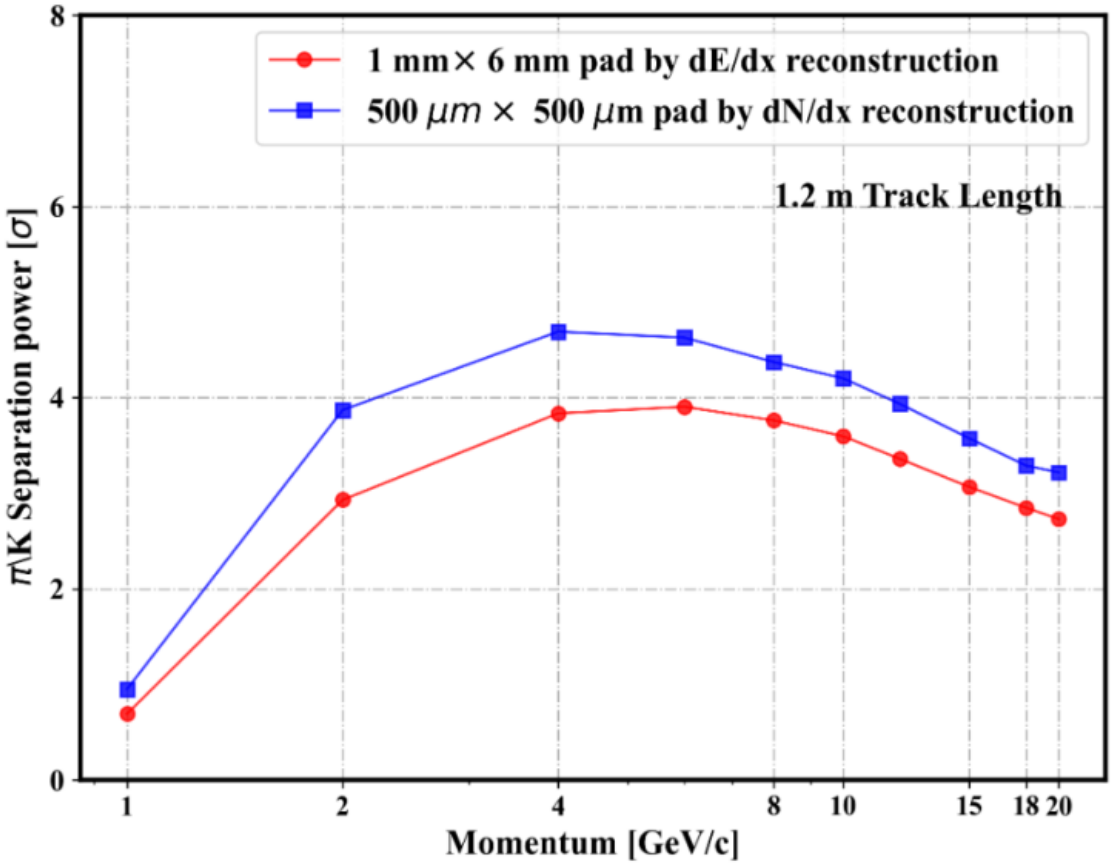
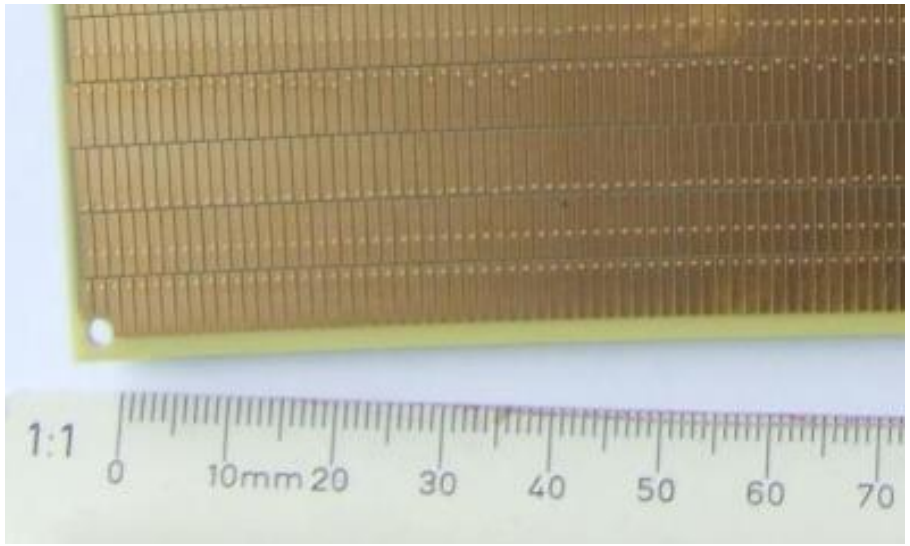
- CEPC： 10-year Higgs → 2-year Z → 1-year W
- PID: dE/dx → dN/dx ~ 3%
- High rate: smaller pixel → lower noise → lower gain → lower ion feedback

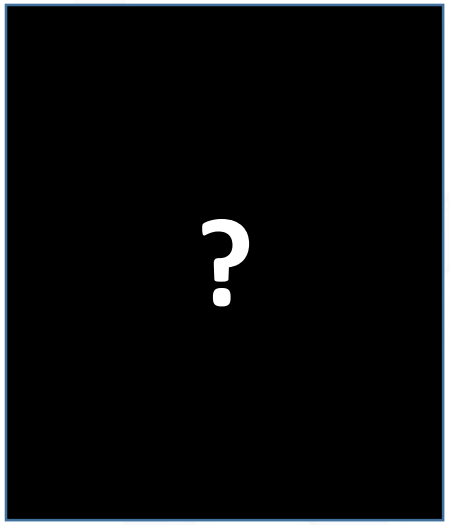


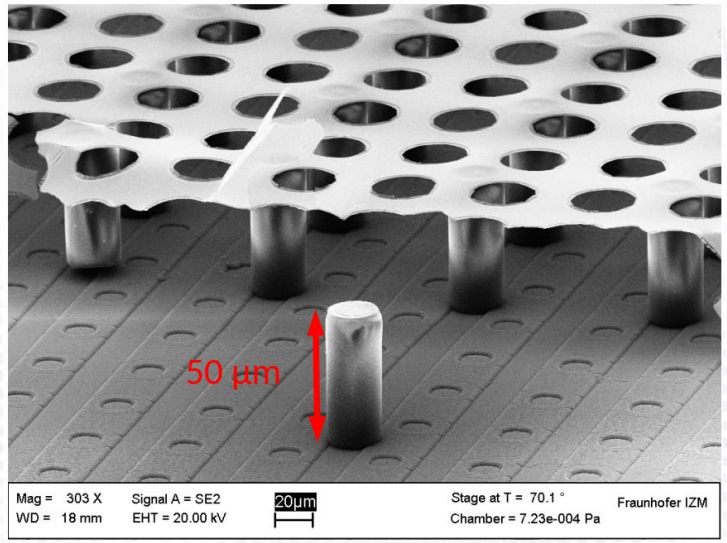


Readout challenging for pixel TPC

- What we have now for large area in ~1m2







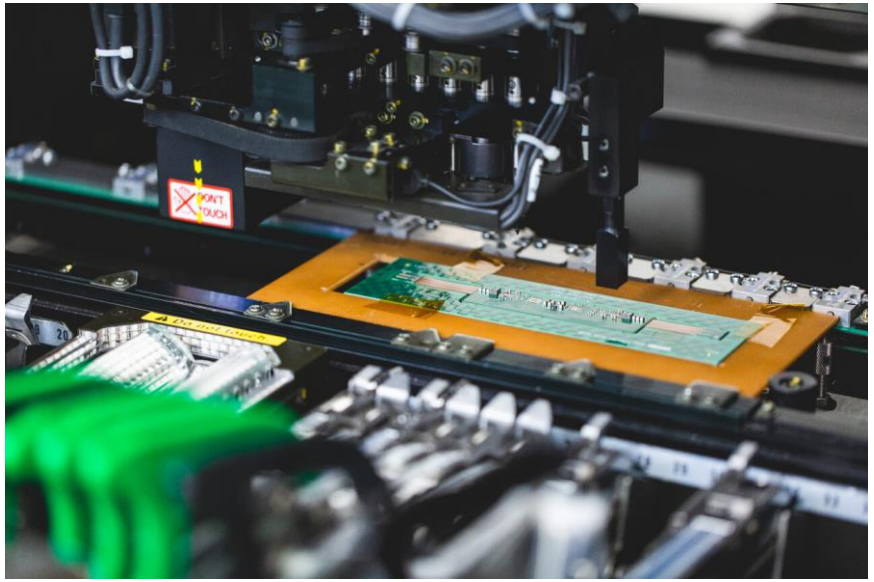
1mm x 6mm

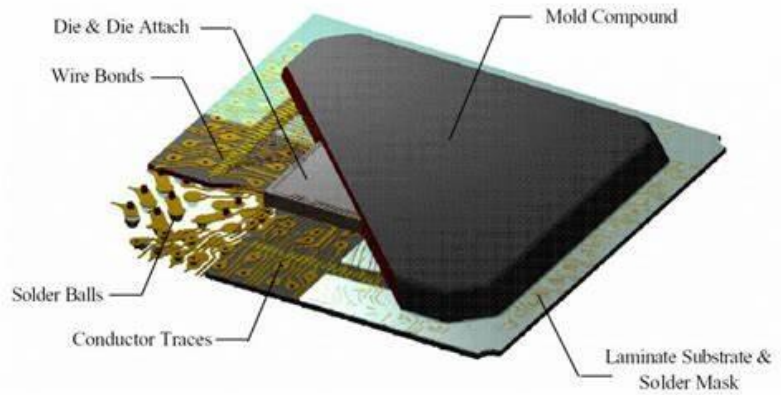
(0.1- 1) mm x (0.1-1) mm?

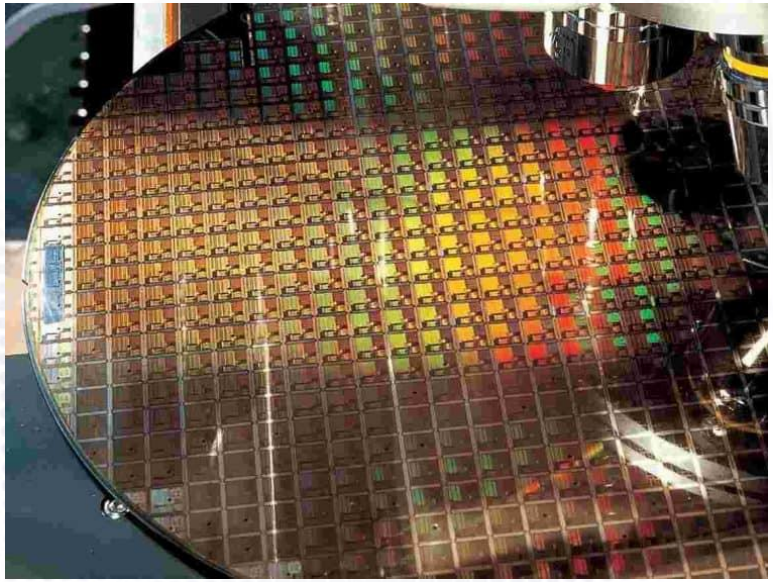
55um x 55um

Readout challenging for pixel TPC

- What we may look for….







High density PCB process
Precision: 100 um
Pads: 10 mm

Chip packaging process
Precision: 1-10 um
Pixels/Pads: 0.1-1 mm

IC process
Precision: 0.1 um
Pixels: ~10 um

Readout challenging for pixel TPC

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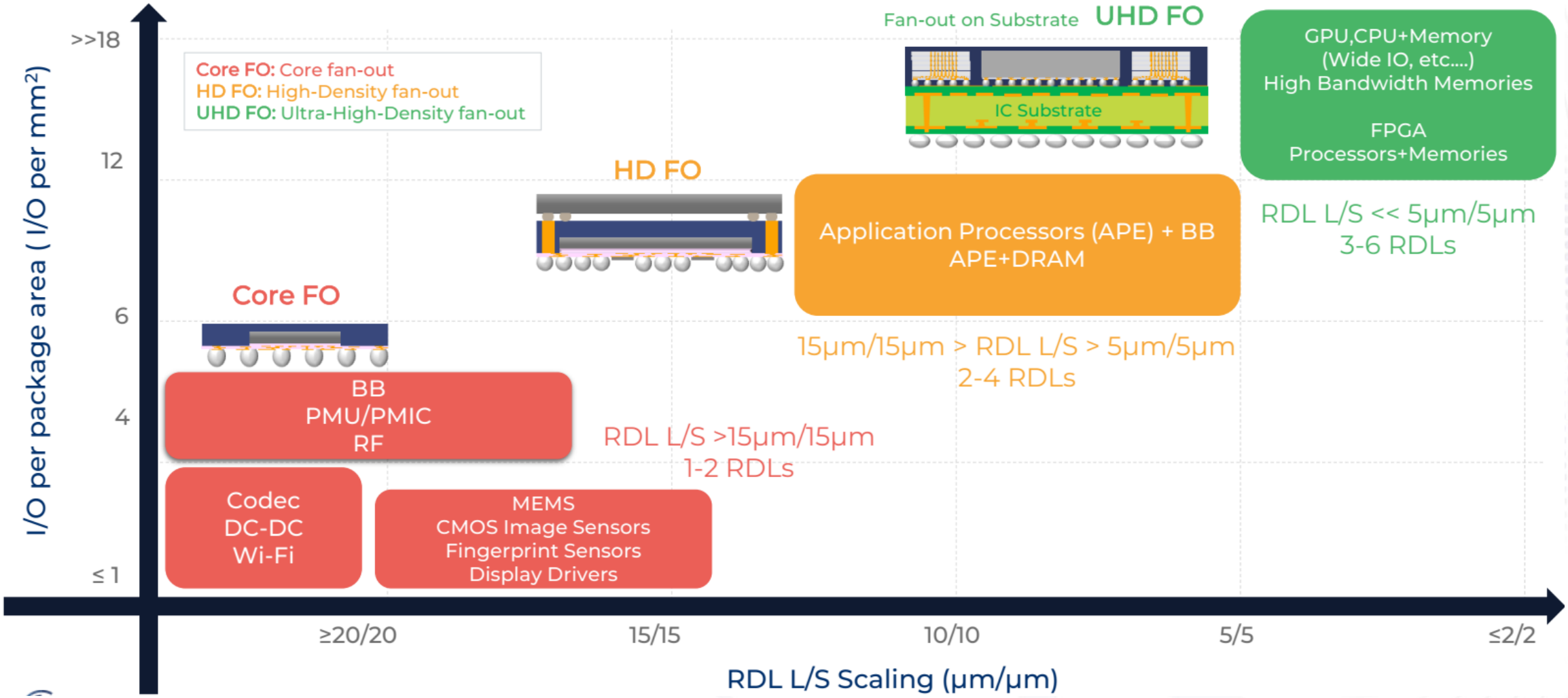
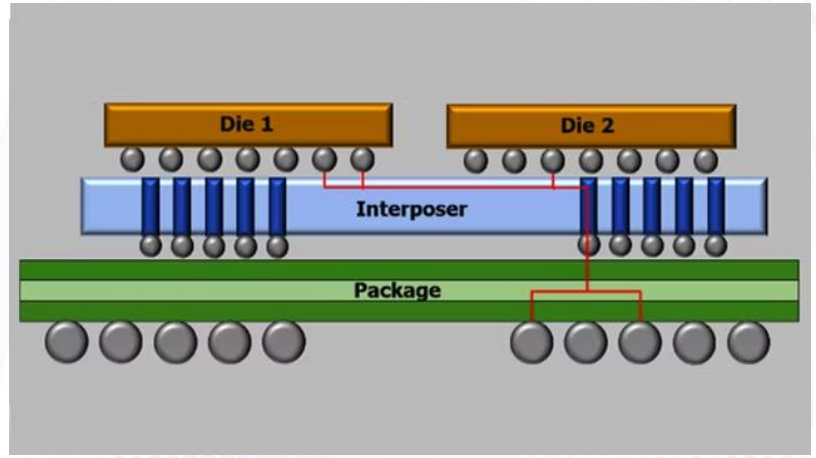
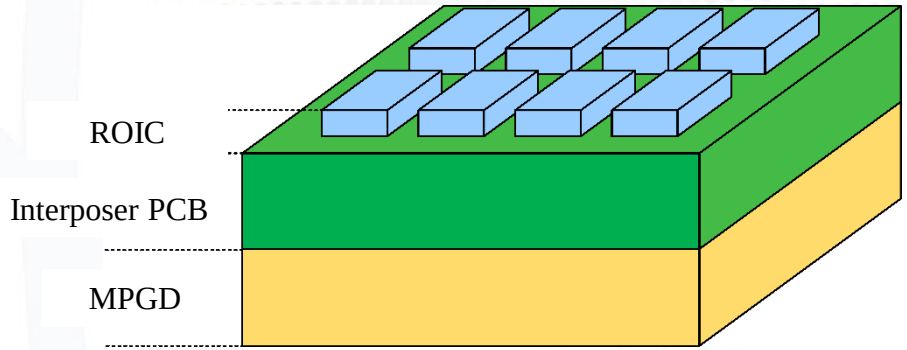
➢ Advanced chip packaging technologies



Interposer based pixel TPC

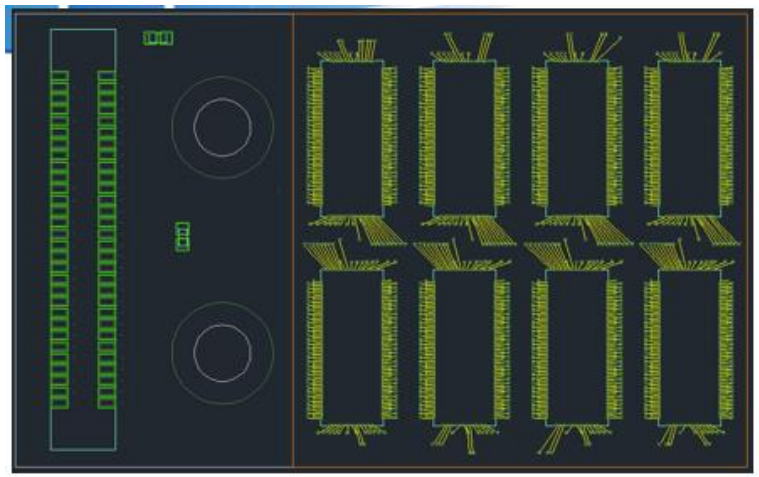
- Pixel readout electronics
  - Multi-ROIC chips + Interposer PCB as RDL
  - High metal coverage
  - Four-side buttable
- Low-power energy/time measurement ASIC：TEPIX
  - Low noise: ~100 e noise
  - 5 ns drift time resolution
  - Low power: 100 mW/cm2 (250uW/ch)



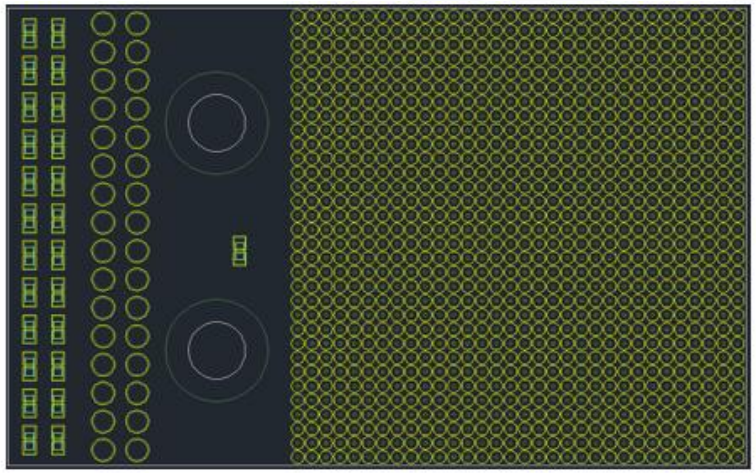


Interposer based pixel TPC

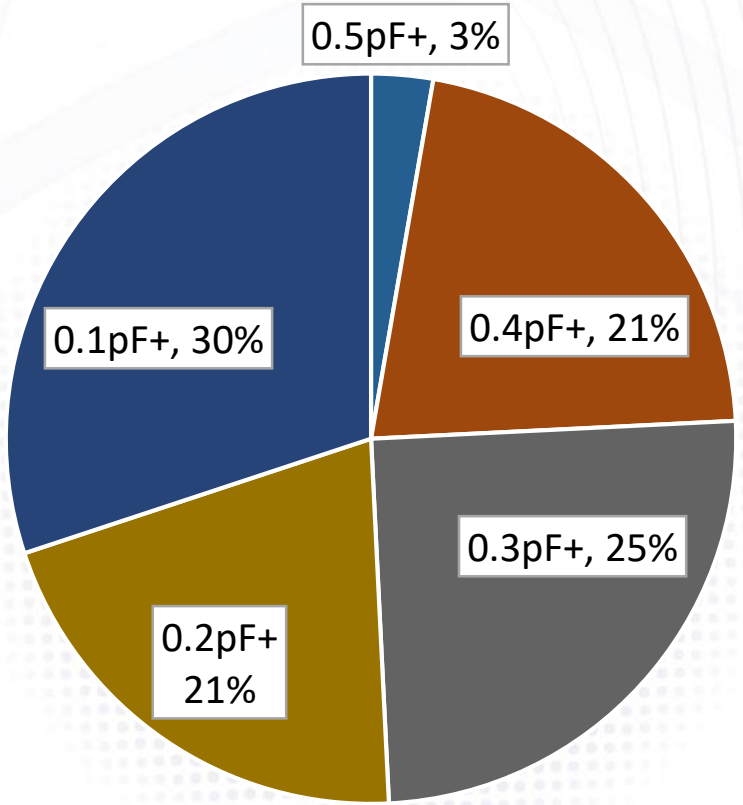
- Interposer design
  - 8 TEPIX chips in the same RDL module
  - L/S: 15 um/15 um, hole size: 50 um， 8 layers
  - Parasitic capacitance optimized



8 TEPIX chips

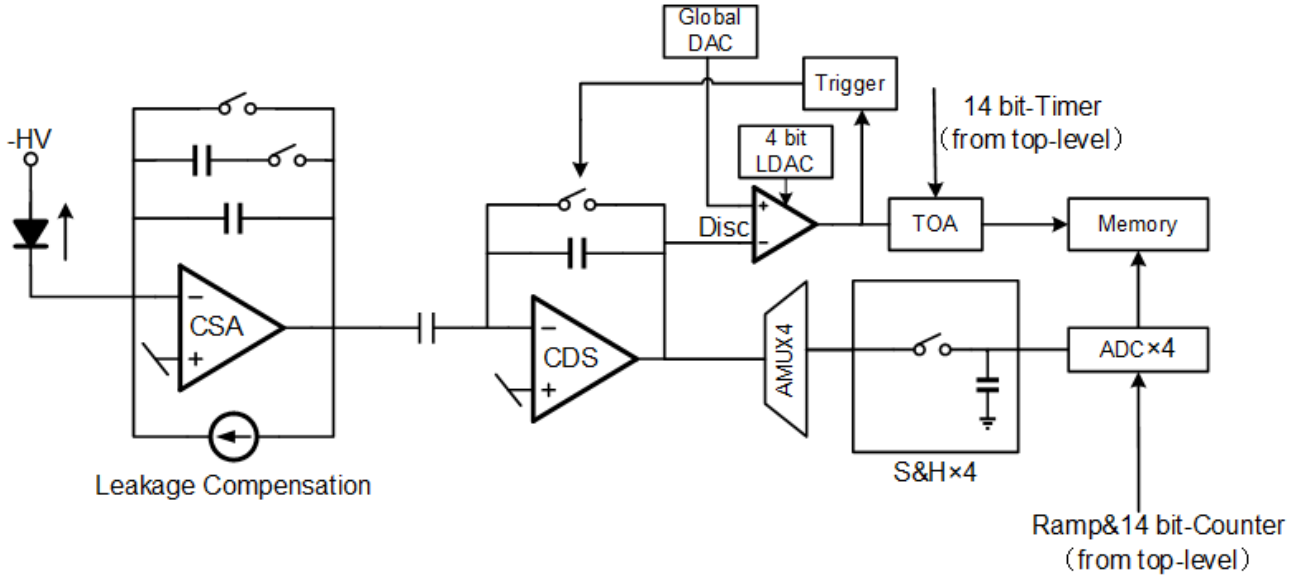


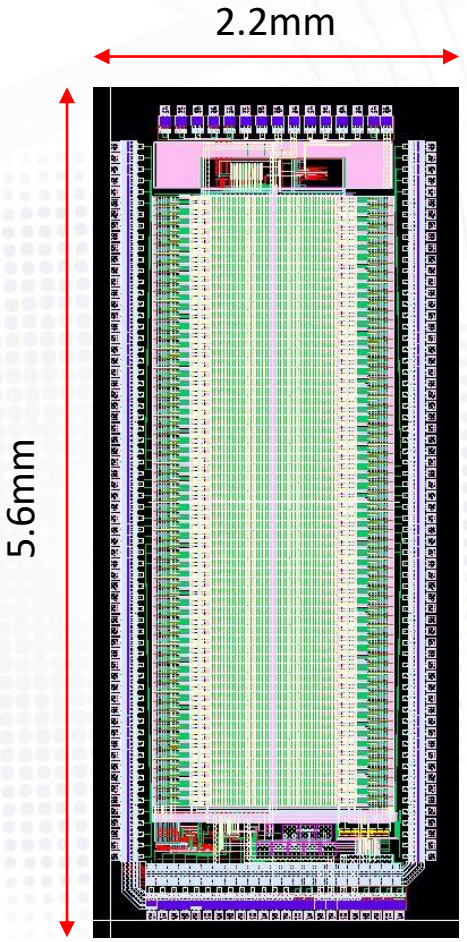
0.5mm x 0.5mm pixels



Readout ASIC: TEPIX

- Block diagram
  - Charge Sensitive Preamplifier(CSA)
  - CDS amplifier provides additional gain and noise shaping
  - Wilkinson type ADC each pixel
  - Timing discriminator with Time of Arrival information

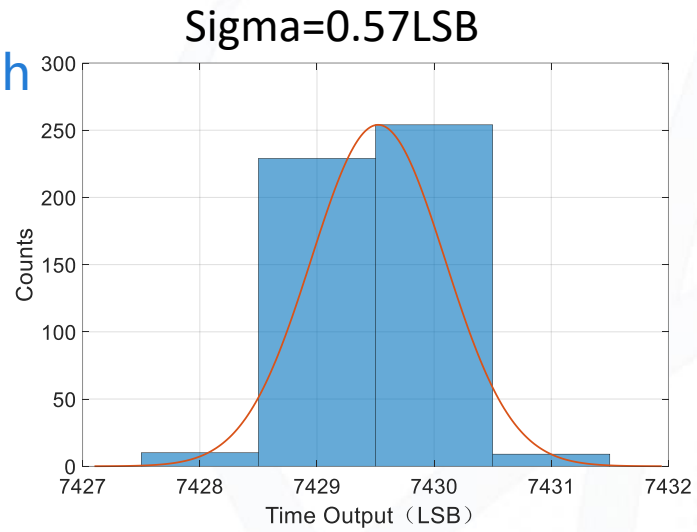


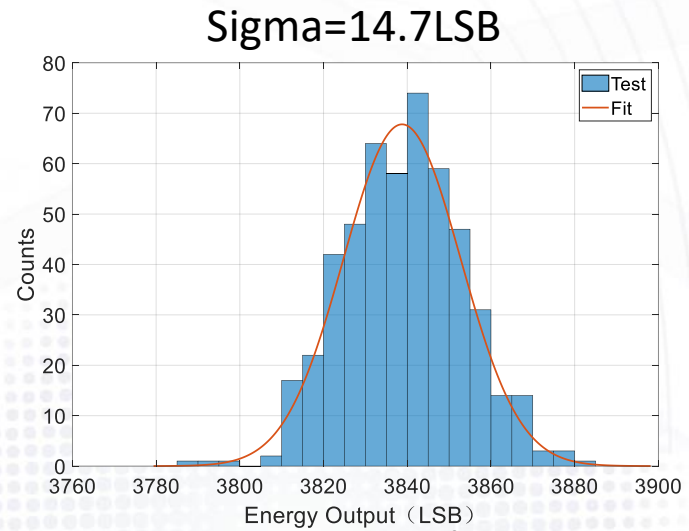


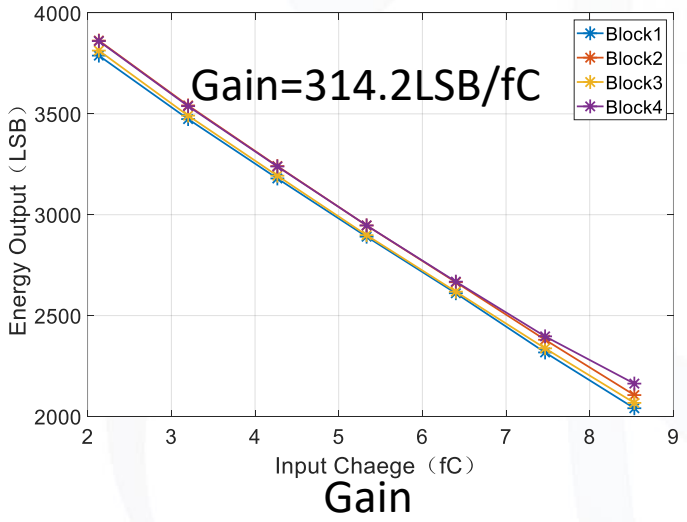
Readout ASIC: TEPIX

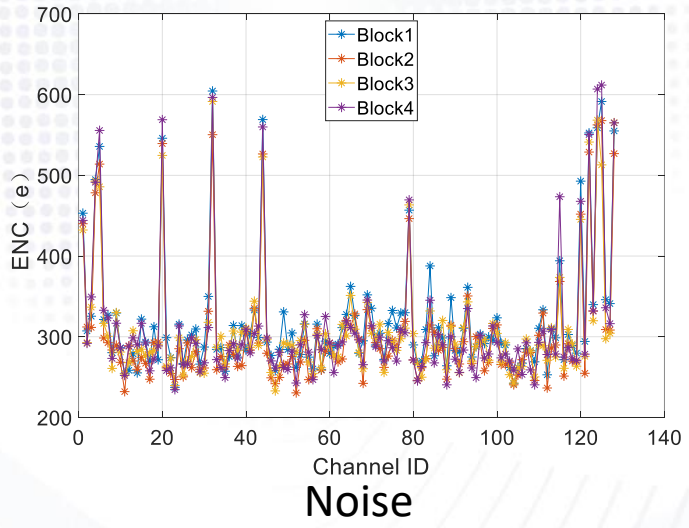
- Test results
  - Power Consumption ~ 0.5mW/ch
  - Timing ~ <1LSB(10ns)
  - Noise ~ 300e

Parameter	Spec
Number of channels	128
Power Consumption	Analog<30mW
	Digital<30mW
ENC	~300 e(high gain)
Dynamic Range	25fC(high gain)
	150fC(low gain)
INL	<1%
Time Resolution	<10ns



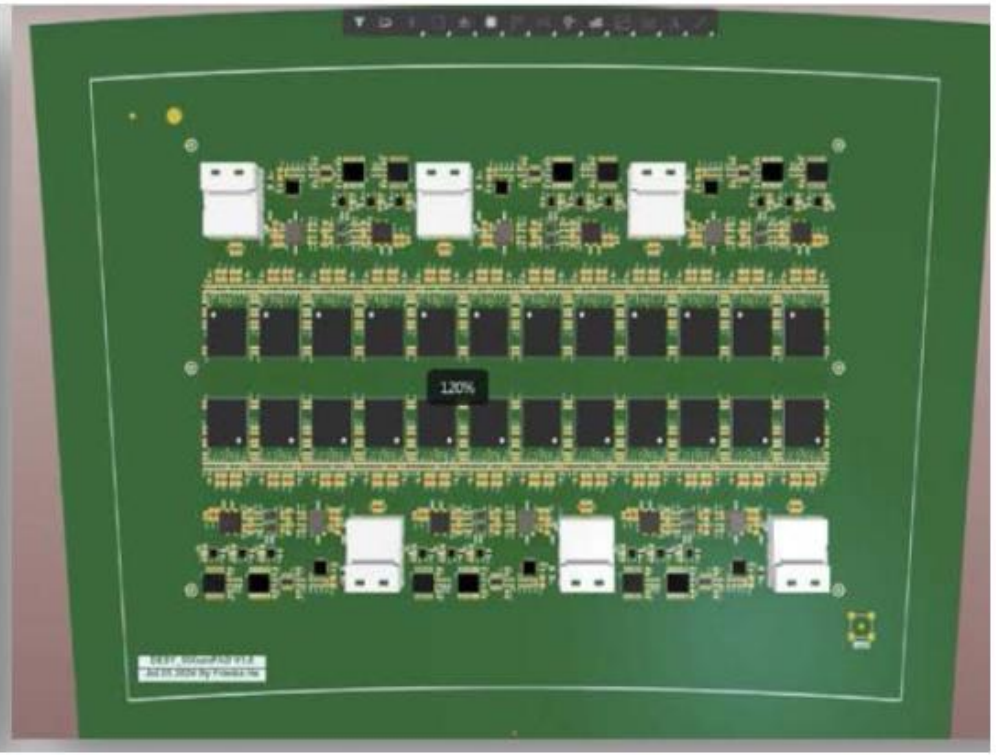






Prototype for beam test

- Pixel size: 0.5mm x 0.5 mm pixel
- Pixel number: 5 mm x 150 mm → 10 x 300 channels

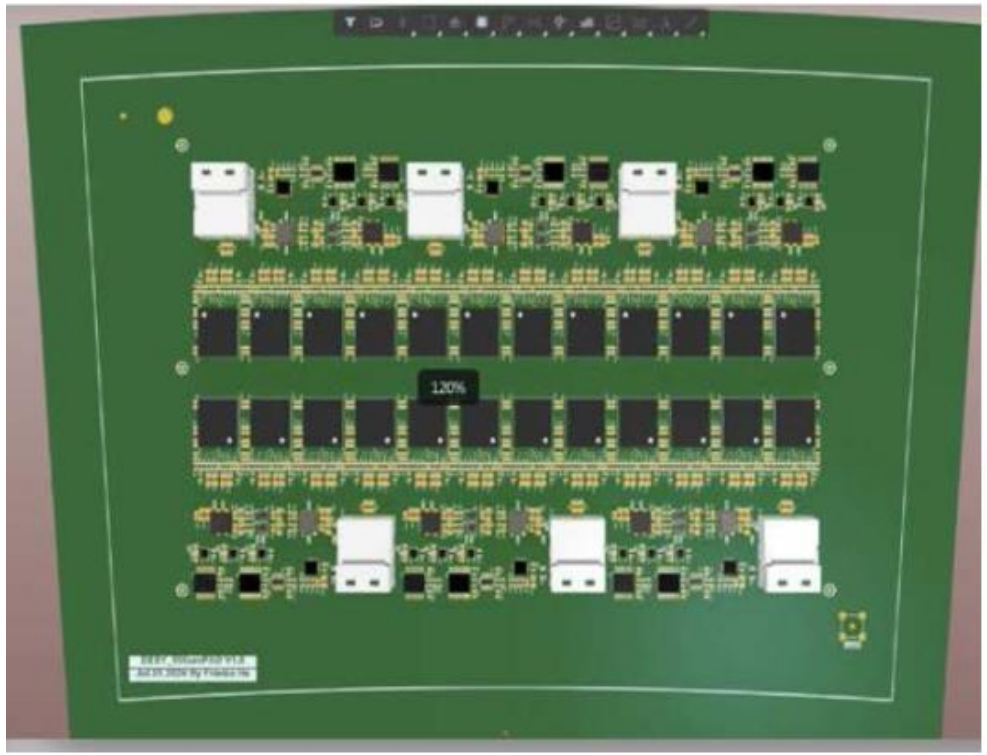


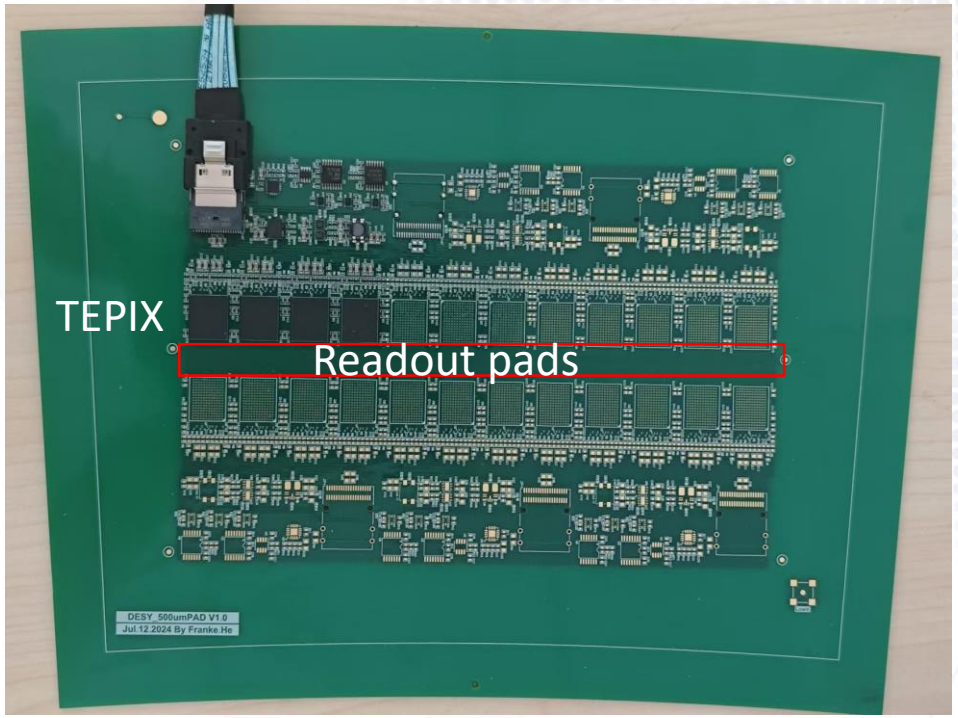
Prototype for beam test

清華大學工程物理系
Department of Engineering Physics, Tsinghua University

- Test board and setup

FE-link





Prototype for beam test

清華大學工程物理系
Department of Engineering Physics, Tsinghua University

Preliminary test results with calibration signal:

- Charge injected ~6fC;
- 4 triggers, gap between each trigger 40us

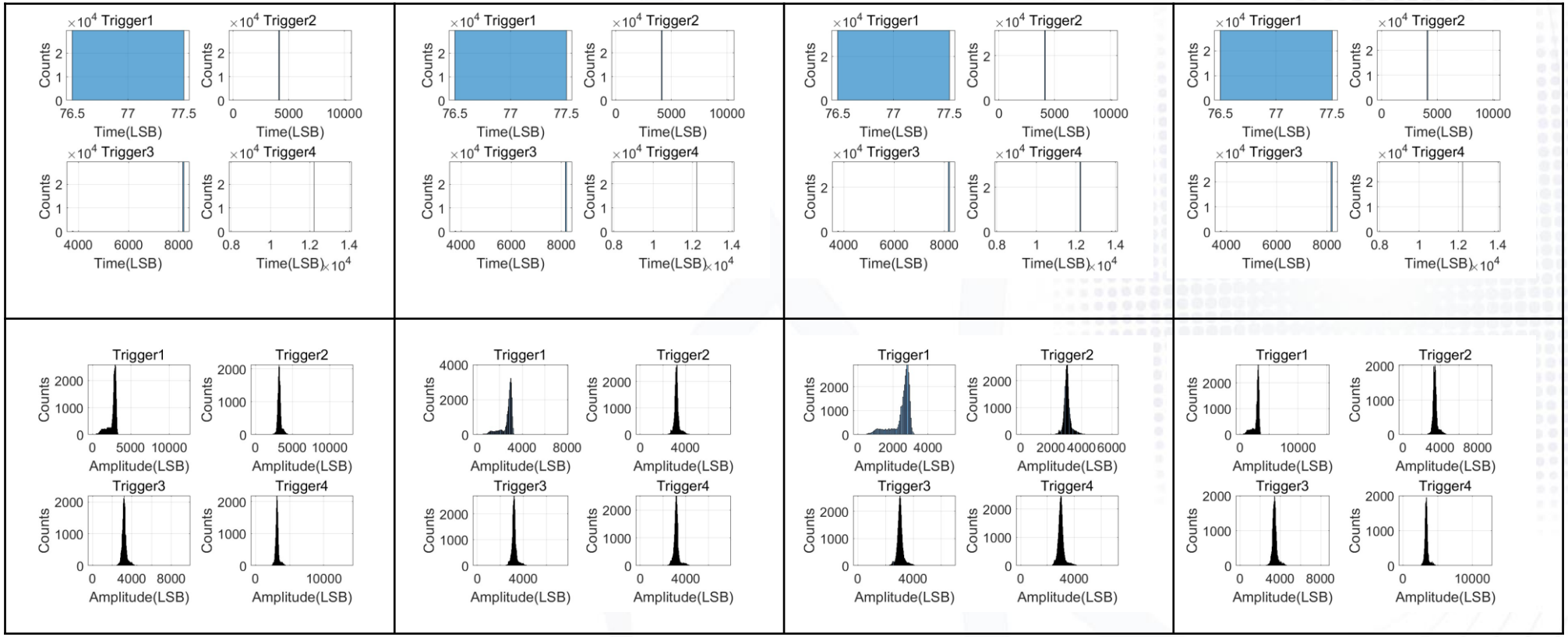
Results:

- got expected trigger time.
- got expected energy value according to the charge injected.
- some channels has lower energy of 1st trigger, need further investigation.

Trigger time and energy histogram:

Time:

Energy:



TEPIX1 TEPIX2 TEPIX3 TEPIX4

04 | Summary

Summary

- TPC can realize large-volume, 4π solid angle coverage of three-dimensional particle track detection, and has a wide range of application prospects in basic physics experiments, astronomical observations, and nuclear energy development

- In the past ten years, we have developed a variety of waveform sampling front-end chips for pad-type TPC readout, and the latest WASA chip integrates analog front-end, ADC waveform sampling, digital filter, trigger logic and other circuit functions, and based on this chip, we have developed a scalable TPC readout electronics system

- Pixel readout is also one of the current development trends of TPC detector technology, and we have developed a low-power energy and time measurement readout chip TEPIX for pixel TPC readout, which realizes sub-millimeter pixel readout through a high-density interposer substrate

Acknowledgements

- We would like to thank Li Yulan and Feng Hua of Tsinghua University, Li Jin and Qi Huirong of the Institute of High Energy Research, and Zhu Chengguang of Shandong University for their technical exchanges and support in TPC detectors

- Special thanks to the graduate students who completed the chip development and test: Liu Wei, Dong Jianmeng, Liu Canwen (currently studying), Wei Tong (currently studying), Yang Yanxiao (currently studying)

THANKS