# Design and optimisation challenges while codesigning a new front-end ASIC together with a resistive Micromegas detector for AMBER experiment

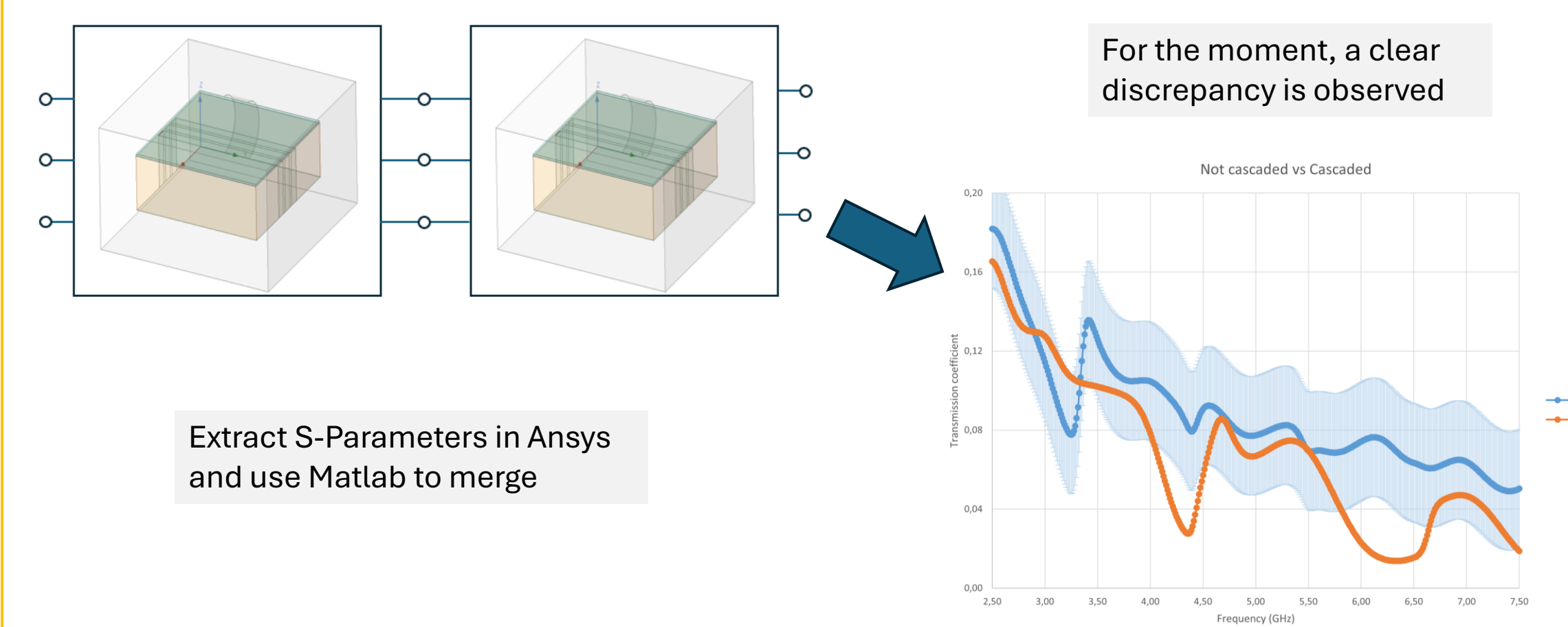Maxim Alexeev & Chiara Alice on behalf of ASIC & MM design teams

We are looking on the signal path from the generation to the FE ASIC

We consider the Gas amplification and current induction mechanisms well described

Gas mixture: Ar-CO$_2$ 93/7
Amplification gap: 120 μm
Conversion gap: 5mm

We have a priori knowledge of the detector structure, but how to implement it into the signal propagation simulation?

X shielding and connector layer : 35um copper
-3.2mm Glass epoxy
X strip layer : 35um Copper
-50um Prepreg
-50um Kapton
X DLC layer
-pillars 150um
X mesh: 45/18

Drift gap : 5mm
Drift mesh :45/18
Drift gap: 5mm

U.V mesh: 45/18
-pillars 150um
U.V DLC layer
-50um Kapton
-50um Prepreg
U Layer: 35um Copper
-28um Prepreg
V Layer: 17um copper
-3.2mm glass epoxy
U.V bottom shielding and connector layer: 35um copper

Single channel response simulation with 25ns and 250ns peaking times

To properly design the readout ASIC a description of the path and effective signal deteriorations look useful

Finite elements?

In software like Ansys HFSS A full model of the path could be created but it is very computation expensive, and licence bonded
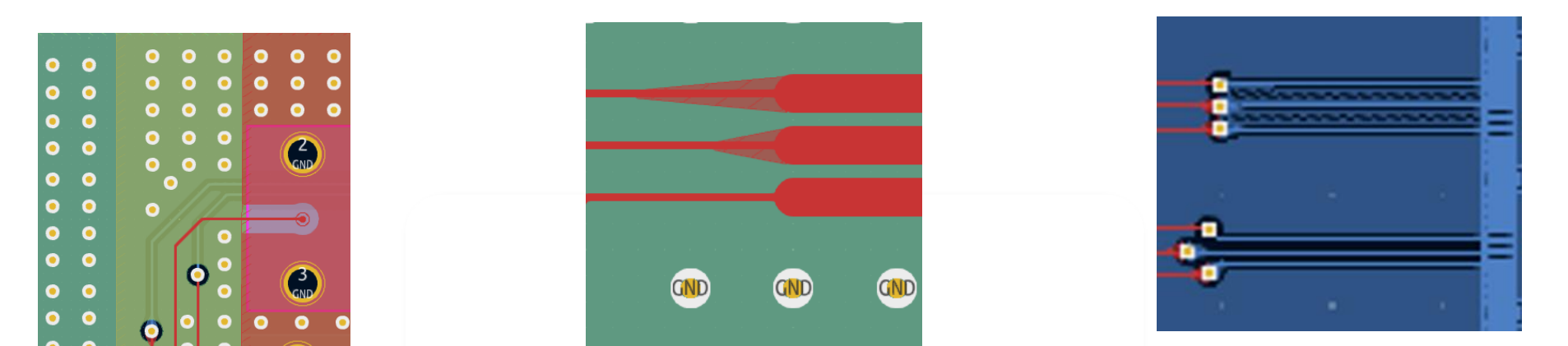
500 mm
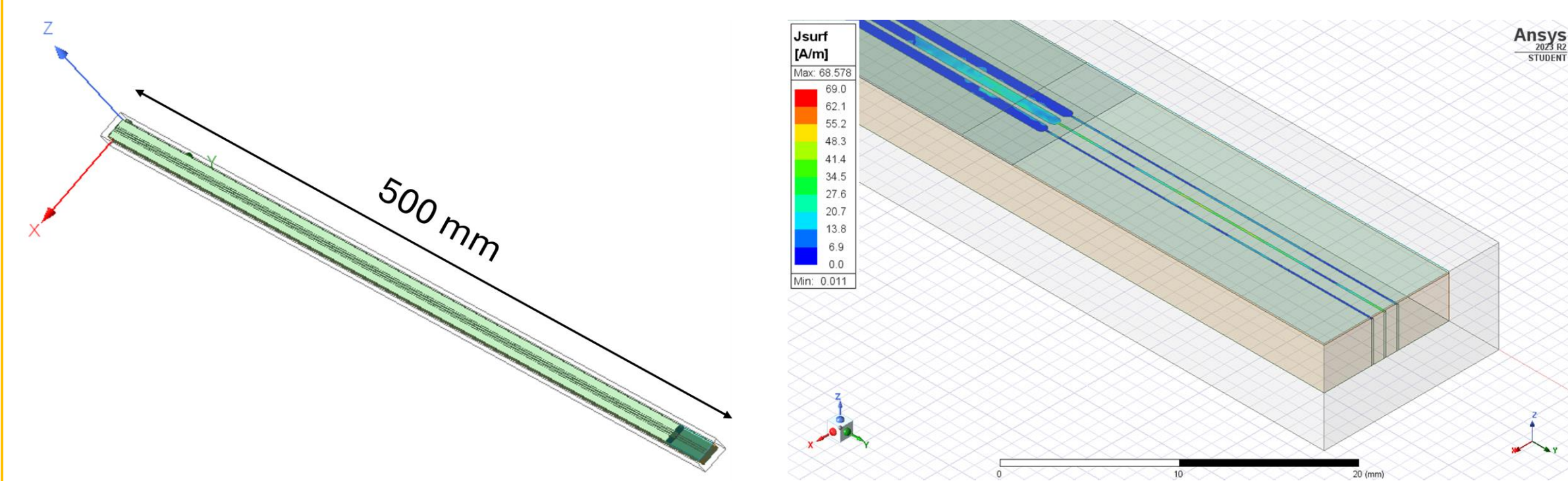
We could simulate small elements of the path and try to merge the results into a simulation model (Cascade models)?
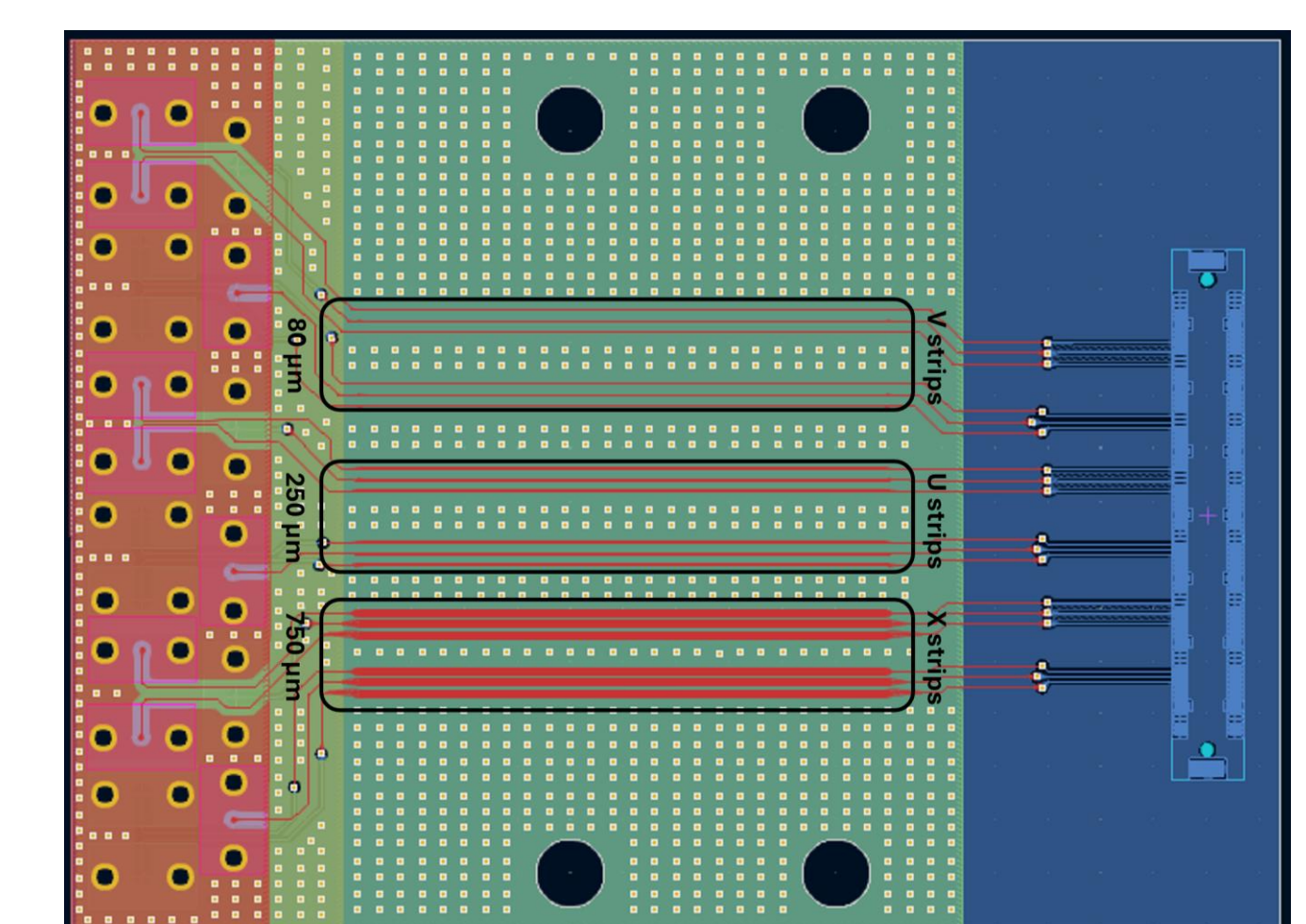
Extract S-Parameters in Ansys and use Matlab to merge

For the moment, a clear discrepancy is observed

Not cascaded vs Cascaded

To check if we understand the results we could go for a simplified test?

Can we extract it from a real detector?

The FE board should be taken into account
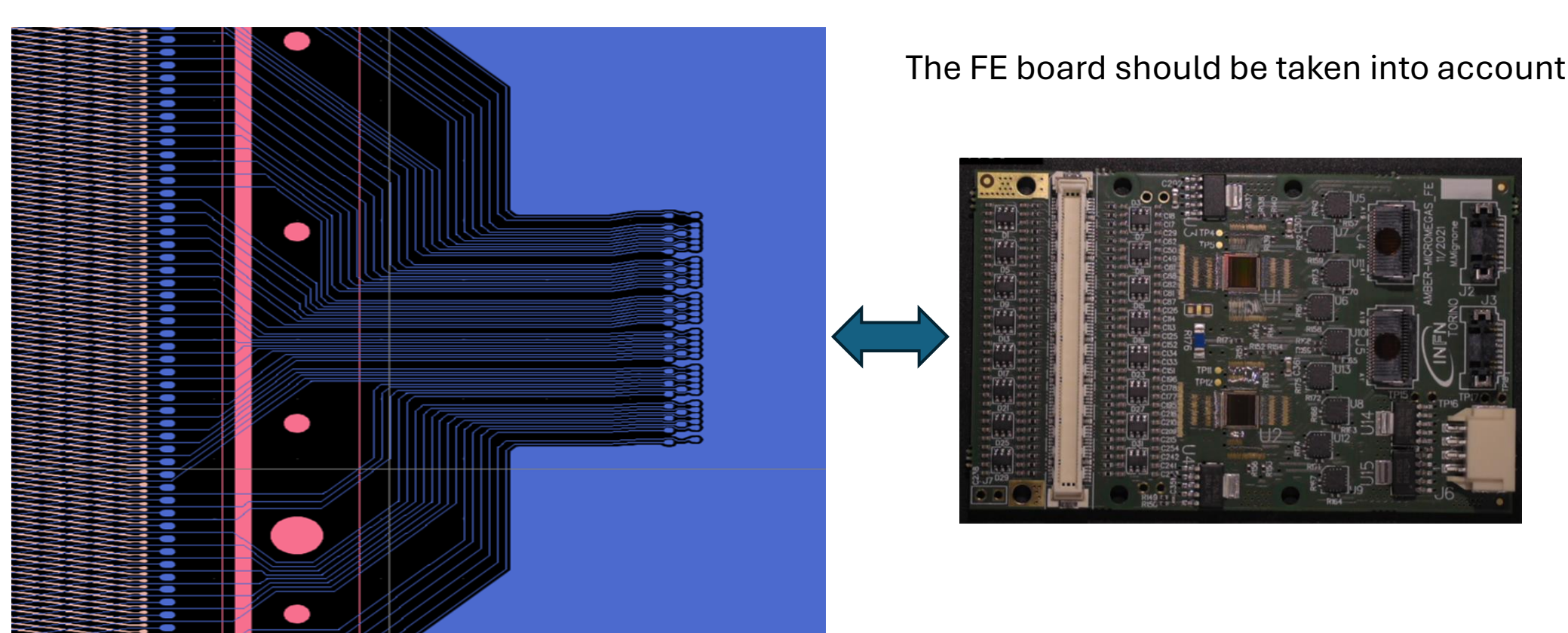
Signal path description in terms of S-parameters needs to take into account all possible discontinuities such as vias or connectors. We can use TDR instruments to extract the real response

For higher frequencies a SPICE model should include a S-parameters parametrization

Vector Network Analyzer (VNA) + Time Domain Reflectometer (TDR) Capabilities

Port 1   Port 2
a_1 b_2
S_{11} S_{22}
S_{12}
b_1 a_2
Z_0 Z_0

Detector in the simulation
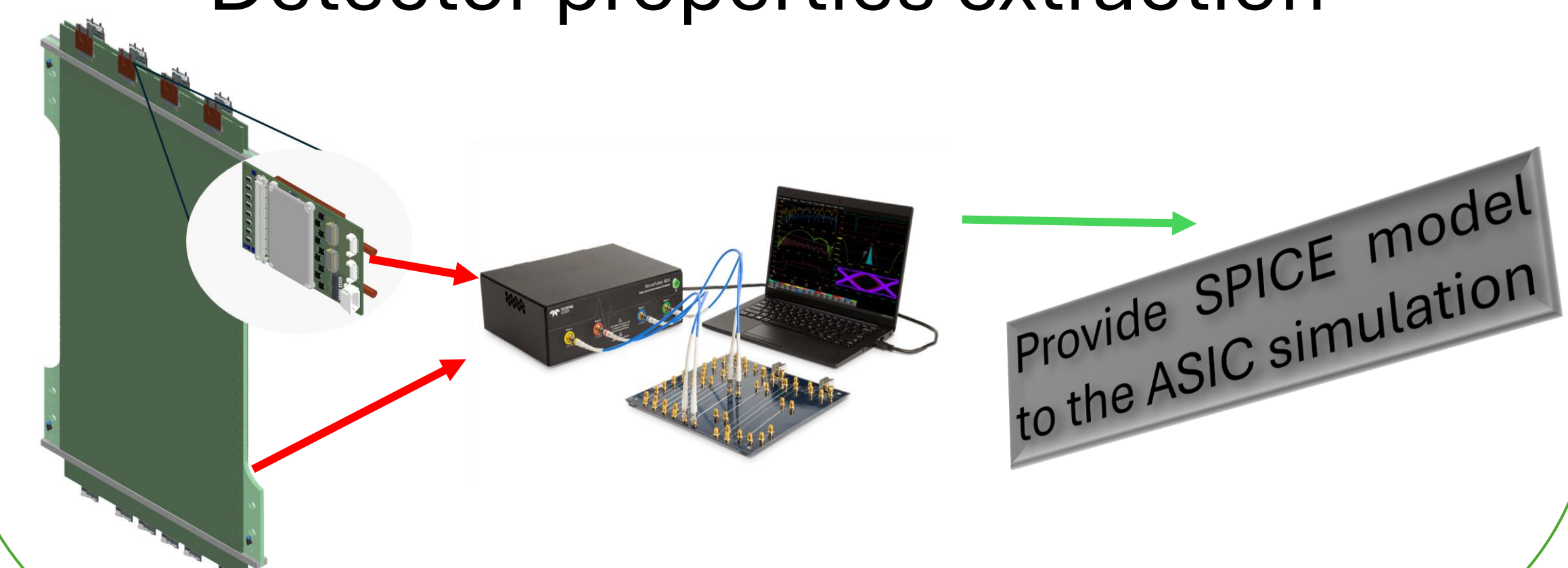
We would like to add details here

ASIC simulation

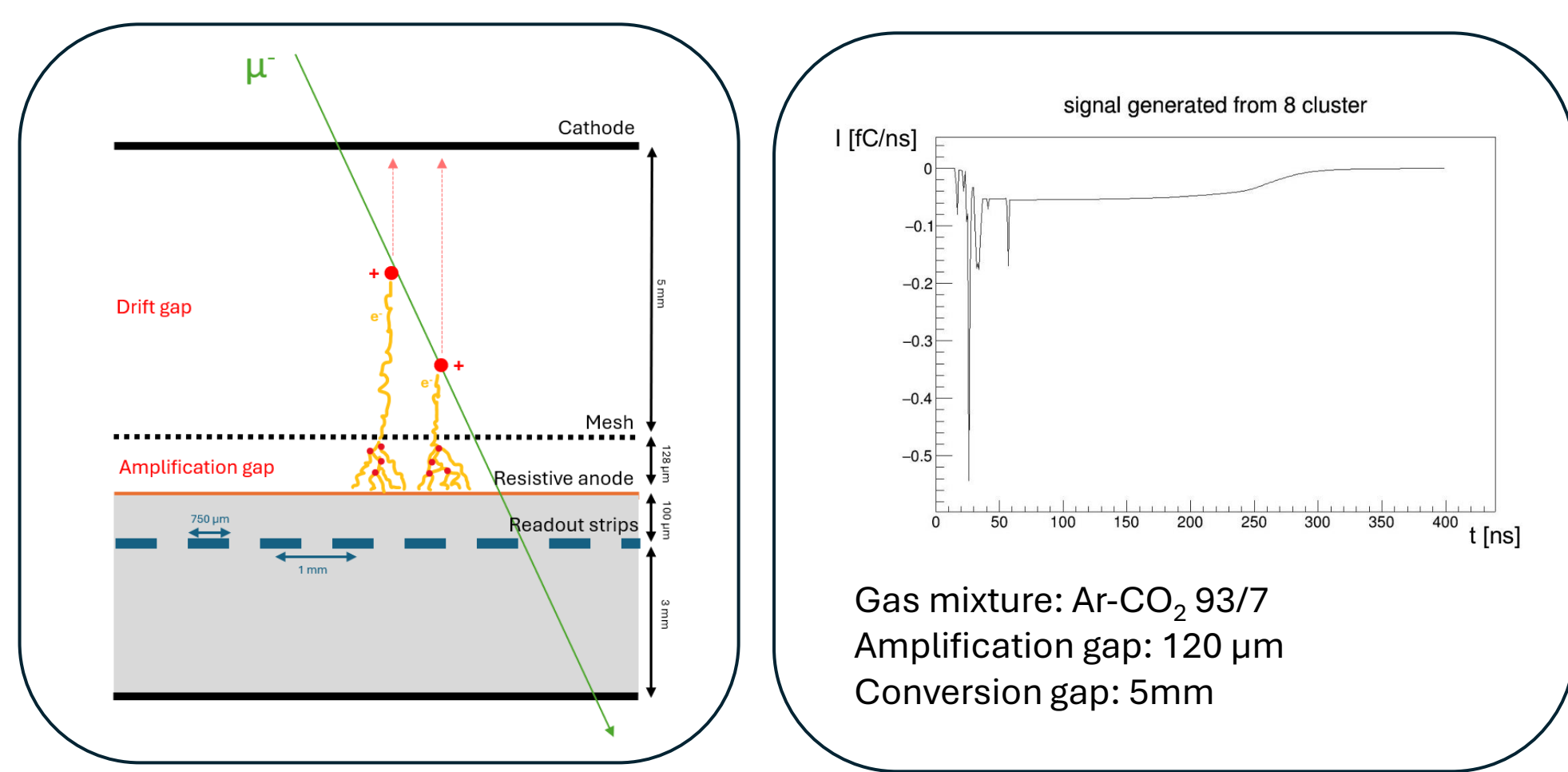## Our way

Element PCBs sim VS reality

Segment PCBs sim VS reality

Detector properties extraction

Provide SPICE model to the ASIC simulation