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3. Design and optimisation challenges while codesigning a new front-end ASIC together with a resistive Micromegas detector for AMBER experiment

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The Apparatus for Mesons and Baryon Experimental Research (AMBER, NA66) is a high-energy physics experiment at CERN's M2 beam line at the Super Proton Synchrotron (SPS). Its broad physics program extends beyond 2029. Measurements of the anti-proton production cross-section on He, proton, and Deuterium to support the dark matter searches, the charge-radius of the proton to contribute to the solution of the puzzle in the values and the Kaon and Pion PDFs using Drell-Yan process are already approved for the initial part of the experiment. For this new apparatus we are designing together with the CERN MPT workshop both a resistive MICRO-MEsh GAseous Structure (Micromegas) detector and a new custom 64 channel fully digital front-end ASIC ToRA (Torino Readout for AMBER) for timing and energy measurements. The ASIC is closely tailored to the specifications of the Micromegas but also should be fully suited to equip some of the existing Wire type detectors to make them compatible with the future trigger-less Data Acquisition system (DAQ) of AMBER. This simultaneous design of the ToRA ASIC and of the associated detector aims to achieve a good optimisation of their performance. We must face the challenges coming from the integration with the resistive Micromegas with 1.0-2.5 fC signals at the low end of the charge amplitude spectrum up to 100-150 fC for high signal amplitudes. AMBER Micromegas will have a ˜1.2x0.5 mˆ2 size with ˜1.2 m long strips of up to ˜150 pF capacitance reaching rates of up to 500 kHz/strip. To face these conditions, we need a good control over the system noise and signal integrity performance of the detector itself together with the full signal path to the ASIC to be able to make use of target intrinsic ENC of the ToRA of ˜1000-1500 e- at 150pF. The use of ToRA with Wire detectors adds the requirements of variable gain to cope with charges of up to 1-1.5 pC, a 10-bit ADC resolution and a ˜1ns time resolution. To address the issue of the cooling we expect to reach a <10 mW/ch power consumption. The 65nm design node was chosen for the ToRA ASIC.

We present the models of the detector and signal path elements used in simulation together with simulation results and real measurement of signal integrity on produced test elements. The architecture of the ToRA v1 ASIC will be presented in the contest of this optimisation work with some considerations towards the ToRA v2 review.

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