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Multi-dimensional measurement ASIC for Micro-Pattern Gas Detectors

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Introduction

- The ASIC comprises 1024 row × 1024 column pixel units and a readout control circuit. The readout control circuit groups the pixel array into sets of 4 columns and achieves lossless readout at a frequency of 200 MHz. It includes an address module, a signal judgment module, two levels of FIFO, a first-level continuous arbitration circuit, a four-level cyclic arbitration circuit, and a Token Ring control circuit.
- The chip outputs the address of the hit pixel, the corresponding energy information and the arrival time using an event-driven method. The measurement accuracy is 5 ns, the spatial resolution is 15 μm, the dead time is 60 ns, and the readout efficiency is higher than 99%.

Overall architecture

The chip employs an event-driven approach to output the address of the hit pixel, along with the corresponding energy information and arrival time. The size of the chip pixel array is 1024 by 1024. The peripheral modules of the chip include a Time-to-Digital Converter (TDC), Signal Discrimination Unit (SDU), Address Coding Unit (ACU), Token Ring Control Unit (TRCU), Super Column Control Module (SCC), Column Block Control Module (CBC), as well as cyclic arbitration circuit and continuous arbitration circuit,as shown in Figure 1.

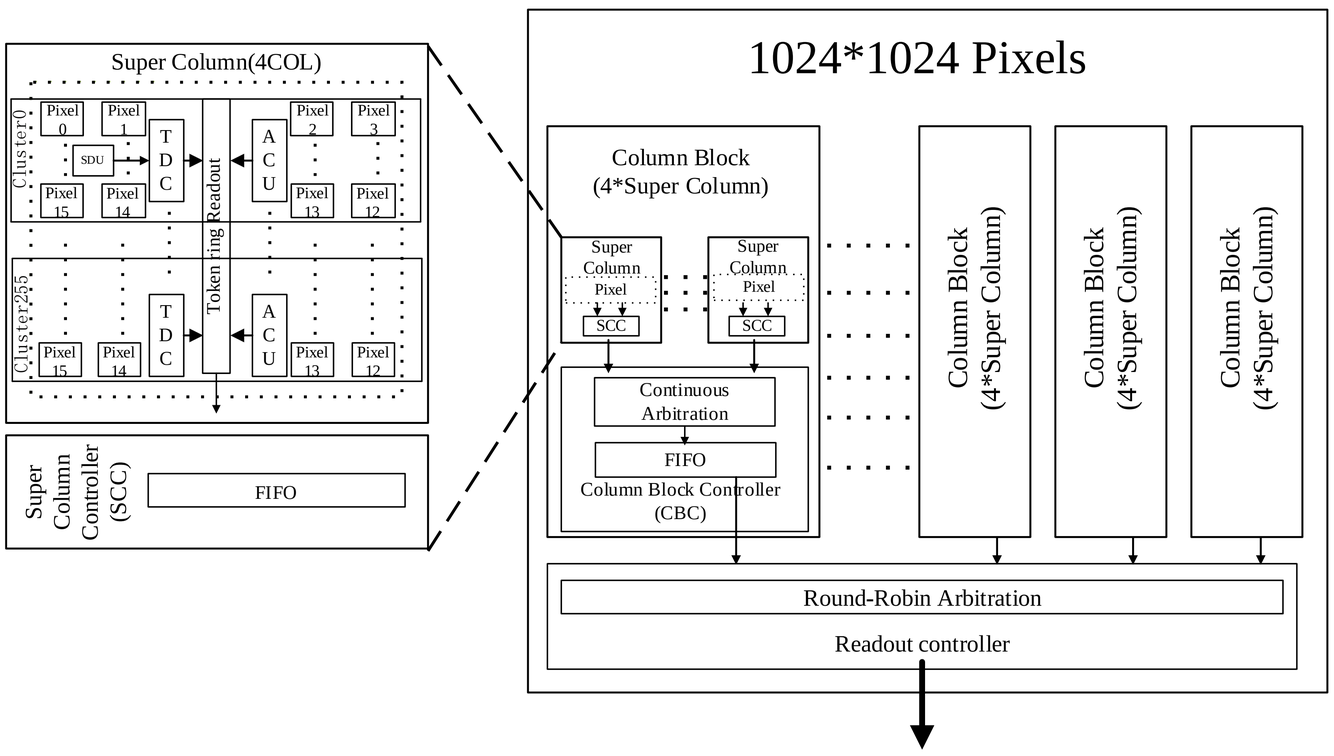

Figure 1 Structure of the pixel readout chip

Arbitration Circuit

- Continuous Arbitration Circuit:When four channels need to transmit data, the continuous arbitration circuit transmits data based on the status of the channels. If all channels have non-empty states, data transmission begins in the order of channels 0, 1, 2, and 3. If a channel is non-empty, data is transmitted; if it is empty, the circuit skips to the next channel and evaluates its signal. If all channels are empty, the module enters an idle state and stops searching. The module will continuously read data from a specific channel until its FIFO memory is empty. This means data transmission will continue if the current channel remains non-empty. The state diagram of continuous arbitration circuit are shown in Figure 3.
- Cyclic Arbitration Circuit:When four channels need to transmit data, the cyclic arbitration circuit transmits data based on the status of the channels. If all channels are in a non-empty state, data transmission begins in the order of channels 0, 1, 2, and 3. If a channel is non-empty, data is transmitted; if it is empty, the circuit skips that channel and checks the next channel's empty signal. If all channels are empty, the circuit enters an idle state and stops searching.When reading data from a specific channel, the circuit reads only one data cycle, which reads one data set before moving on to the next non-empty channel. It continues this process of reading one set of data from each non-empty channel in a cyclic manner until all channels are empty. The state diagram of cyclic arbitration circuit are shown in Figure 3.

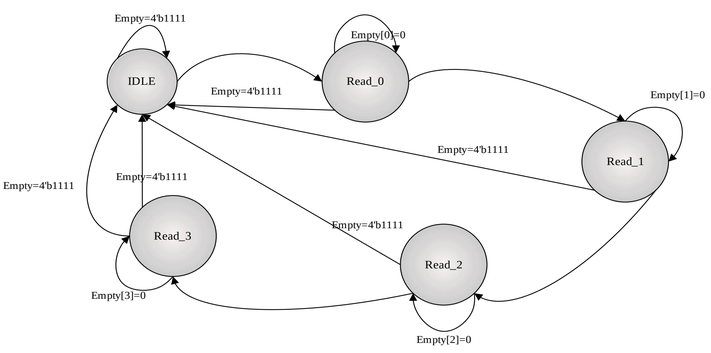

Figure 3 State Diagram of Continuous Arbitration Circuit

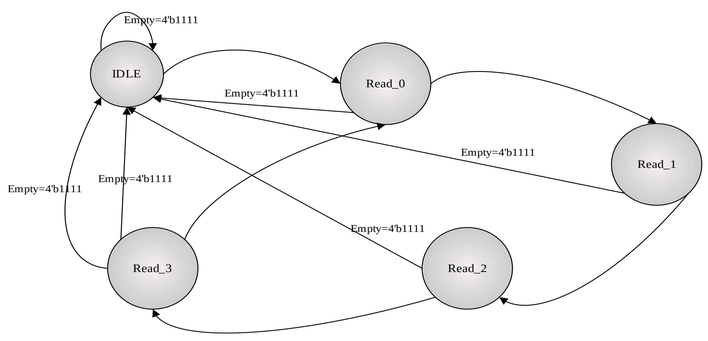

Figure 4 State Diagram of Cyclic Arbitration Circuit

Column Readout Circuit

In the column structure, the signal readout process is described as follows:

- In SCC, 16*16 pixels are called a cluster and share a TDC. There are 256 clusters in SCC. When a pixel in the cluster is hit, the Hit signal is judged by the SDU unit. Only the rising edge of the first Hit signal is output, and the falling edge is sent to the TDC unit to measure the energy information and arrival information; at the same time, ACU will also detect the rising edge of the first Hit signal, and determine its position in the cluster, and then output 4-bit address information.
- The Token Ring method facilitates the readout of necessary information among the 256 clusters within the SCC. If a cluster requires data output and possesses a valid token, it can transmit its information to the data bus. Concurrently, the token is updated and transferred to the next pixel unit in line. The newly issued token prevents other units from transmitting data until the current cluster has finished. Once the data output for a cluster is completed, the token is then synchronized and passed on to the next cluster that is queued to output its data.
- Data that has been transmitted is held in temporary storage within the bottom FIFO unit, pending its retrieval by the continuous arbitration circuit for subsequent readout. This process ensures an orderly and efficient management of data flow within the system.

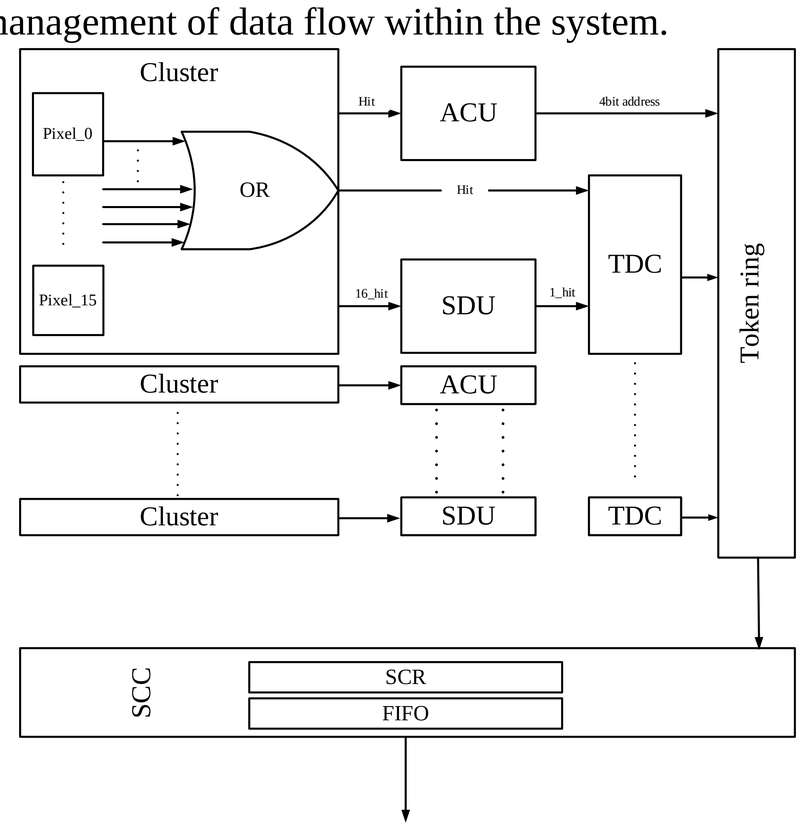

Figure 2 Architecture of Column Readout

Summarized and prospected

The chip design work as follows. Currently, the Verilog code for the readout chip has been completed and successfully verified through simulation using Synopsys VCS, achieving the intended functionality and specifications of the design. Next, we will conduct prototype verification on a Xilinx 7 Series FPGA to evaluate the readout chip's readout rate, dead time, and readout efficiency under simulated random particle hit conditions.

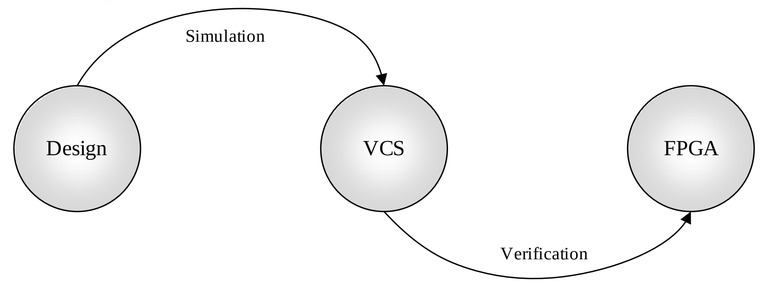

Figure 5 Flow Diagram of chip design

References

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[2] X. Wie, High data-rate readout logic design of a 512 × 1024 pixel array dedicated for CEPC vertex detector[J]. 2019 JINST 14 C12012