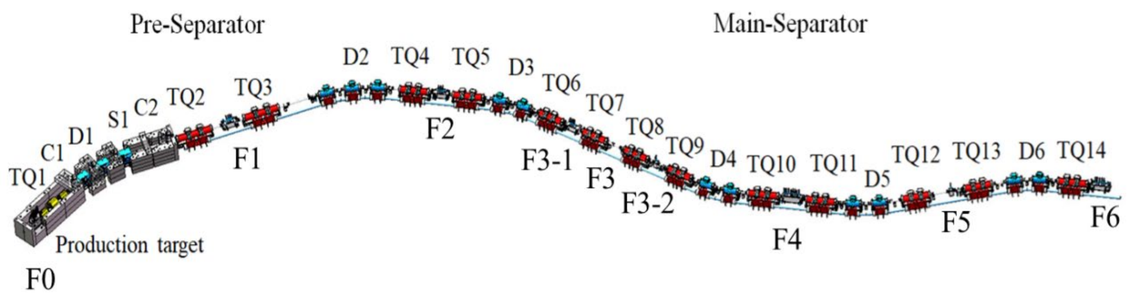
Prototype design of the high-precision clock generation and distribution for multiple detectors cooperative work at HIAF-HFRS

Jieyu Zhu[1,2], Haibo Yang[1,2,*], Yangzhou Su[1,2], Chengxin Zhao[1,2]
([1]Institute of Modern Physics, Chinese Academy of Sciences, China)
([2]School of Nuclear Science and Technology, University of Chinese Academy of Sciences, China)
yanghaibo@impcas.ac.cn

Abstract—This paper describes the prototype design of high-precision clock generation and distribution for multiple detectors in HFRS at HIAF. The system is based on a master-slave architecture design. The test results indicate that the period jitter is better than 4.47ps, the time interval error (TIE) jitter is better than 2.16 ps, and the cycle-to-cycle period (C-C period) jitter is better than 7.78 ps after transmission over 200 m optical fiber. The system can provide a stable and accurate 40 MHz synchronous clock to meet the design requirements.

HIAF and HFRS

A High Intensity Heavy-Ion Accelerator Facility (HIAF) is currently under construction, and a cutting-edge High Energy Fragment Separator (HFRS) with high energy and intensity capabilities is being installed. HFRS is an important facility in the HIAF, located between BRing and SRing, with a total length of 180 m. It is designed to study the properties of rare isotopes and their nuclear reactions relevant to astrophysics. HFRS is characterized by high magnetic rigidity, large optical acceptance of ions, and accurate particle identification.

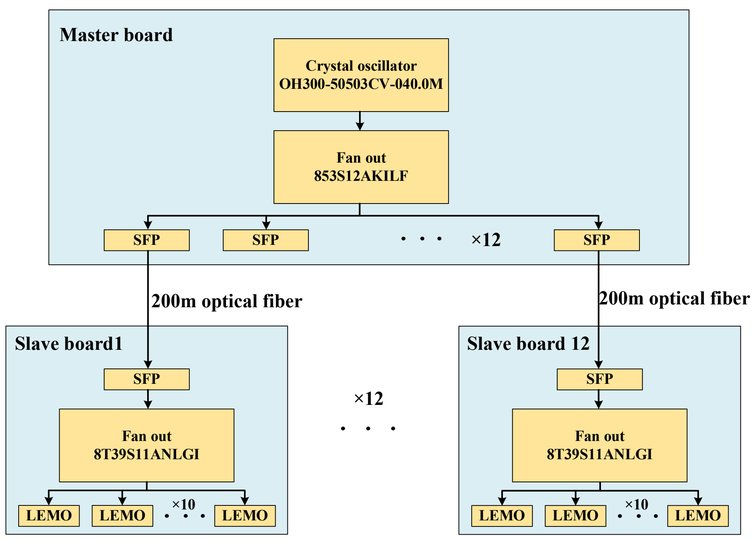


The diagram of HFRS

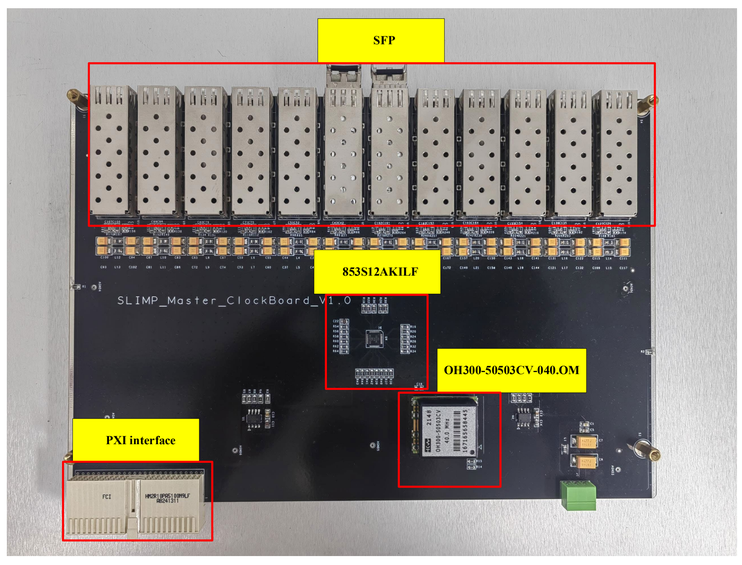
HFRS identifies particles using time-of-flight measurements, position measurements, and energy loss measurements from multi-detector cooperation can identify isotopes with mass numbers up to 200. HFRS provides accurate energy loss measurement with multiple sampling ionization chambers, time measurement with diamond detectors and position resolution with GEM-TPC detectors.

The design of the clock board

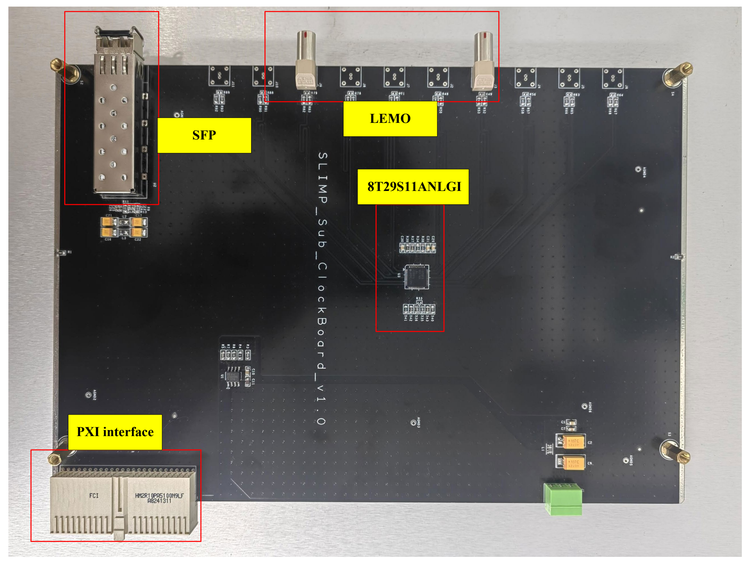
The master board generates a high-precision 40 MHz clock through a high-quality crystal oscillator. Then, it feeds it to the input of a low-jitter clock fan-out chip, which can distribute the 12 LVPECL level signal outputs to the optical transceivers and then transmit to the slave boards via optical links. The slave board receives the clock signals from the master board, then fans out 10 LVDS differential clock signals through a low jitter clock chip, and provides synchronized clock signals to the front-end electronics or DAQ system through the differential LEMO connectors. The slave boards and master boards are connected by 200 meters of optical fibers.



The diagram of clock board



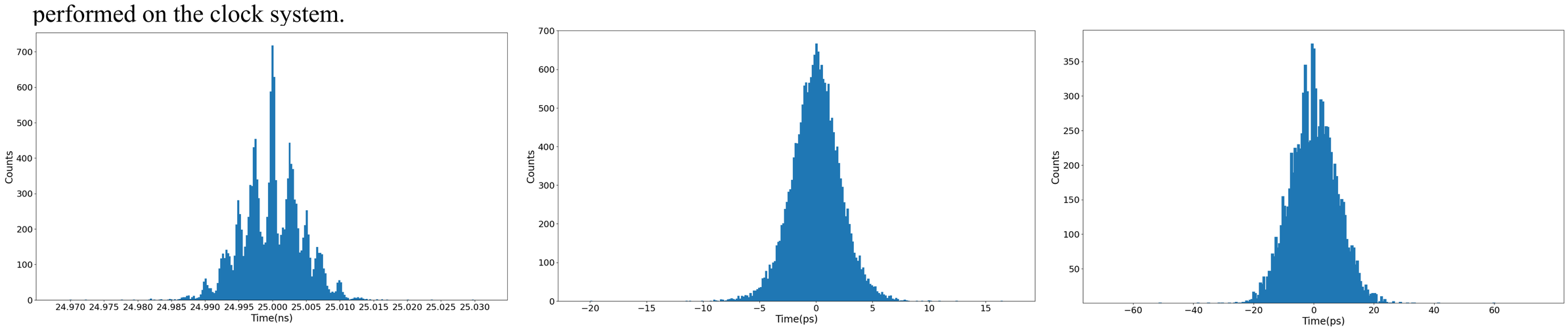
The image of master board



The image of slave board

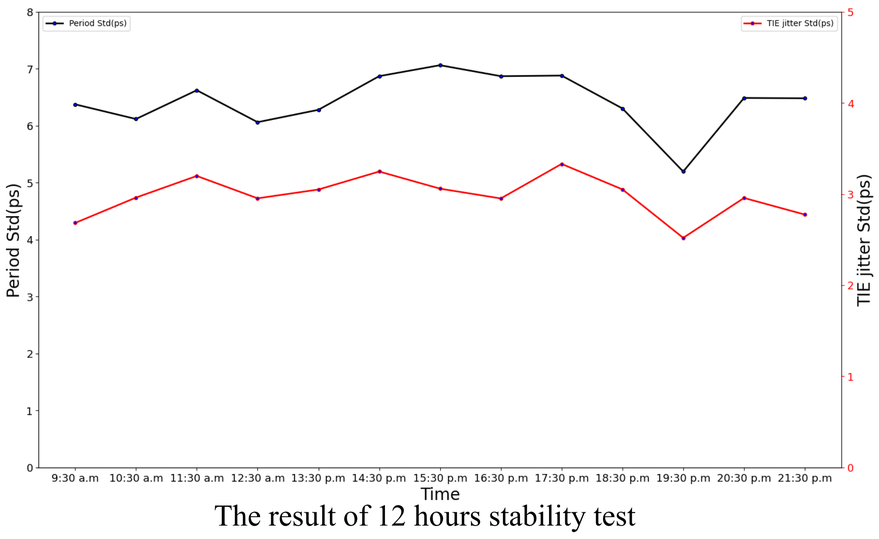
The test of the clock board

A high-precision clock generation and distribution system was tested. The cycle distribution, time interval error (TIE) jitter, and C-C cycle jitter have been tested. Through the test results, we can find that the Std of the period jitter is less than 4.47 ps, the Std of the TIE jitter is less than 2.16 ps, and the Std of the C-C period jitter is less than 7.78 ps. The phase skew of the clocks between different channels is within 100 ps. A 12-hour stability test was also performed on the clock system.



(a) (b) (c)

The testing of a high-precision clock generation and distribution system. (a) the period of the clock; (b) the time interval error (TIE) jitter of the clock; (c) the C-C period jitter of the clock



The result of 12 hours stability test

Conclusion

Test results based on 200 m optical fibers connection:

- Period jitter (Std) : 4.47 ps
- TIE jitter (Std) : 2.16 ps
- C-C period jitter (Std) : 7.78 ps
- Phase skew between channels: within 100 ps

Reference

[1] J. J. Qin, J. W. Li, D. D. Qi, T. Chen, S. Y. Huang, H. Z. Xie, *et al.*, "Design of a high-precision clock distribution and synchronization system," *Nucl. Instrum. Methods Phys. Res. A*, vol 1062, pp. 169198, May. 2024.