

International  
UON Collider  
Collaboration



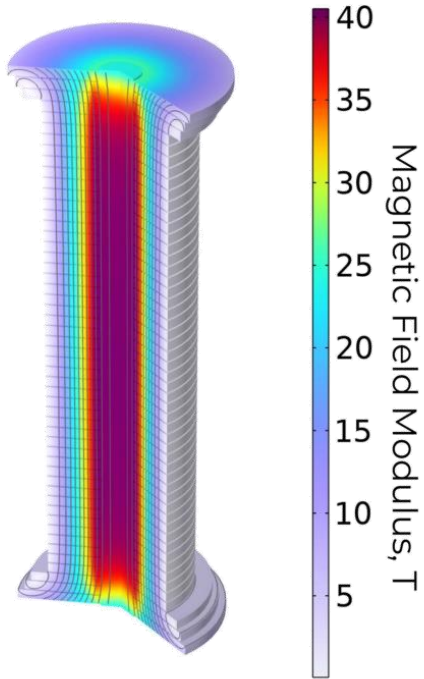
MuCol

# Experimental tests for winding technology of Final Cooling Solenoid

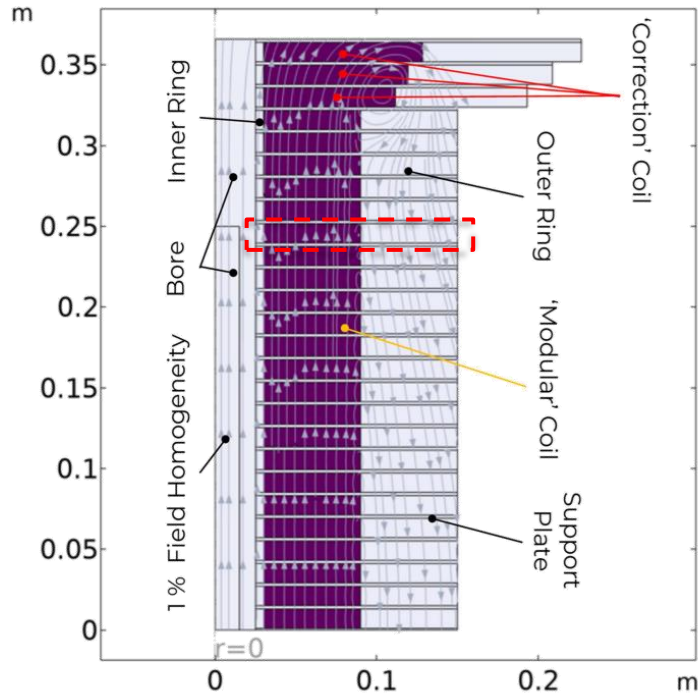
M. Abdel Hafiz

*On behalf of Final Cooling Solenoid working group*

# Final Cooling Solenoid



*B. Bordini & al., 2024*



- 40 T , 50 mm bore diameter
- Each pancake is in a solder matrix to redistribute stress

Proposal for widening a pancake :  
How does that effect the tape properties ?

# Final Cooling Solenoid *Outline*

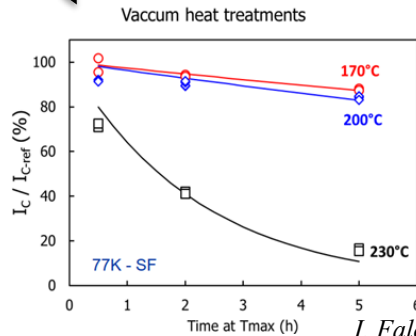
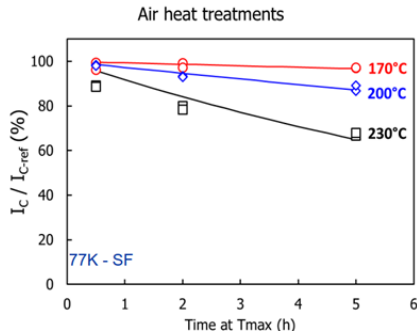
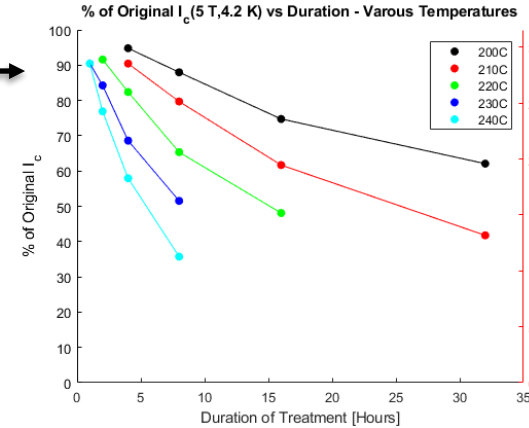
- Effect of Temperature on tape
- Description of the winding
- Effect of the winding proposal on pancake properties
- Chemical etching to control transverse resistance
- Effect of the etching on pancake properties

**All results presented from this study have been performed on a Theva TPL4421**

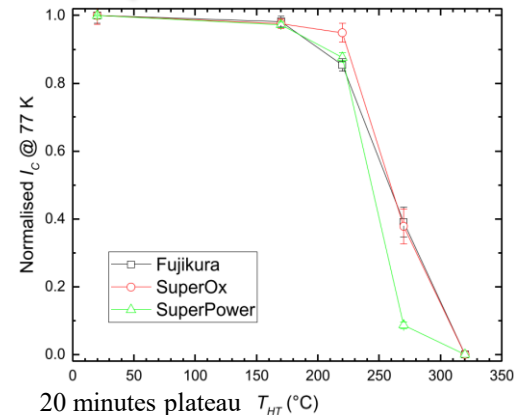
# Temperature influence on $I_C$

## Literature

- $I_C$  degrades with time and temperature
- 2 mechanisms of degradation :
  1. Oxygen-out diffusion from grain boundaries of ReBCO layer
  2.  $T > 250^\circ\text{C} \rightarrow$  Oxygen-out diffusion from grains of ReBCO layer
- Heat treatment cycle does not affect
- Stabilizer thickness is a parameter of degradation
- Depends on the manufacturing process
- Vacuum could have an effect



*I. Falorio (2020)*



*M. Bonura & al. (2022)*

*G. Bradford & al. MT26 (2019)*

# Temperature influence on $I_C$

## *Preparing samples*

### Sample holder :

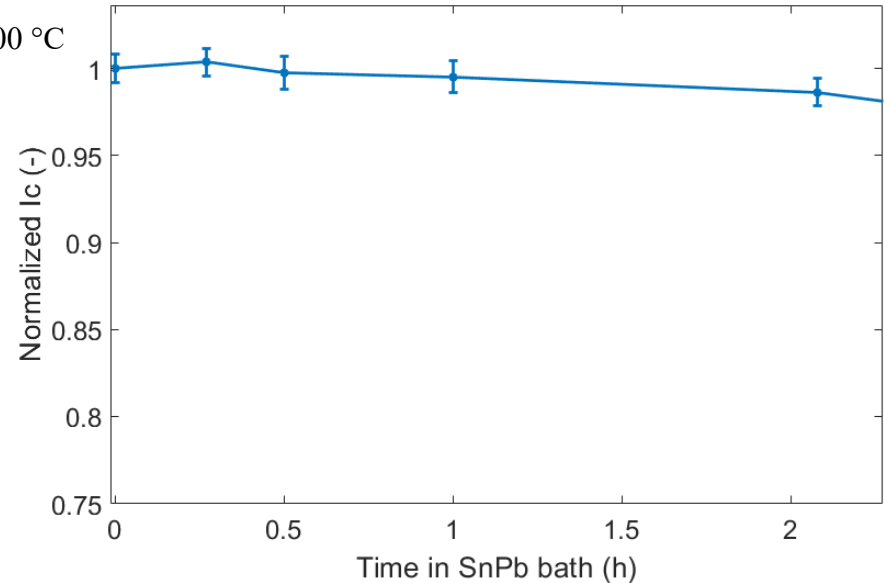
- G10 insulating plate (~ 1 mm)
- Both sides :
  - Cu coating (~75  $\mu\text{m}$ )
  - SnPb coating



Sample Holder

### Sample cycled :

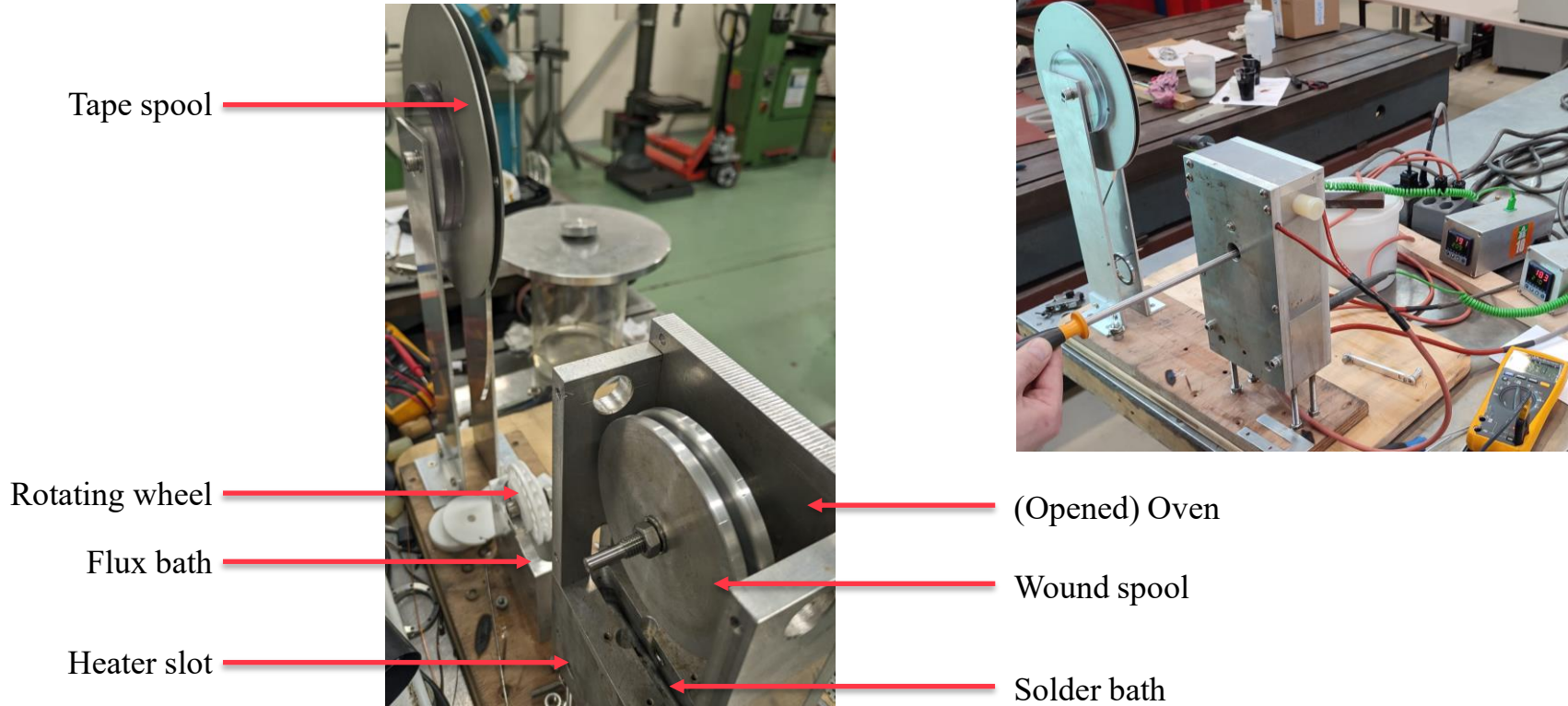
- Coating tape and soldered to the sample holder
- $I_C$  measurement @ 77K
- Heated in solder bath @200 °C
- Cycling process



- Preparing and coating samples do not visibly affect  $I_C$  on measured length
- $I_C$  Degradation of Theva TPL tape < 3% after 2h @200°C in SnPb bath

# Hot winding

## *Winding tool prototype*

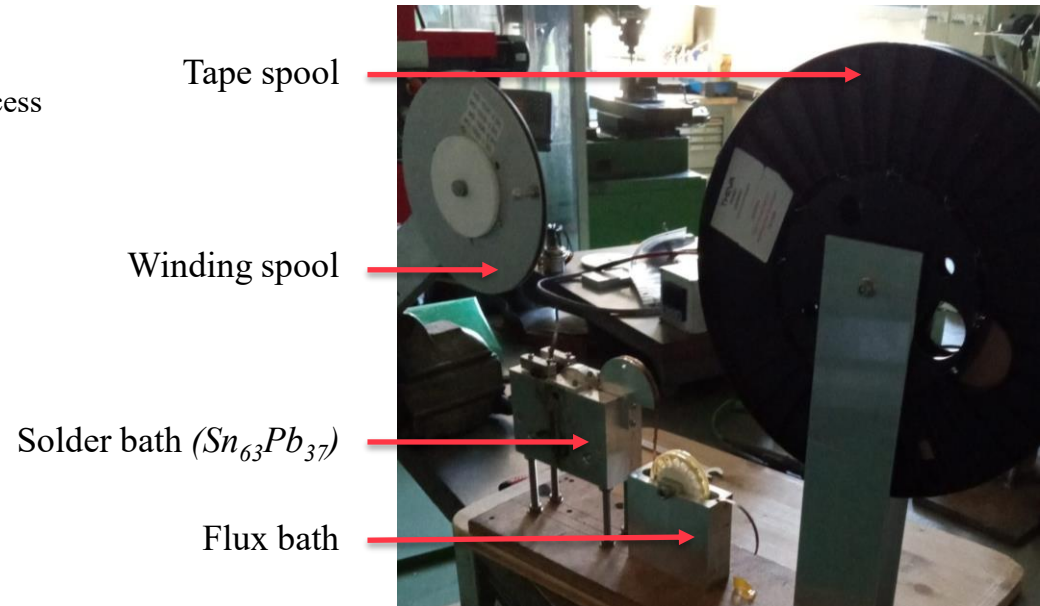


# Hot winding

## *Winding protocol*

### 1. Precoating tape

- Heat up to 200°C to melt SnPb (~15 min)
- Tape passes through flux and solder (~ 10 s)
- Gravity seems to be enough to remove *some* excess of solder
- Precoating tapes allows to :
  - Control coating of tapes
  - Remove flux bath during winding process



# Hot winding

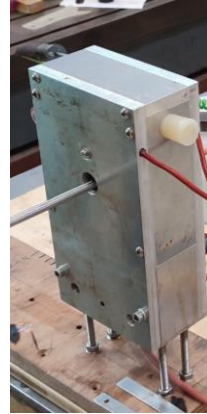
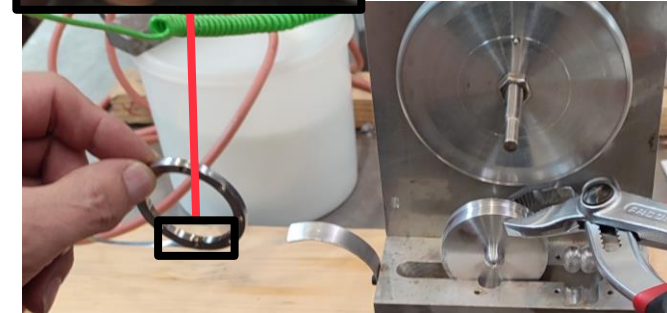
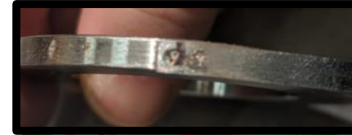
## *Winding protocol*

### 1. Precoating tape

- Heat up to 200°C to melt SnPb (~20 min)
- Tape passes through flux and solder (~ 10 s)
- Gravity seems to be enough to remove *some* excess of solder
- Precoating tapes allows to :
  - Control coating of tapes
  - Remove flux bath during winding process

### 2. Starting winding

- Heat up the oven to 200°C to melt SnPb (~45 min)
- Remove the door & install the mandrel
  - Invar mandrel has been chosen for these tests
    - Invar shrinkage from 473K to 77K is lower than HTS and limiting radial tensile stresses in the pancake during cooling down
    - Invar bounds well and easily to SnPb
  - Tape is pre-installed on the mandrel
    - Hooked in a groove
    - Spot welded to the mandrel
- Close the door and reheat to 200°C (~20 min)





# Hot winding

## *Winding protocol*

### 1. Precoating tape

- Heat up to 200°C to melt SnPb (~20 min)
- Tape passes through flux and solder (~ 10 s)
- Gravity seems to be enough to remove *some* excess of solder
- Precoating tapes allows to :
  - Control coating of tapes
  - Remove flux bath during winding process

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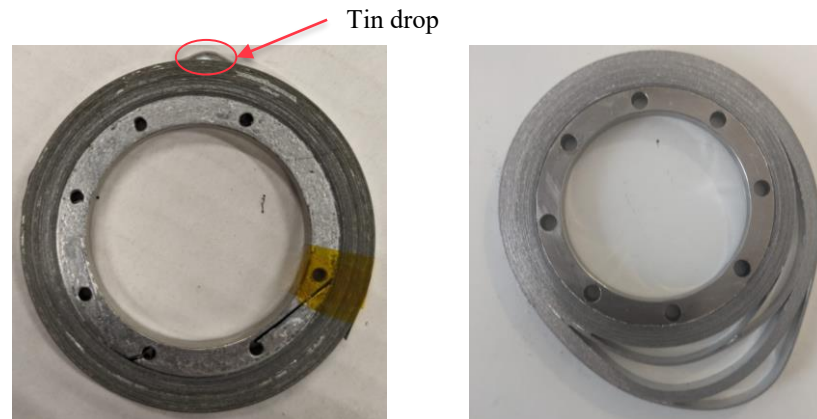
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  - Tape is pre-installed on the mandrel
    - Hooked in a groove
    - Spot welded to the mandrel
- Close the door and reheat to 200°C (~20 min)

### 3. Winding pancake

- No controlled tension is applied nor measured
- Winding duration for 15m of tape took **20 to 40 minutes**

### 4. Cooling down

- To room temperature (~ 1h)



**2h of heating for the tape**  
**4 Pancakes successfully prepared**

# Pancake Properties

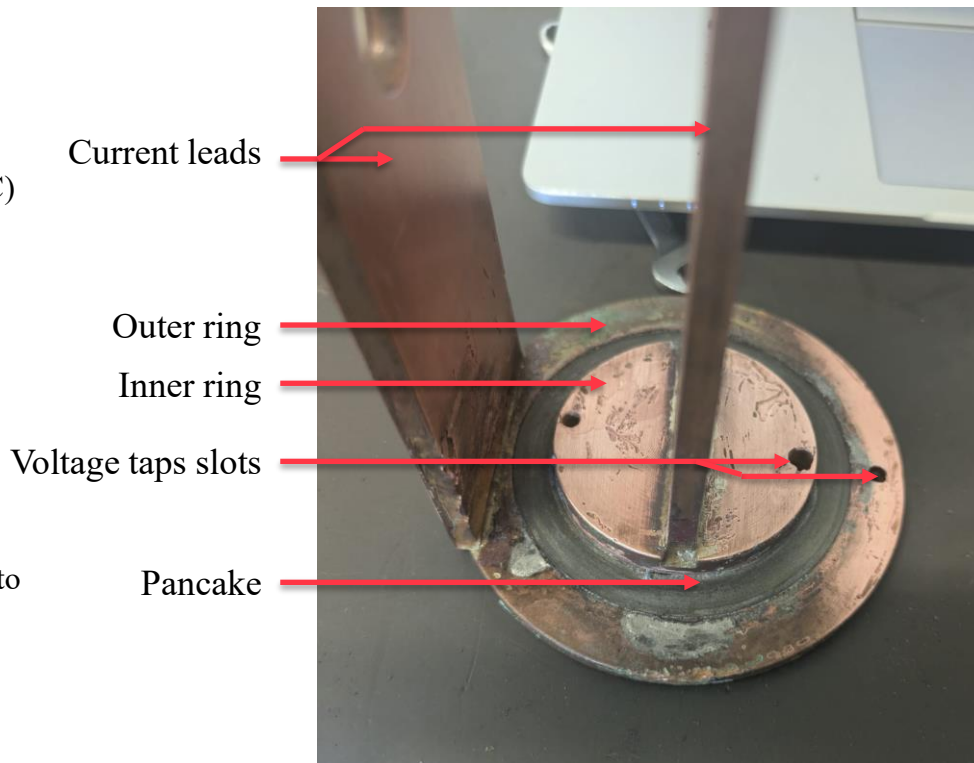
## *Preparation for experiment*

### 1. Installing current leads

- Ensure electrical contact from rings to pancake without melting the pancake (183°C)
  - Low temperature solder ( $\text{Bi}_{58}\text{Sn}_{42}$  138°C)

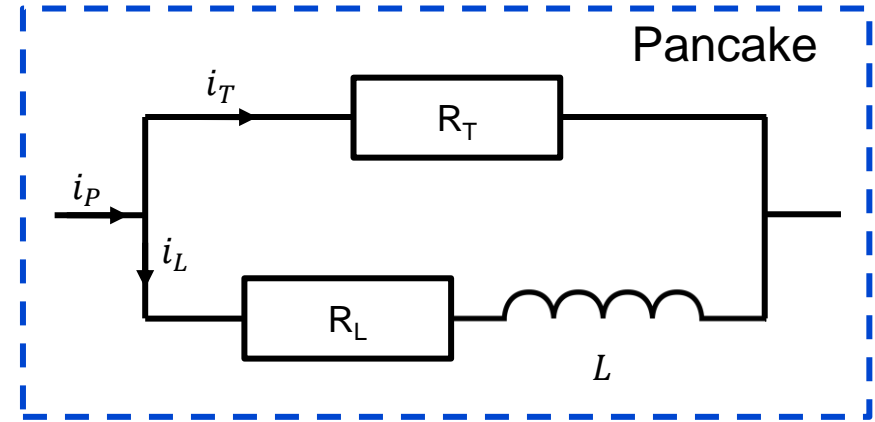
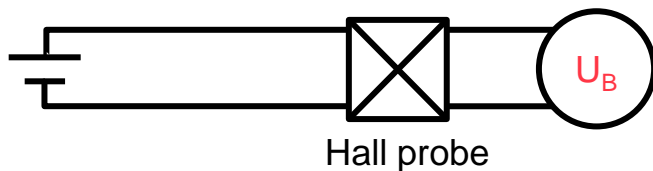
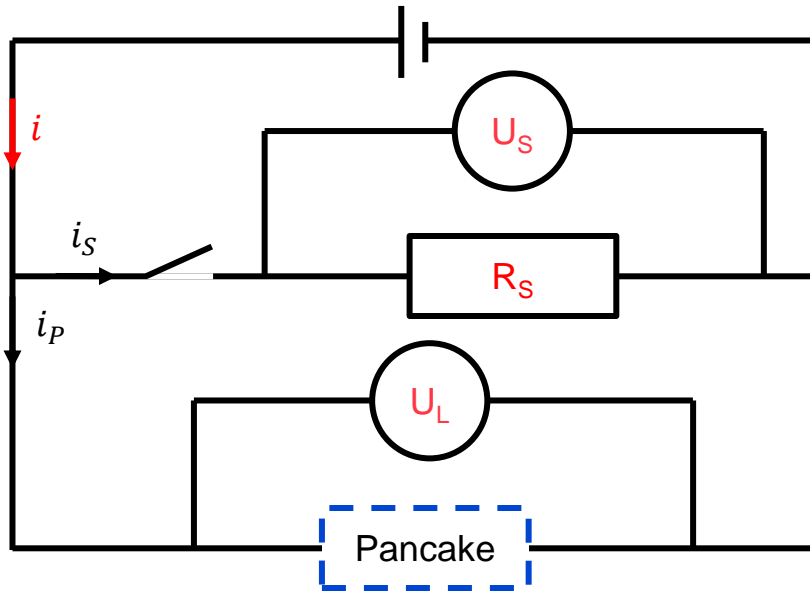
### 2. Tests performed @77K

- Measure critical current  $I_C$  of the pancake
  - Steady state study with low ramp rate
- Measure time constant  $\tau$ 
  - Steps current
- Hall Probe located in the center of the pancake to measure central field



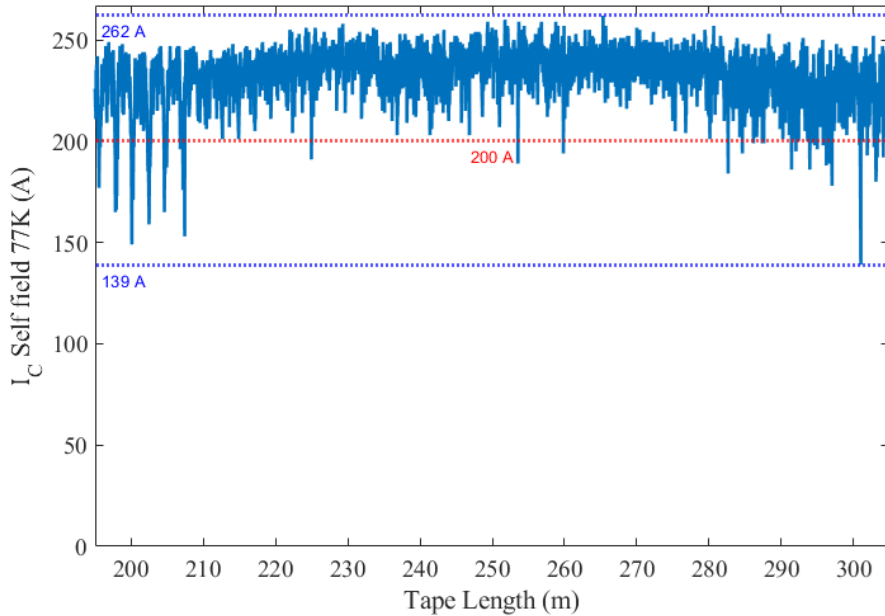
# Pancake Properties

## *Experiment Scheme*



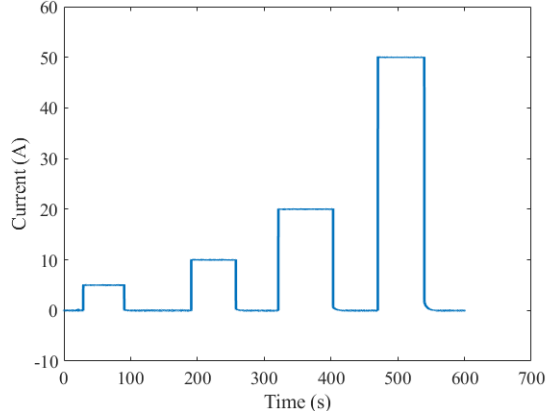
$i$	Power supply current
$i_S$	Shunt current
$i_P$	Pancake current
$i_T$	Transverse ( <i>radial</i> ) current
$i_L$	Lengthwise ( <i>azimuthal</i> ) current
<hr/>	
$U_S$	Shunt voltage
$U_L$	Pancake voltage
$U_B$	Hall Probe Voltage

Tape  $I_C$  map

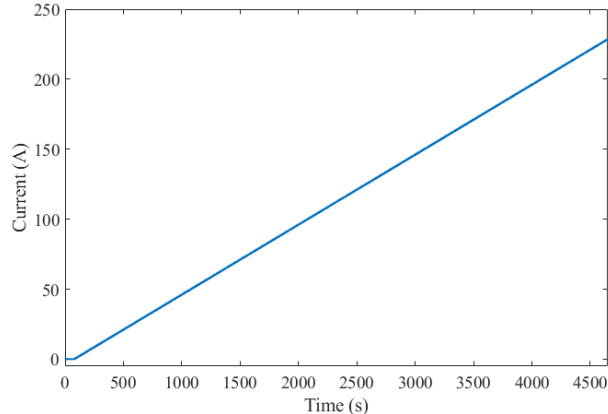


	Pancake 1	Pancake 2	Pancake 3	Pancake 4
Inner radius	24 mm	24 mm	30 mm	30 mm
Outer radius	30.2 mm	31.6 mm	35.6 mm	35.6 mm
Nb of turns	74	84	64	64
Mean thickness per tape	84 $\mu\text{m}$	90 $\mu\text{m}$	88 $\mu\text{m}$	88 $\mu\text{m}$
Inductance	479 $\mu\text{H}$	606 $\mu\text{H}$	474 $\mu\text{H}$	474 $\mu\text{H}$

# Pancake Properties



Transient study: Steps at different current

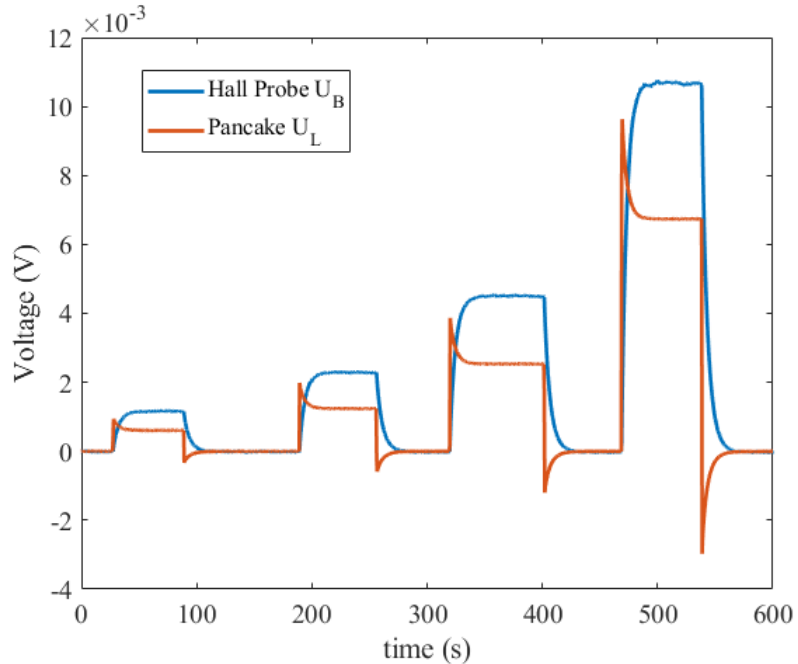


Steady state study : ramp of 0.05A/s

	Pancake 1	Pancake 2	Pancake 3	Pancake 4
Inner radius	24 mm	24 mm	30 mm	30 mm
Outer radius	30.2 mm	31.6 mm	35.6 mm	35.6 mm
Nb of turns	74	84	64	64
Mean thickness per tape	84 $\mu\text{m}$	90 $\mu\text{m}$	88 $\mu\text{m}$	88 $\mu\text{m}$
Inductance	479 $\mu\text{H}$	606 $\mu\text{H}$	474 $\mu\text{H}$	474 $\mu\text{H}$

# Pancake Properties

## *Transient Study*



$\tau$ (s)	Charge	Discharge
5 A	4.87	4.92
10 A	4.70	5.05
20 A	4.78	5.02
50 A	4.60	4.83

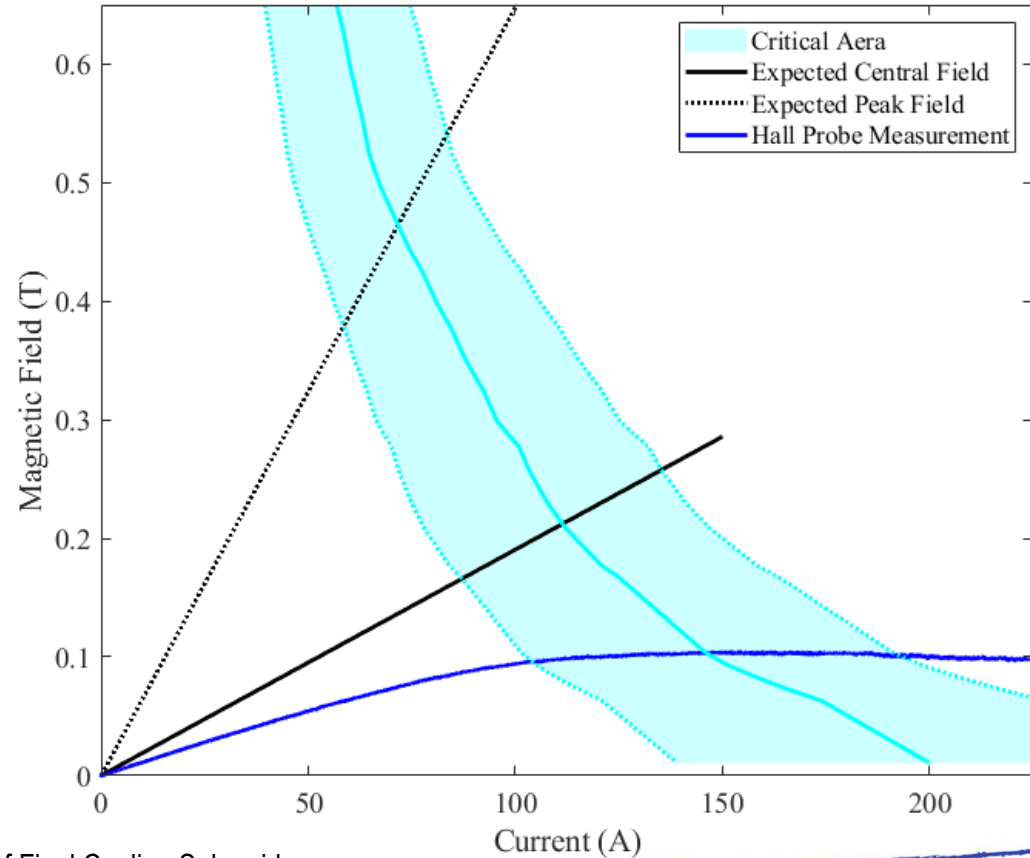
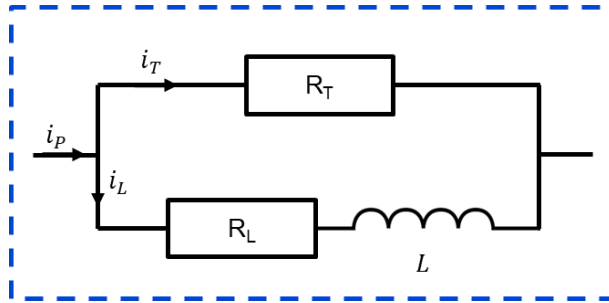
$$\tau = \frac{L}{R_{eq}} \text{ with } R_{eq} = \int \frac{\rho_{eq}}{2\pi r w} dr$$

	$\tau$ (s)	$\rho_{eq}$ (m $\Omega$ . mm)
Pancake 1	5.2	10.1
Pancake 2	4.8	11.5
Pancake 3	1.6	43.5
Pancake 4	3.1	22.5

# Pancake Properties

## *Steady State Study*

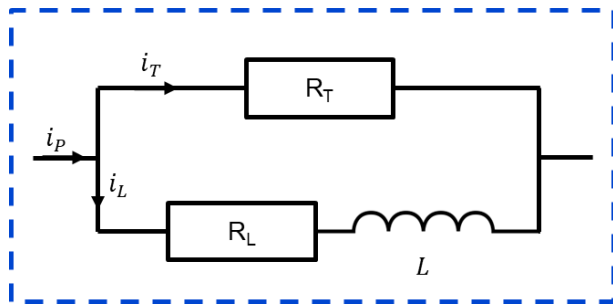
Pancake



# Pancake Properties

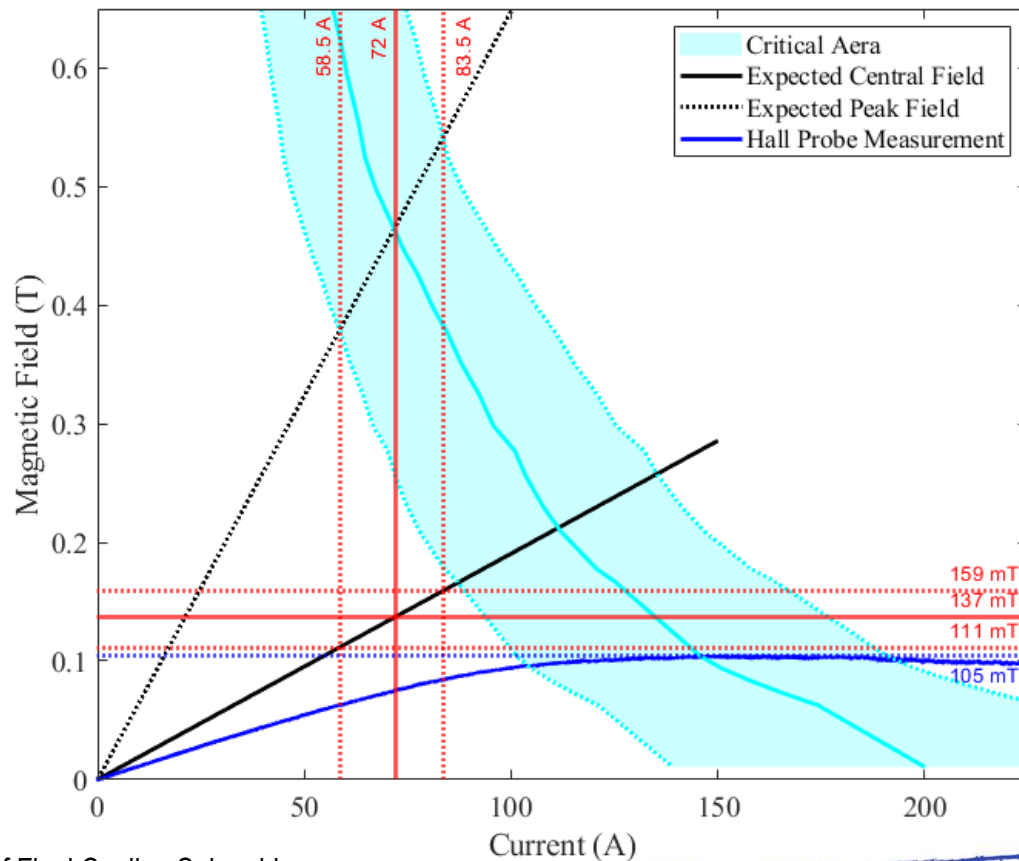
## *Steady State Study*

Pancake



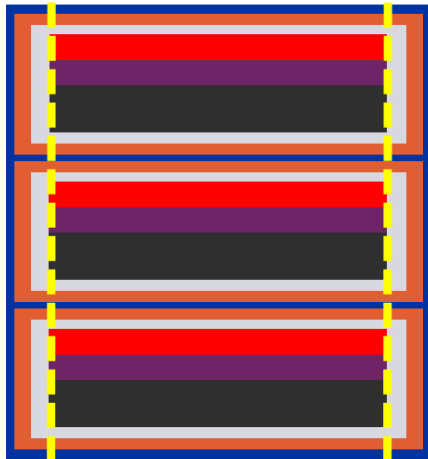
'Maximum' Field (mT)	Expected	Measured
Pancake 1	129	115 ( <b>89%</b> )
Pancake 2	137	105 ( <b>77%</b> )
Pancake 3	93	72 ( <b>77%</b> )
Pancake 4	93	68 ( <b>73%</b> )

**75 % of the expected maximum field**





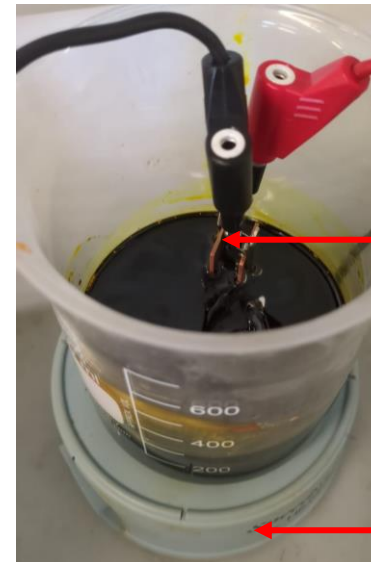
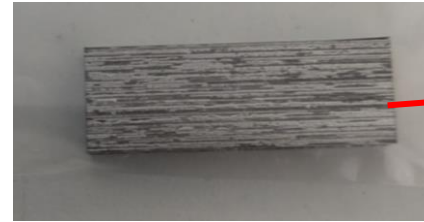
# Chemical Etching



*Scheme of tapes stack cross section*

Layer properties for Theva  
TPL4421 4 mm width  
(*tape property sheet*)

- ~ 10  $\mu\text{m}$  Cu stabilizer
- ~ 1  $\mu\text{m}$  Ag
- ~ 4.5  $\mu\text{m}$  HTS layer
- ~ 3.5  $\mu\text{m}$  buffer layers  
(*insulating MgO*)
- ~ 48  $\mu\text{m}$  C-276 substrate
- ~ 15  $\mu\text{m}$  Sn-Pb solder  
(*estimation*)

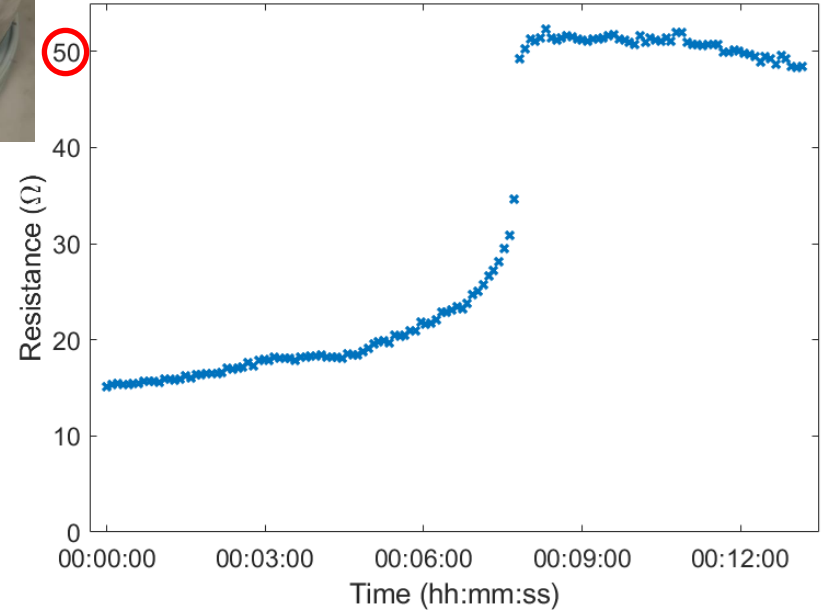
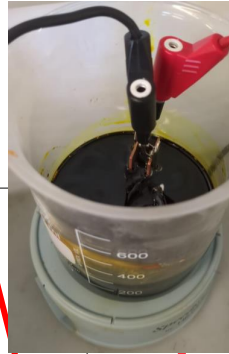
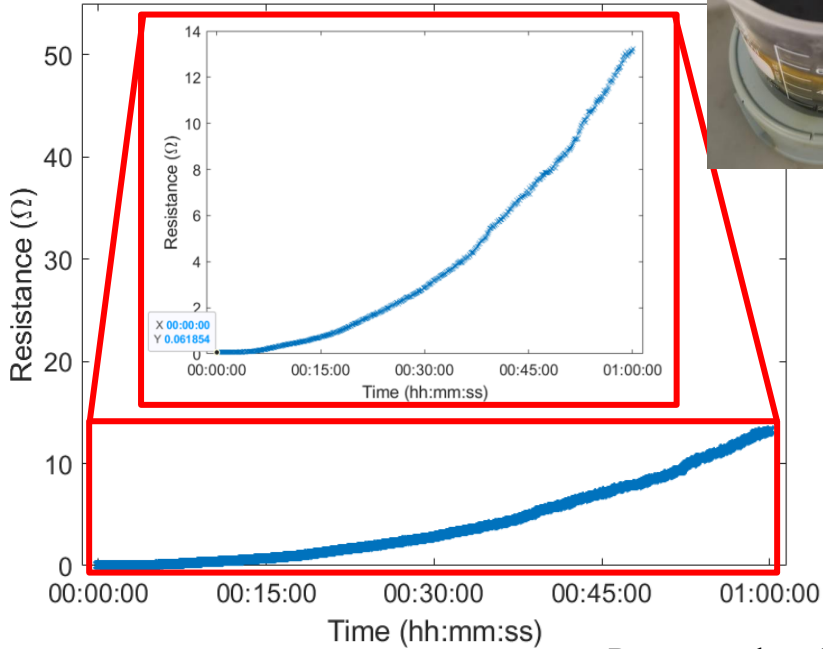


Ohmmeter

Magnetic stirrer

**Chemically ( $\text{FeCl}_3$  etching) remove both side of the tape to increase resistance**

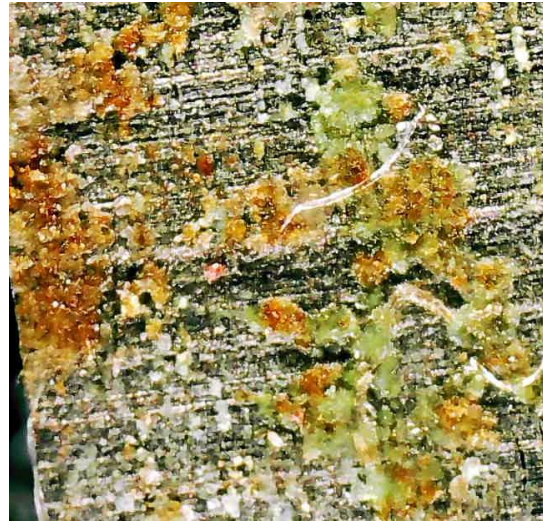
# Chemical Etching



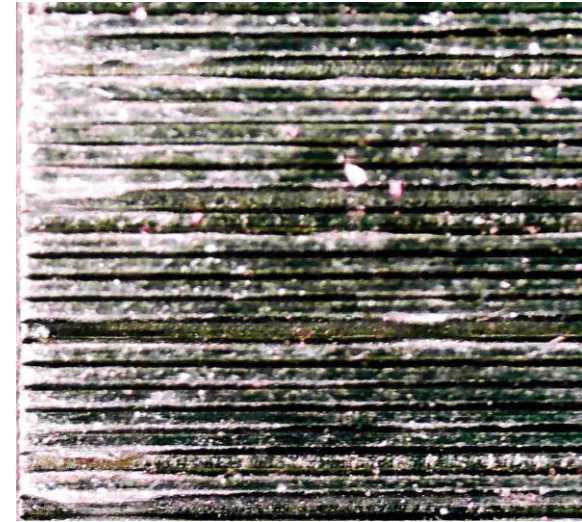
Program shut down for a few minutes



$< 0.05 \Omega$



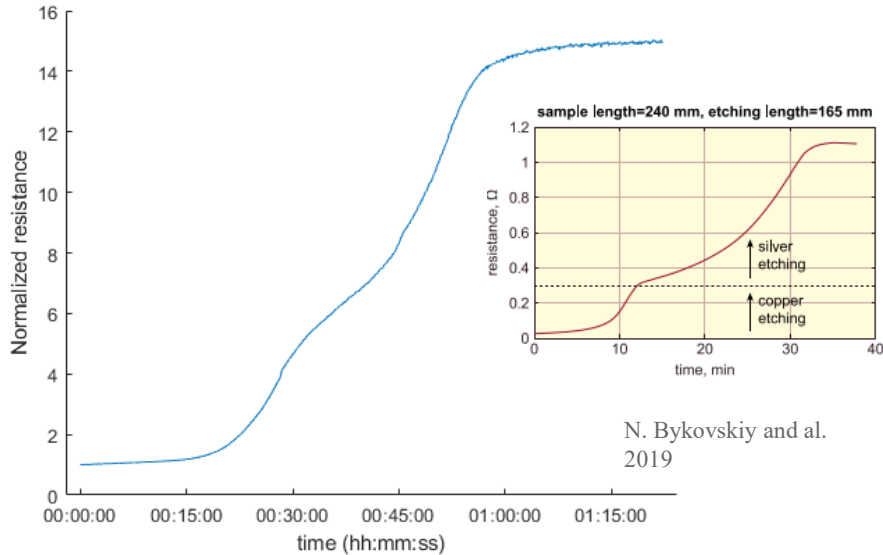
$0.5 \Omega$



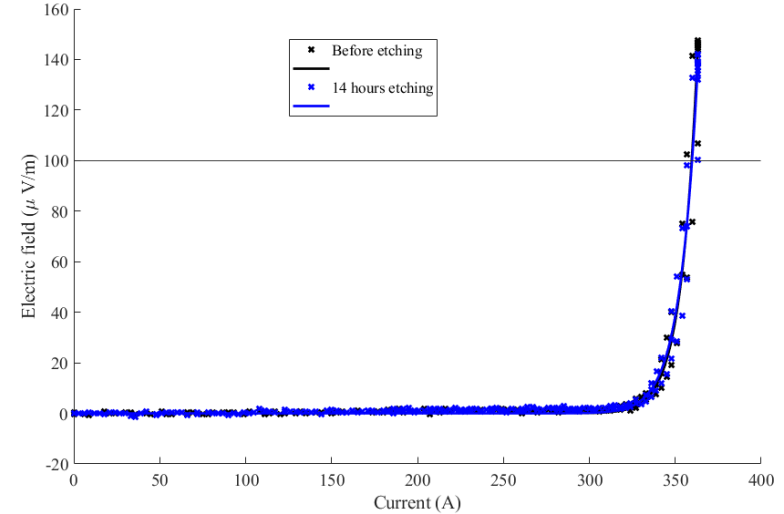
$200 \Omega$

**Resistance @77K increased by 4 order of magnitude after etching  
What about  $I_C$  ?**

Two tapes soldered to each other

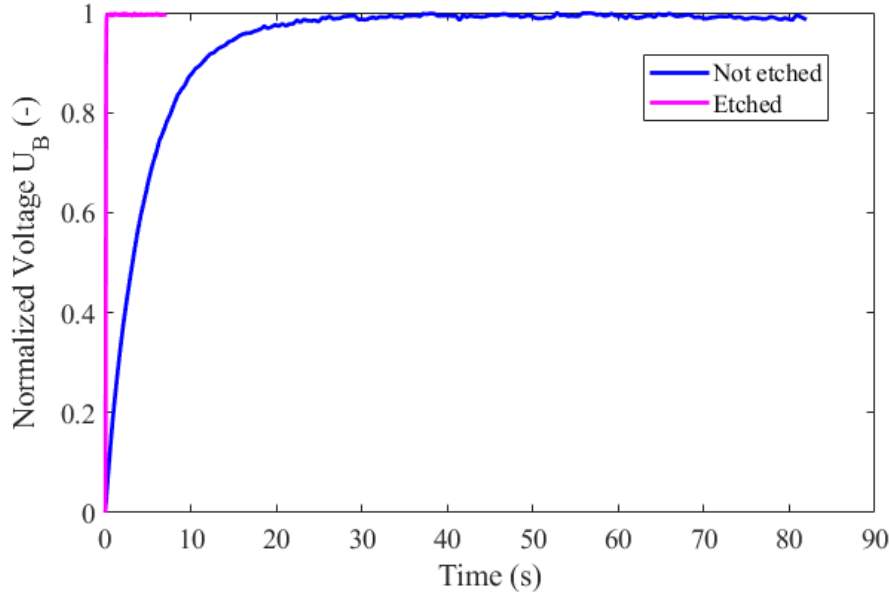


- Cu removed in  $\sim 30$ min
- Ag removed (?) in  $\sim 1$ h



**Etching seems to have no effect on  $I_C$  need to be determined  
Further experiments required to confirm**

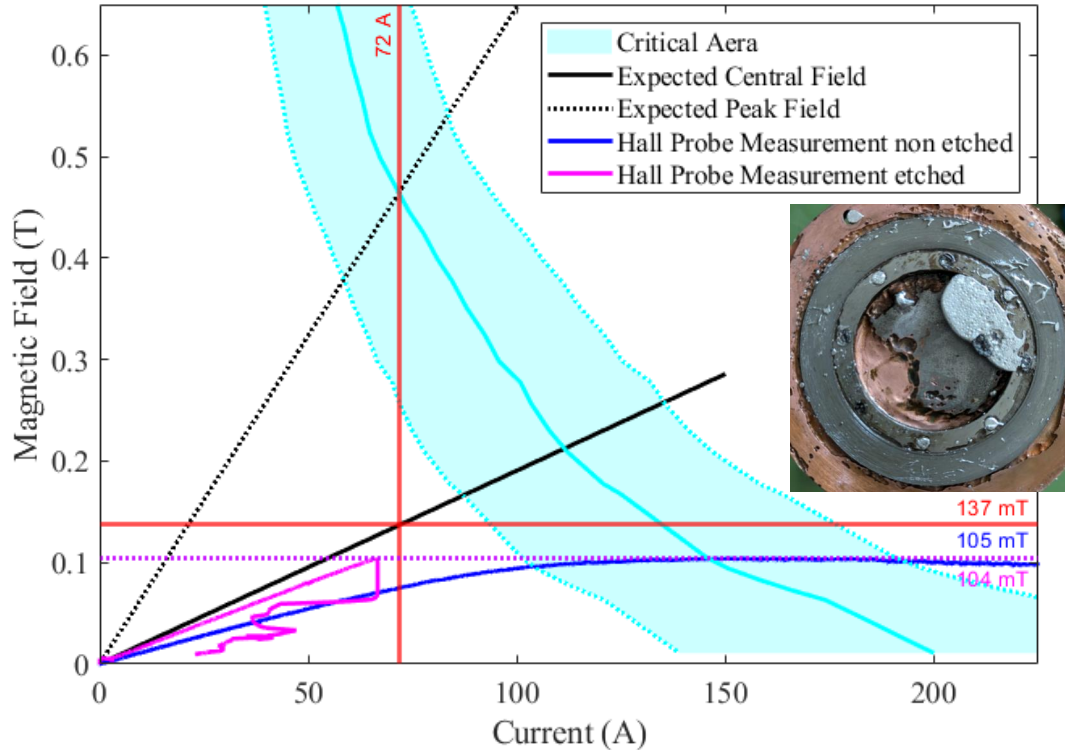
# Chemical Etching *Pancake Properties*



		$\tau$ (s)	$\rho_{eq}$ (m $\Omega$ .mm)
Pancake 1	raw	5.2	10.1
	etched	0.4	268
Pancake 2	raw	4.8	11.5
	etched	< 0.04	> 1384
Pancake 3	raw	1.6	43.5
	etched	< 0.02	> 3480
Pancake 4	raw	3.1	22.5
	etched	< 0.02	> 3480

**Time constant decreased by a factor 100**

# Chemical Etching *Pancake Properties*



'Maximum' Field (mT)		Measured	
Pancake 1	Non etched	115	<b>(89%)</b>
129	Etched	98	<b>(76%)</b>
Pancake 2	Non etched	105	<b>(77%)</b>
137	Etched	104	<b>(76%)</b>
Pancake 3	Non etched	72	<b>(77%)</b>
93	Etched	50	<b>(54%)</b>
Pancake 4	Non etched	68	<b>(73%)</b>
93	Etched	52	<b>(56%)</b>

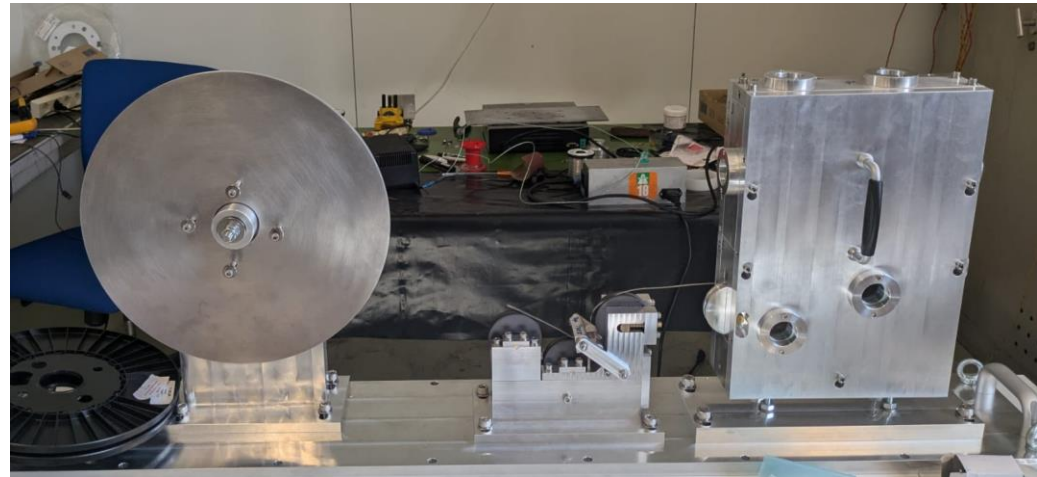
**- 15 % of from the non-etched maximum field**

**These conclusions can only be assessed for Theva TPL 4421 tapes :**

- $I_C$  of the tape degrades by less than **5% after 2h in solder bath**
- We have no control of current distribution in the pancake
  - It is difficult to define a critical current for the pancake
  - The magnetic field produced is about **25% lower than expected**
- Chemical etching increases the transverse resistance by about **4 order of magnitude** and **does not seem to affect  $I_C$** 
  - Concerning the pancakes it reduces the time constant by **at least a factor 100**
  - The magnetic field is reduced **by another 15%**
    - It is not clear whether that is the effect of etching, or the presence of defects already here highlighted by the removal of the stabilizer
  - *Thermo-mechanical tests are needed to characterize the properties of an etched stack*

## On going work :

- New winding tool has been machined and assembled for further pancake production  
(*F. Sanda, A. Kolehmainen, A. Dudarev, A. Dallochio*)

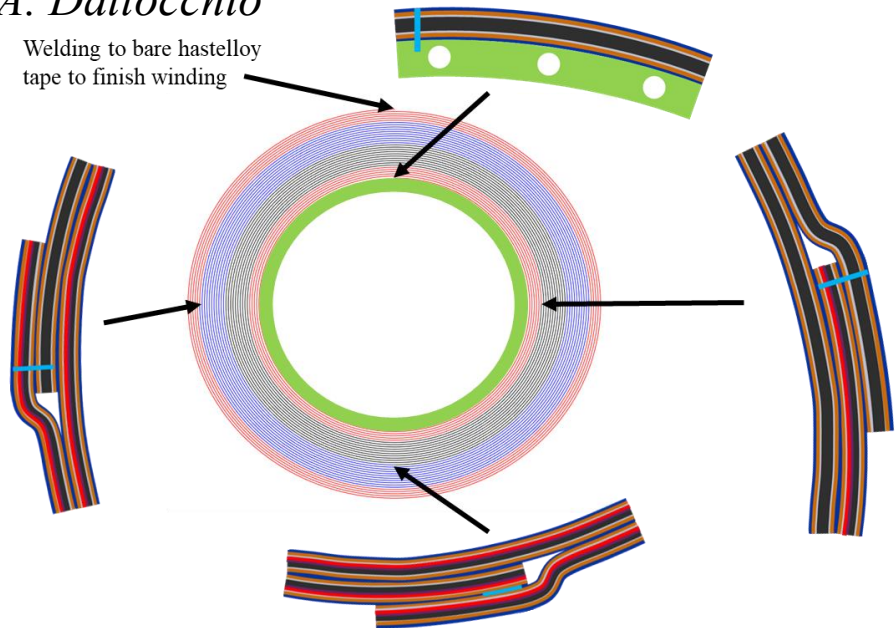


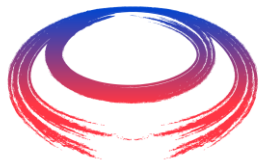


## On going work :

- New winding tool has been machined and assembled for further pancake production  
(*F. Sanda, A. Kolehmainen, A. Dudarev, A. Dalocchio*)
- Problematic of the joints
  - Tape to inner/outer ring
  - Tape to outer ring
    - Layer jump

- Mandrel
- Copper/Hastelloy tape (inner)
- HTS tape inwards
- HTS tape outwards
- Copper/Hastelloy tape (outer)





International  
UON Collider  
Collaboration



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Thank you for your attention

M. Abdel Hafiz

*On behalf of Final Cooling Solenoid working group*

# Temperature influence on $I_C$

Sample cycled :

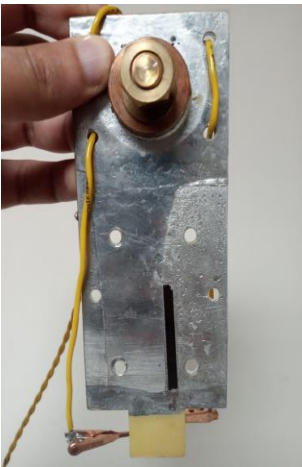
- Preparing sample

Sample holder : •  $I_C$  measurement @ 77K

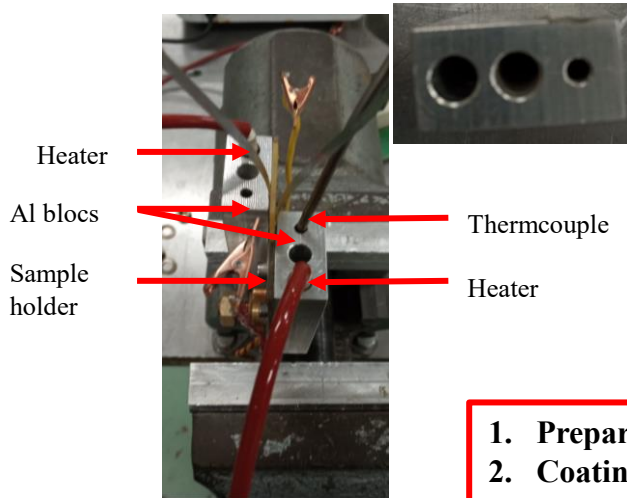
- G10 insulating plate (~1 mm)
- Both sides :
  - Cu coating (~75  $\mu\text{m}$ )
  - SnPb coating
  - Extremity etched for clamping voltage tapes

Sample preparation :

1. Screw Al blocs to sample holders
2. Heat up to 200°C to melt SnPb (~10 min)
3. Insert tape within groove (~1 min)
4. Wait for cooling down (~10 min)



Sample Holder



Sample Preparation



Voltage tapes

*Bloc and heaters @200°C for 25 minutes for test*

1. Preparing sample does not degrade  $I_C$  of measured length
  2. Coating sample does not visibly affect  $I_C$
- @77K**

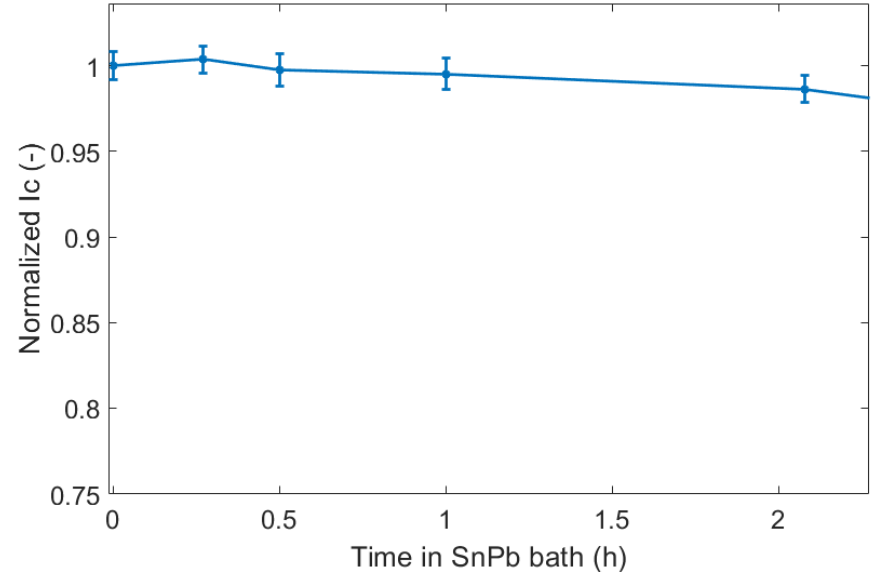
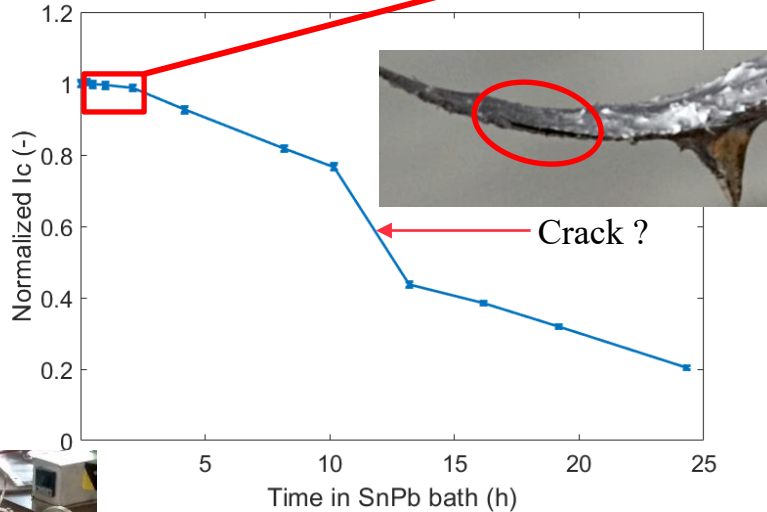
# Temperature influence on $I_C$

## *Experiment*

Sample cycled :

- Preparing sample
- $I_C$  measurement @ 77K
- Heated in solder bath @200 °C
- Cycling process

$I_0 = 190$

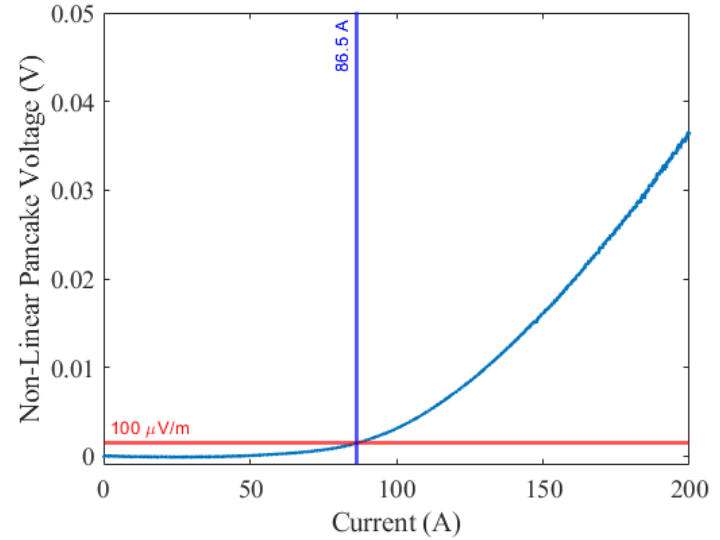
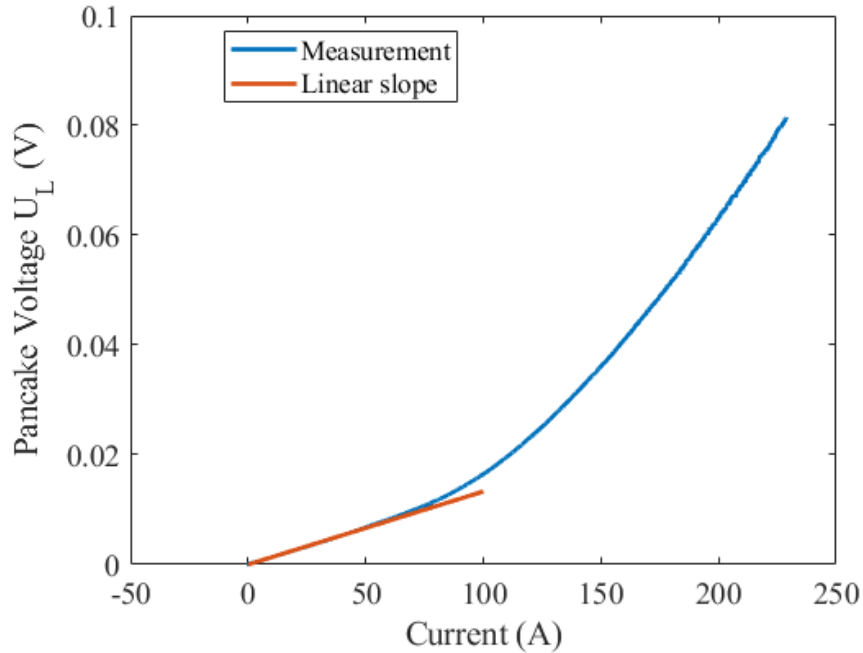


**Degradation of Theva TPL tape < 2% after 2h @200°C in SnPb bath**

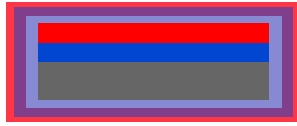


Solder bath

# Pancake Properties



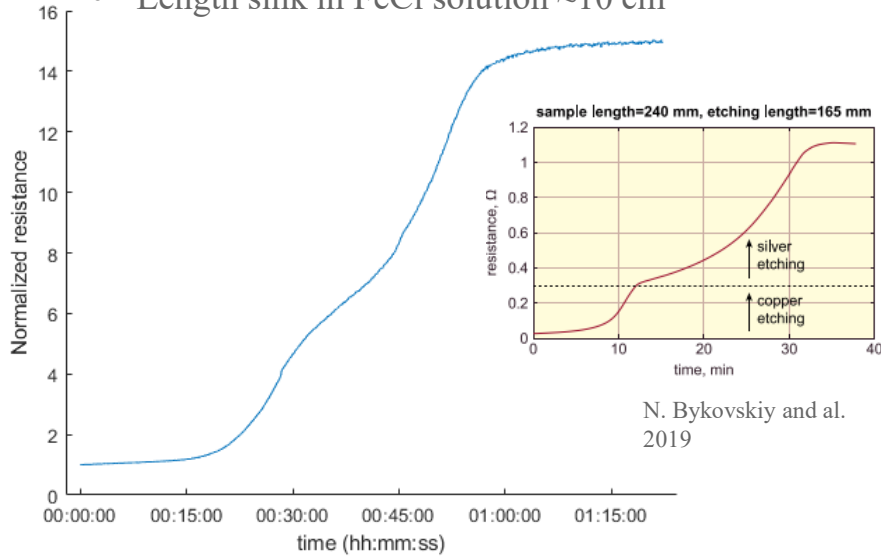
	Critical Current (A)	Expected	Measured
Pancake 1	75	54	
Pancake 2	72	86	
Pancake 3	76	53	
Pancake 4	76	143	



Single tape

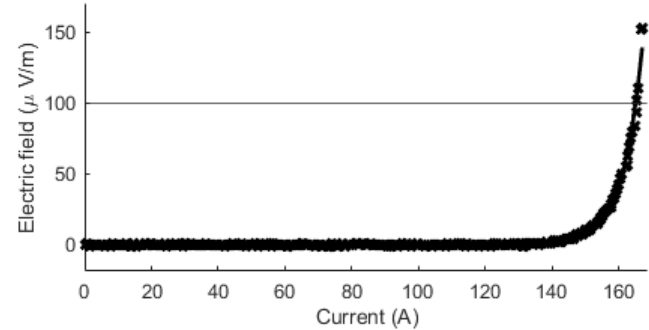
How much time needed to remove copper from side ?

- Lengthwise resistance measured in FeCl @ room temperature
- Length sink in FeCl solution ~10 cm



- Cu removed in ~30min
- Ag removed (?) in ~ 1h

- $I_C$  measured @77K at the end of R measurements (~ 1h20)



- Degradation < 20%

**Single tape still superconductive after removing Cu and Ag(?) (1h20) in FeCl**

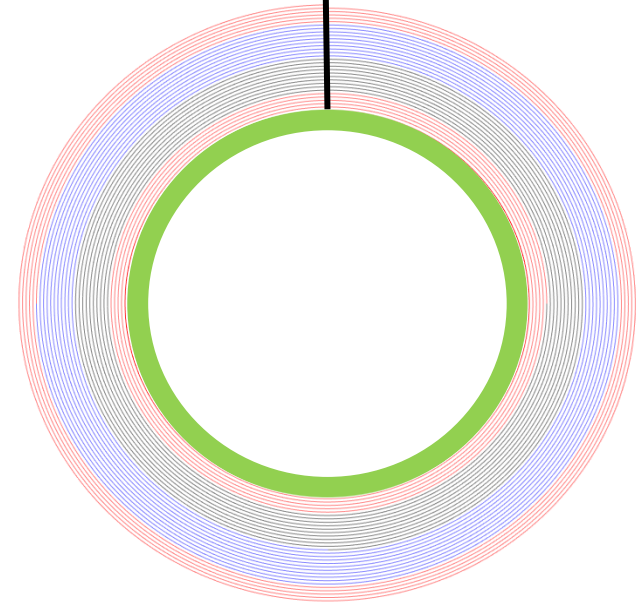
**Further experiments required to confirm**

**According to N. Bykovskiy, depends on the tape**

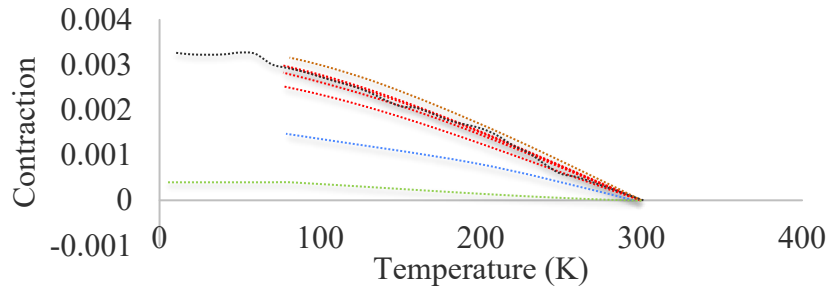
# Mandrel

- Mandrel thermal shrinkage be lower than tape

- Only lengthwise (tape) thermal shrinkage found



Thermal Shrink



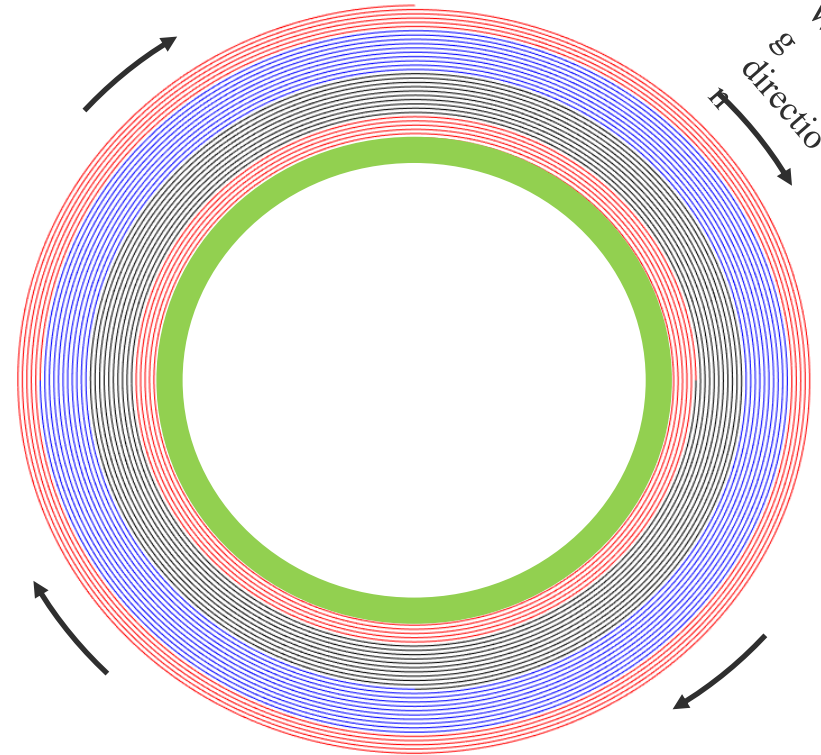
● HTS   
 ● Copper   
 ● Ti   
 ● Hasteloy   
 ● Invar

## • Different areas in pancake

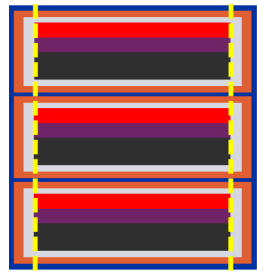
- Mandrel (invar)
- Copper/Hastelloy tape (inner)
- HTS tape inwards
- HTS tape outwards
- Copper/Hastelloy tape (outer)

## • Joints

- Connections should handle 200°C during winding
- Spot welding Hastelloy/Hastelloy and gluing copper/copper are retained methods
  - Introducing local defect
  - Is it mechanically fragile ?
- These steps can all be done before winding (*not necessarily preferably*)









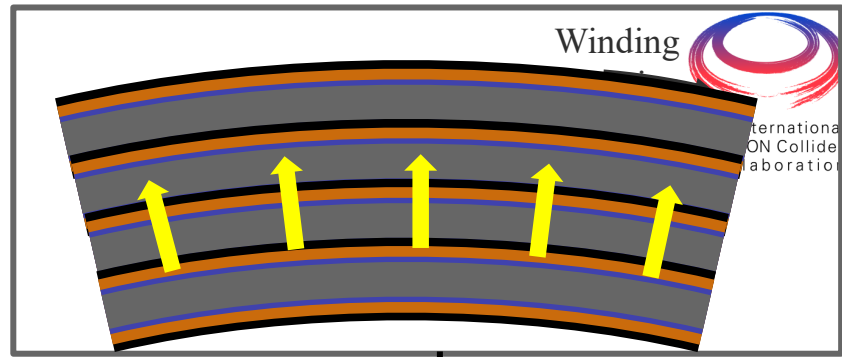




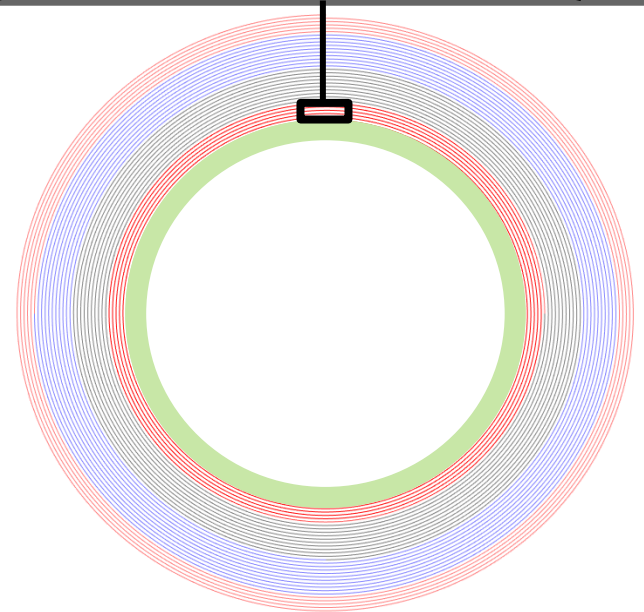
Scheme of tapes stack cross section

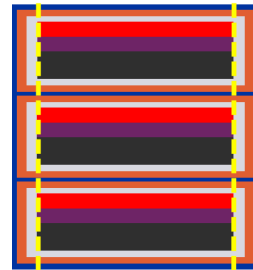
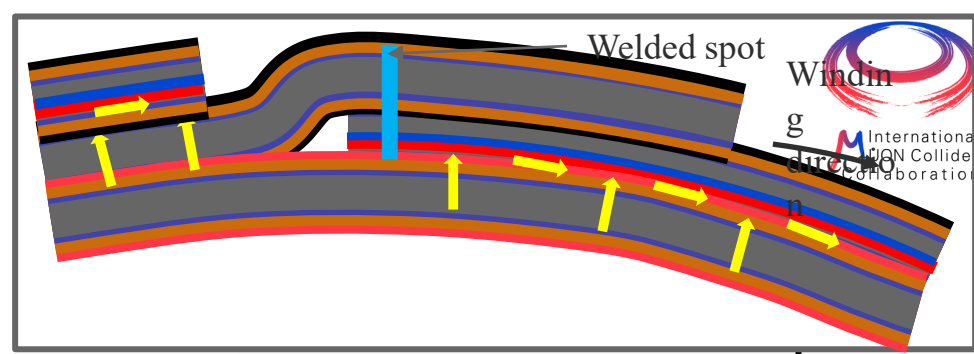
Layer properties for Theva  
TPL4421 4 mm width  
(tape property sheet)

-  ~ 10  $\mu\text{m}$  Cu stabilizer
-  ~ 1  $\mu\text{m}$  Ag
-  ~ 4.5  $\mu\text{m}$  HTS layer
-  ~ 3.5  $\mu\text{m}$  buffer layers  
(insulating MgO)
-  ~ 48  $\mu\text{m}$  C-276 substrate
-  ~ 15  $\mu\text{m}$  Sn-Pb solder  
(estimation)



- First turns with hastelloy/copper tape (without HTS)
  - Redistributing stress
  - Electrical connection
  - **Calculations** to estimate  $n^\circ$  of turns and acceptable stresses (?)
  - Resistance  $\sim 0.1 \mu\Omega$  per turn

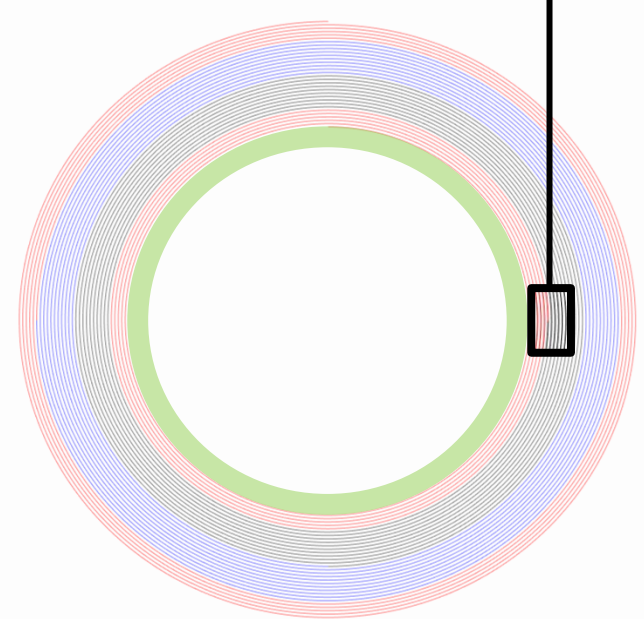




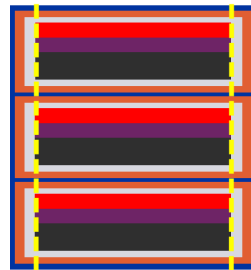
Scheme of tapes stack cross section

Layer properties for Theva TPL4421 4 mm width  
(tape property sheet)

- ~ 10  $\mu\text{m}$  Cu stabilizer
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- ~ 3.5  $\mu\text{m}$  buffer layers  
(insulating MgO)
- ~ 48  $\mu\text{m}$  C-276 substrate
- ~ 15  $\mu\text{m}$  Sn-Pb solder  
(estimation)



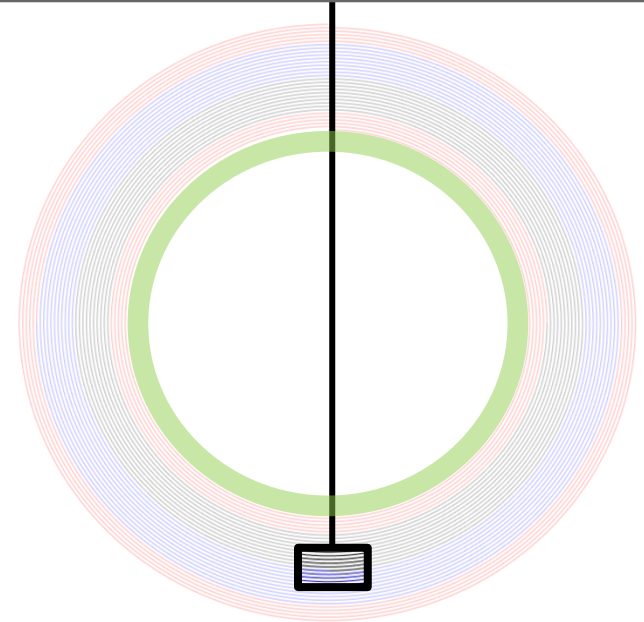
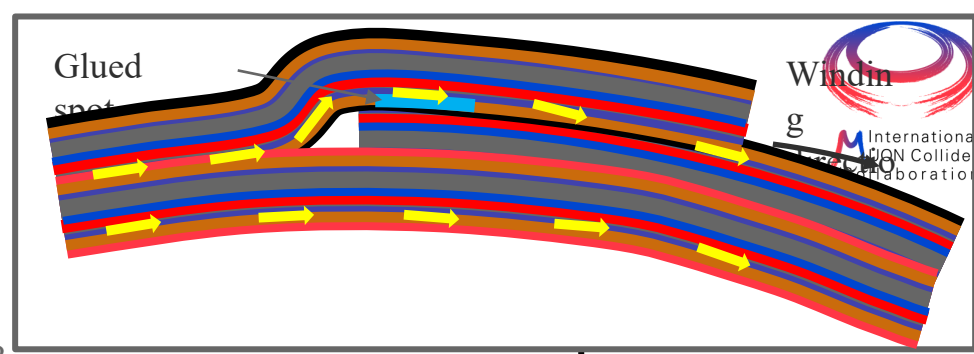
- Where to perform layer jump ?
  - At the beginning to save material in case of failing ?
  - At lowest magnetic field location to reduce stresses ?
- Can be glued
- Resistance  $< 2 \mu\Omega$  for 5 mm contact

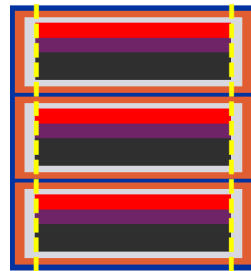
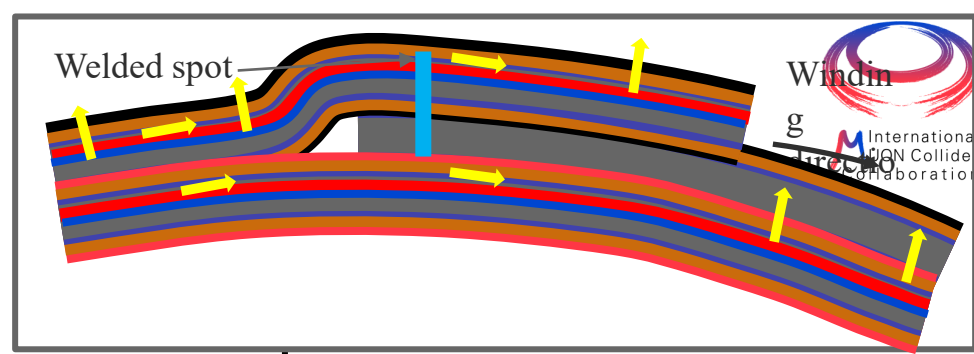


Scheme of tapes stack cross section

Layer properties for Theva TPL4421 4 mm width  
(tape property sheet)







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- ~ 3.5  $\mu\text{m}$  buffer layers (insulating MgO)
- ~ 48  $\mu\text{m}$  C-276 substrate
- ~ 15  $\mu\text{m}$  Sn-Pb solder (estimation)

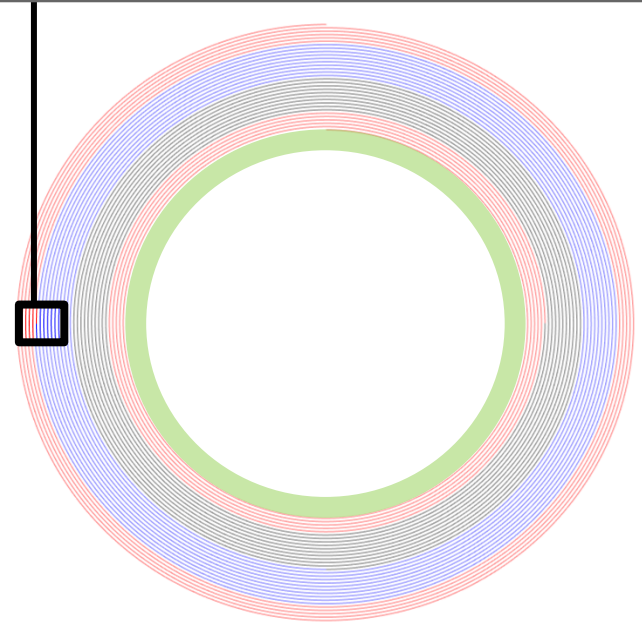


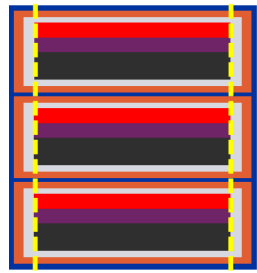


Scheme of tapes stack cross section







Layer properties for Theva  
TPL4421 4 mm width  
(tape property sheet)

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(insulating MgO)
-  ~ 48  $\mu\text{m}$  C-276 substrate
-  ~ 15  $\mu\text{m}$  Sn-Pb solder  
(estimation)

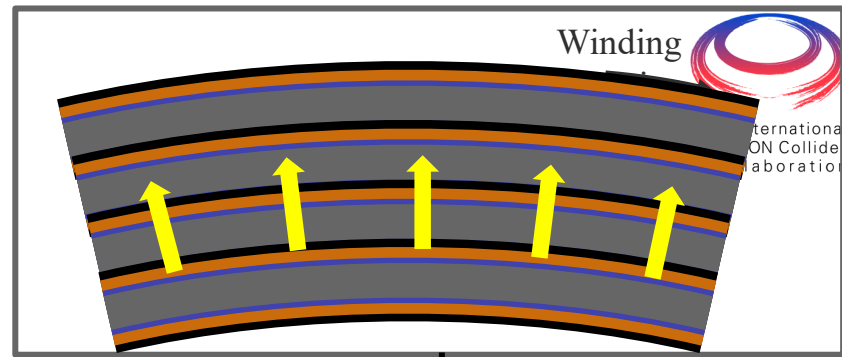




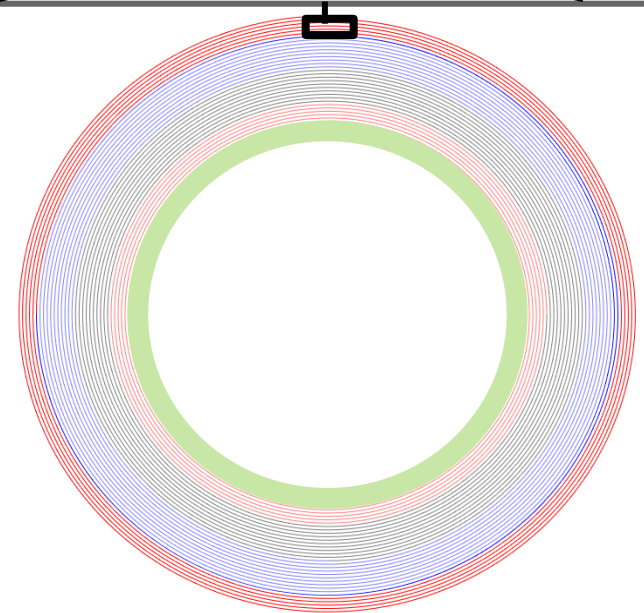
Layer properties for Theva TPL4421 4 mm width  
(tape property sheet)

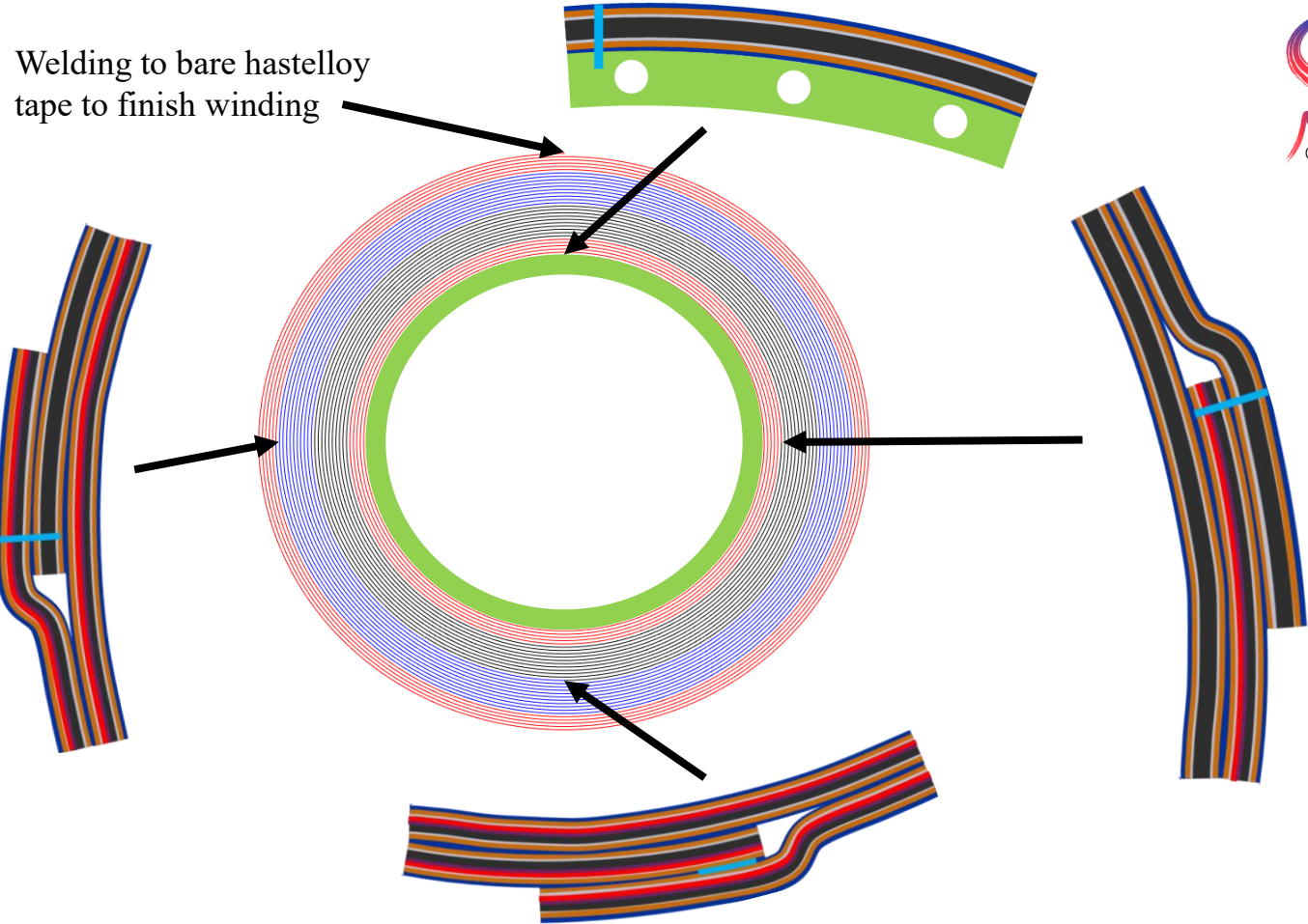
-  ~ 10  $\mu\text{m}$  Cu stabilizer
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(estimation)

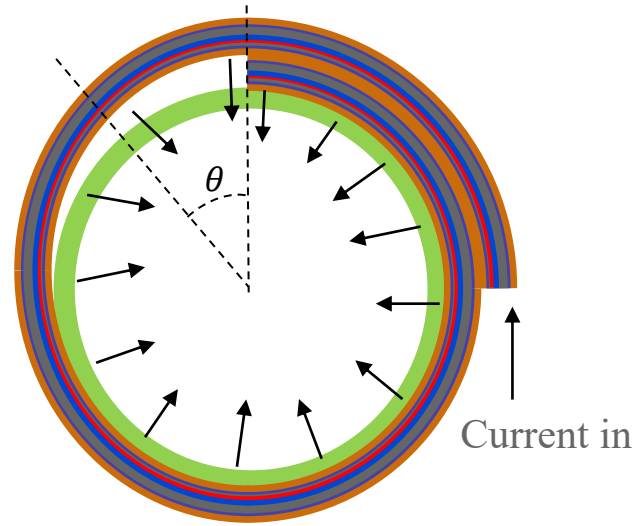
Scheme of tapes stack cross section



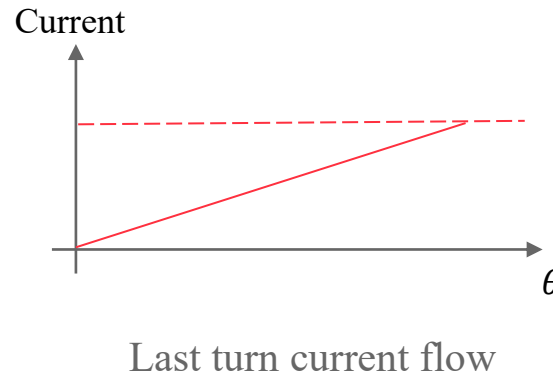
- Last turns with hastelloy/copper tape (without HTS)
  - Allow machining
    - For a deviation of 10  $\mu\text{m}$  per tape  $\rightarrow$  1 mm per 100 turn
  - Electrical connection
  - Resistance  $\sim$  0.2  $\mu\Omega$  per turn
- End of the winding with bare hastelloy tape
  - Removes the drop of solder
  - See the two last pancakes

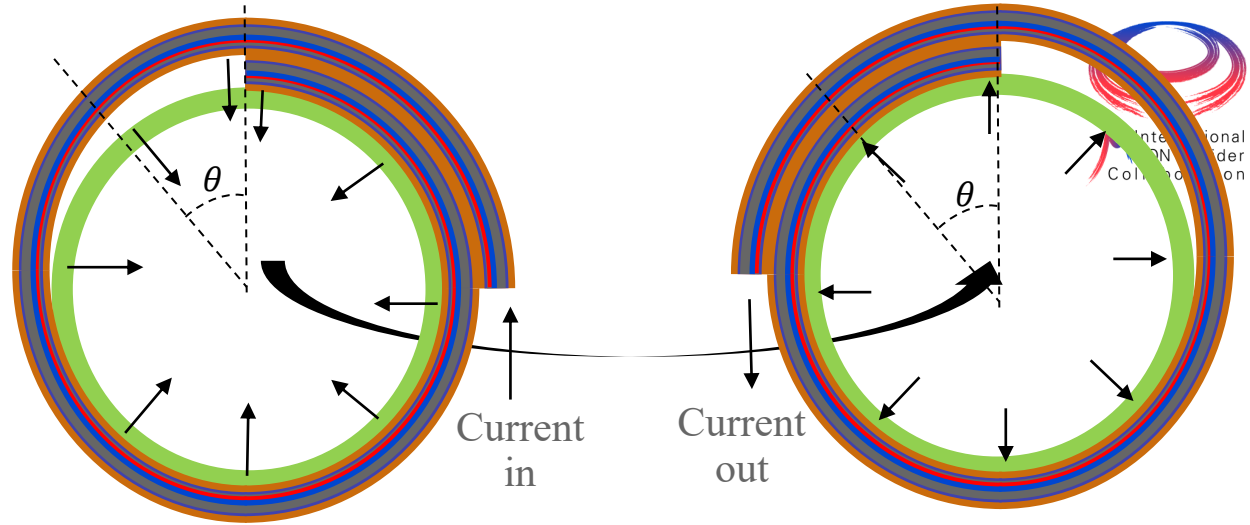




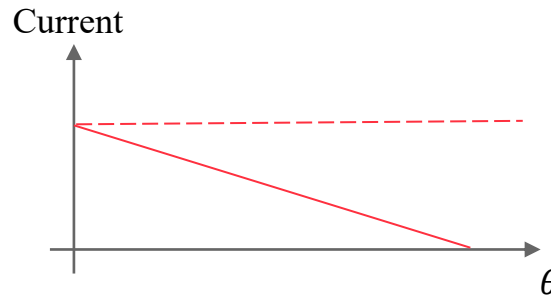


- Current flow *quasi* homogeneous in inner part
- Current flow linearly

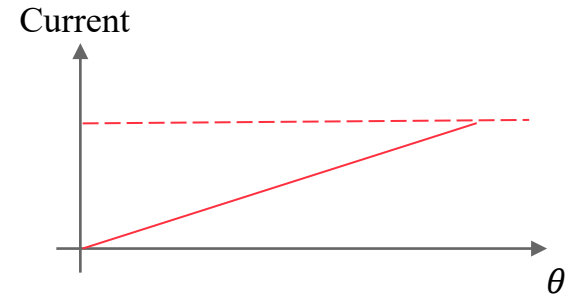




- Current flow *quasi* homogeneous in inner part
- Current flow linearly



Last turn current flow



Last turn current flow



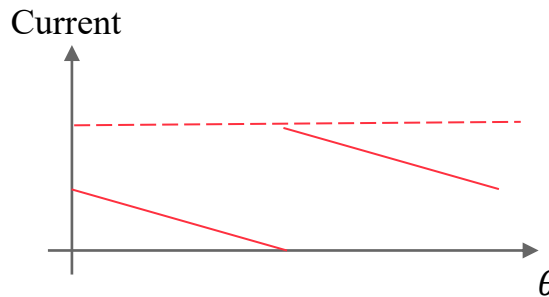
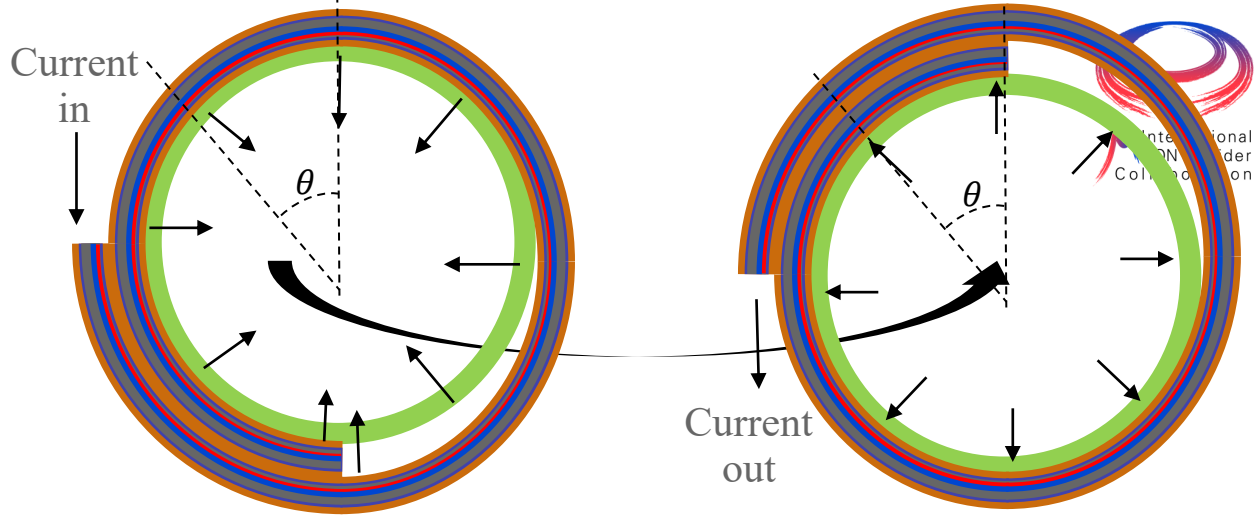
- Issue for field homogeneity ?

Equivalent current in double pancake

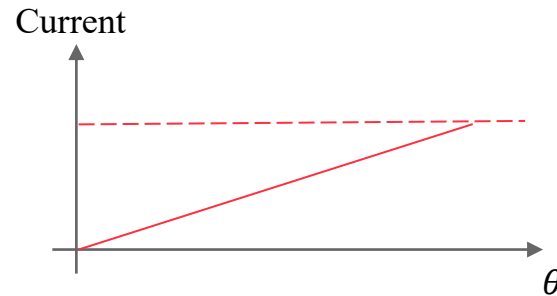
Acceptable tolerance ?



Last turn current flow



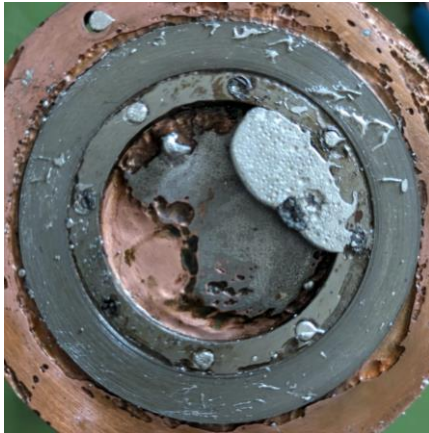
Last turn current flow



Last turn current flow

### Etching

- Parts protected with silicon coating
- Whole pancake drowned into iron chloride
- Cleaned into sodium bicarbonate
- Dried with pressurized air
- Cleaned with acetone
- Cleaned with water
- Dried with pressurized air

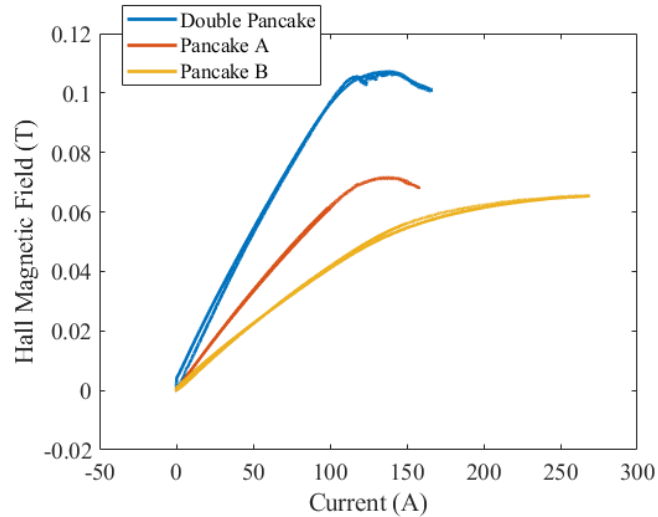
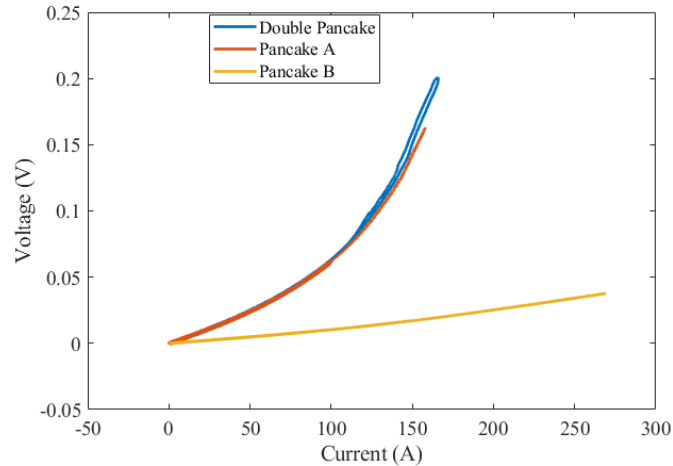


$\tau$ (s)	Pancake 2	
	Charge	Discharge
5 A	4.87	4.92
10 A	4.70	5.05
20 A	4.78	5.02
50 A	4.60	4.83

~ 4.8 s

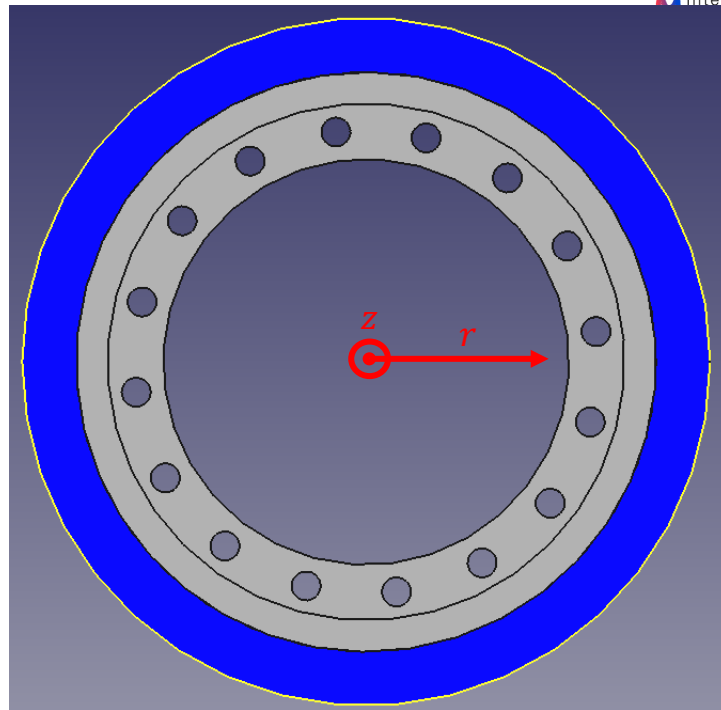
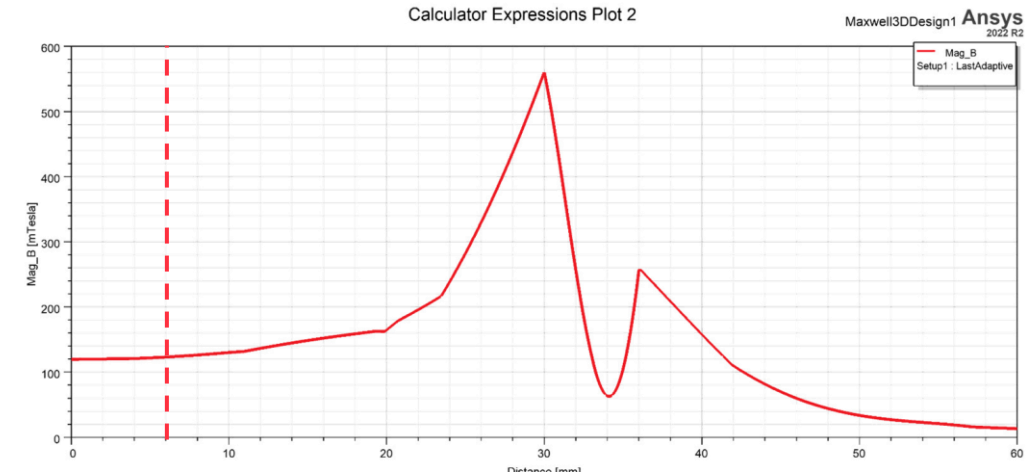
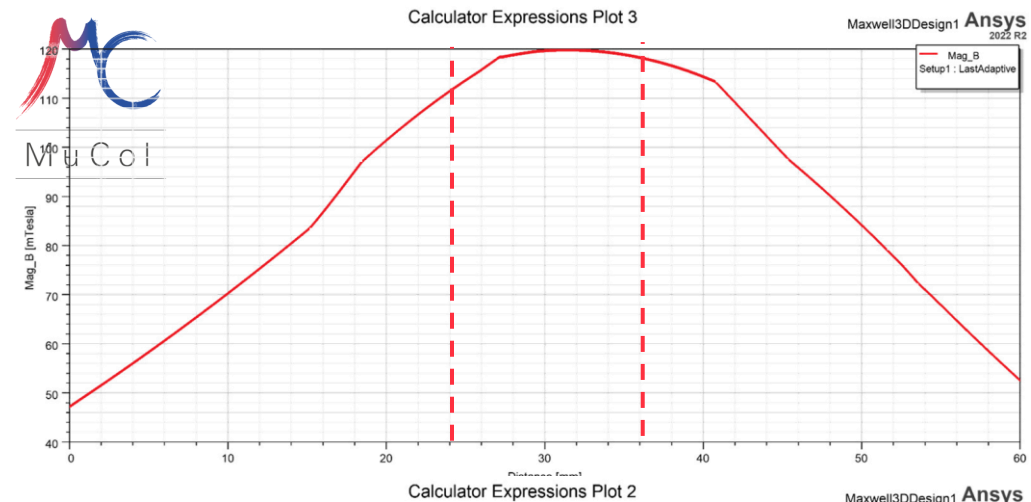
$\tau$ (ms)	Pancake 2 after etching			
	Charge	Discharge	Charge 2	Discharge 2
5 A	41.8	28.2	42.2	29.8
10 A	40.6	51.4		
20 A	30.4	43.1		
30 A	36.4	40.7	34.1	41.1
40 A	50.4	45.4	44.8	41.2
50 A	51.8	50.5		

< 40 ms



	Time Constant $\tau$ (s)
Double Pancake	4.6
Pancake A	1.6
Pancake B	3.1

Where do these differences come from ?



**Variation ~10% of central field  
within  $\pm 5$  mm from center**

