

## Assembly and quality control tests of the 3D sensor modules for the innermost layer of the ATLAS ITk pixel detector

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The High Luminosity upgrade of the Large Hadron Collider (HL-LHC) will demand the ATLAS detector to face an increased instantaneous luminosity up to  $7.5 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$  and an average of 200 proton-proton collisions per bunch-crossing. To cope with this challenge, the present ATLAS Inner Detector will be completely replaced with a new silicon-based Inner Tracker (ITk), made of a Pixel detector at a small radius and a large area Strip detector surrounding it. Specifically, the new Pixel tracker is based on hybrid detectors, in which the pixelated sensors are interconnected via bump-bonding to their dedicated readout ASICs. Whereas the same readout chip (ITkPix) –produced on a 65 nm CMOS technology –is used all along the pixel detector, two different technologies have been chosen for the pixel sensors: planar, for the outer layers, and 3D, for the innermost layer (L0). 3D sensors have been selected by their inherent radiation hardness, since the innermost layer will reach a fluence up to  $2 \times 10^{16} \text{ n}_{eq} \text{ cm}^{-2}$  (with a 1.5 safety factor), which is not suitable for planar sensor operation.

The basic unit of the pixel detector is the pixel Module. For the L0 layer, the pixel Module is known as “triplet”, as it consists of an ensemble of three 3D pixel sensors individually hybridized to their respective readout chips (the so-called “bare modules”) and mounted on a single flexible PCB, which allows for biasing and communication. To reduce the material budget, the modules are powered in serial power chains. There are three different designs for the triplet modules, according to their geometry: linear (with 3 bare modules in a row), which will populate the barrel section of L0; and two ring geometries (R0 and R0.5), in which the bare modules are disposed in a circle sector arrange, and will populate the coupled-ring and the intermediate-ring sections of the L0 end-cap, respectively. Seven European research institutes take care of the assembly and full quality control test of the triplets, with every institution specialized on a different geometry or specific stages of the production chain. The modules are then shipped to SLAC (US) to be loaded on the inner system local supports and interconnected in the serial power chains.

This talk aims at presenting an overview of the status of the ITk triplet modules, which are now entering in their production phase. Details of the assembly and testing procedures of the first triplet prototypes will be included, with a special focus on the specific tests carried out to assess the quality of the bump connectivity, the integrity of crucial sub-systems of the readout chip, and the stability of the sensor performance along the process. Some update of the serial power interconnection and loading on their final supports will be also included.

**Authors:** KAKOTY, Niraj (The Barcelona Institute of Science and Technology (BIST) (ES)); GEMME, Claudia (Universita degli Studi di Genova Dipart. di Fisica); FERNANDEZ-MARTINEZ, Pablo (IMB-CNM, CSIC)

**Presenter:** KAKOTY, Niraj (The Barcelona Institute of Science and Technology (BIST) (ES))

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