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Development and Wafer-level Characterization of the First Production of DC-RSD Sensors at FBK

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DC-RSDs are silicon sensors that aim to provide a time resolution for minimum ionizing particles in the order of 30 ps and a spatial resolution of a few percent of the channel pitch. These performances are enabled by internal charge multiplication and resistive charge division between the channels. The time resolution is expected to be the same as Low Gain Avalanche Diodes (LGADs). The performance of the resistive charge division mechanism was demonstrated in AC-LGADs or Resistive Silicon Detectors (RSD) where a capacitive coupling between readout electrodes and resistive layer was employed. DC-RSDs use a direct coupling between the electrodes and the resistive layer avoiding the bipolar signal of the AC-coupled designs and providing a better bias distribution to the resistive layer. The channel segmentation does not rely on interrupting the gain layer, aiming to maintain a fill factor close to 100%. The first DC-RSD sensor batch was fabricated at FBK with the aim to demonstrate the soundness of the sensor concept. This batch contains design variations of the sensors, trench isolation between channels to provide signal confinement on the resistive layer, and an improvement in the contact resistance between readout electrodes and resistive layer. This talk summarizes the characterization of the sensors performed at wafer level. Results on contact resistance, gain, breakdown voltage, and sheet resistance of the resistive layer will be shown.

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