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Results from a 2nd production run of low temperature wafer-wafer bonded pad-diodes for particle detection

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We are investigating the use of low temperature wafer-wafer bonding in the fabrication of next-generation particle pixel detectors. This bonding technique could enable the integration of fully processed CMOS readout wafers with high-Z absorber materials, facilitating the creation of highly efficient X-ray imaging detectors. It might also facilitate the integration of structures embedded inside the wafer bulk, such as deep uniform gain layers.

The bonding process results in a thin (nm-scale) amorphous layer at the bonding interface. To study the impact of this interface on detector operation, we fabricated simple wafer-wafer bonded pad diodes using high resistivity float-zone silicon wafers. Results from a first fabrication run of such diodes revealed that the presence of the bonding interface alters the depletion behaviour, with the interface acting as a heavily doped N++ layer. However, metal contamination of the bonding surfaces during fabrication compromised these results, making them unrepresentative of an ideal bonding interface.

In this talk, we present the results from a subsequent fabrication run, which does not exhibit this sort of metal contamination. These results confirm that the bonding interface behaves as a heavily doped N++ layer, even without contamination. Finally, we will discuss the reverse leakage current of the bonded samples.

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