Technology and layout developments for the vertex detector in France

Serhiy Senyukov (IPHC Strasbourg)

Monolithic Active Pixel Sensors (MAPS) are the ideal candidate

Fabrizio Palla, Venice, 4 November 2024
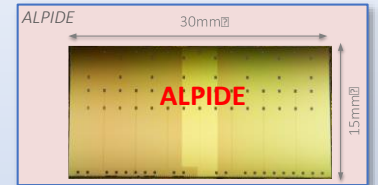
Experience with MAPS vertex detectors in France

- ## STAR-PXL @ RHIC
  - ULTIMATE chip design (IPHC)
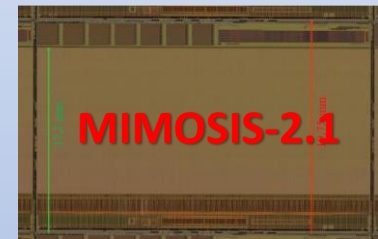   - First MAPS for vertex detector

ULTIMATE

- ## ALICE-ITS2 @ LHC
  - ALPIDE chip design (IPHC, IRFU, IP2I)
    - First in TJ 180 nm
    - First MAPS tracker chip
  - Detector assembly (IPHC)
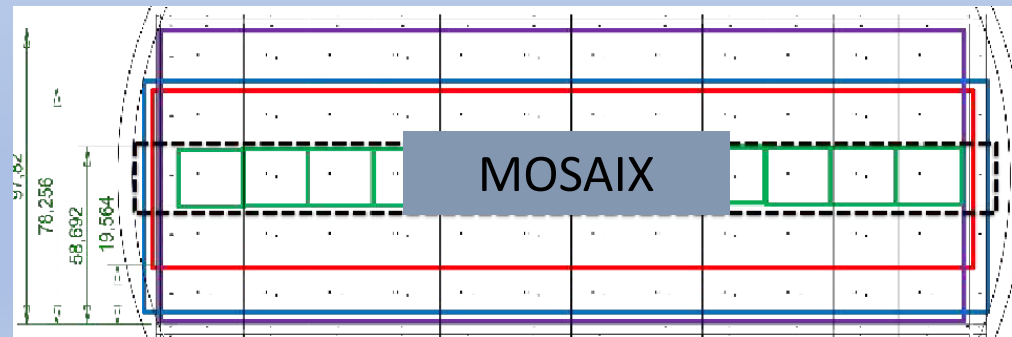

ALPIDE — 30mm — 15mm

- ## CBM-MVD @ FAIR
  - MIMOSIS chip design (IPHC)
    - TJ180 nm
    - Hit rate: 70 MHz/cm^2 (ALIPDE x2)

- ## Belle II VXD @ KEK
  - OBELIX chip design (IPHC, CPMM)
    - TJ 180 nm
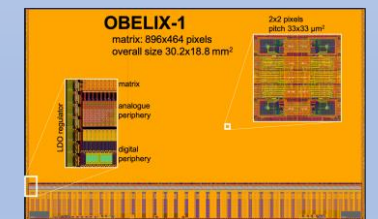   - Time resolution: 100 ns
    - Hit rate: 120 MHz/cm^2 (triggered)

- ## ALICE-ITS3 @ LHC
  - MOSAIX chip design (IPHC)
    - First in TPSCo 65 nm process
    - First large area stitched sensor ~260 cm^2

MIMOSIS-2.1

MOSAIX

OBELIX-1
matrix: 896x464 pixels
overall size 30.2x18.8 mm^2
2x2 pixels pitch 33x33 μm^2

New project – OCTOPUS* (DRD3/7)

Optimized **C**MOS **T**echnology f**O**r **P**recision in **U**ltra-thin **S**ilicon

- Simulation, development and characterization of MAPS in TPSCo 65 nm CMOS Imaging Process targeting future Lepton Collider specifications :
  - Single point resolution: 3 µm
  - Time resolution: 5 ns
  - Power dissipation: 50 mW/cm^2
  - Thickness: 50 µm
  - Readout architecture scalable to large area
- Intermediate step – high resolution sensor for beam telescope
  - Time resolution: 100 ns
  - Power dissipation: <500 mW/cm^2
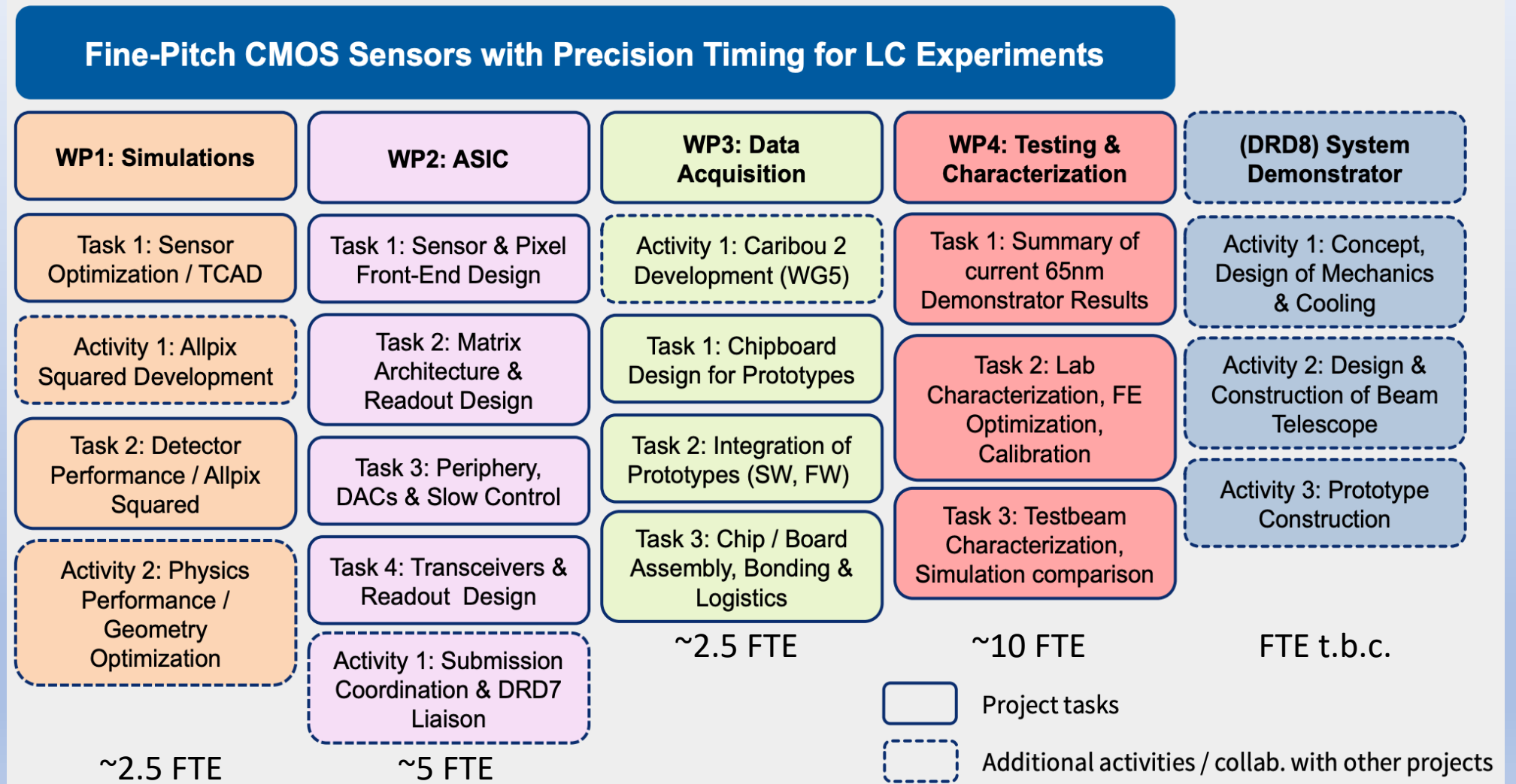
* Perhaps not the final name. Voting in progress

OCTOPUS: Milestones and deliverables

Number	Deliverable/Milestone Title	WP project #	Lead	Type	Dissemination Level	Due Date
M1	Report on Demonstrators	4	DESY	Report	DRD3 report	Month 9 (Q1 2025)
D1 **MPR2**	Beam Telescope Demonstrator Matrix Submission **3 μm**	1, 2	IPHC	Prototype **Full column height**	Manual / Presentation	Month 24 (Q2 2026)
M2	Report on Demonstrator Matrix Characterization	3, 4	DESY	Report	Publication	Month 36 (Q2 2027)
D2 **MPR3**	Full Beam Telescope Sensor Submission	2, 3	IPHC	Prototype	Manual / Presentation **≥ 2cm² sensor**	Month 48 (Q2 2028)
M3	Report on Beam Telescope Sensor Performance	3, 4	DESY	Report	Publication	Month 60 (Q2 2029)
D3 **ER**	LC Vertex Sensor Demonstrator Submission	1, 2	IPHC	Prototype	Manual / Presentation	Month 66 (Q4 2029)
M4	Report on LC Vertex Sensor Demonstrator Performance	3, 4	DESY	Report	Publication	Month 78 (Q4 2030)

OCTOPUS: project structure

Fine-Pitch CMOS Sensors with Precision Timing for LC Experiments

WP1: Simulations	WP2: ASIC	WP3: Data Acquisition	WP4: Testing & Characterization	(DRD8) System Demonstrator
Task 1: Sensor Optimization / TCAD	Task 1: Sensor & Pixel Front-End Design	Activity 1: Caribou 2 Development (WG5)	Task 1: Summary of current 65nm Demonstrator Results	Activity 1: Concept, Design of Mechanics & Cooling
Activity 1: Allpix Squared Development	Task 2: Matrix Architecture & Readout Design	Task 1: Chipboard Design for Prototypes	Task 2: Lab Characterization, FE Optimization, Calibration	Activity 2: Design & Construction of Beam Telescope
Task 2: Detector Performance / Allpix Squared	Task 3: Periphery, DACs & Slow Control	Task 2: Integration of Prototypes (SW, FW)		Activity 3: Prototype Construction
Activity 2: Physics Performance / Geometry Optimization	Task 4: Transceivers & Readout Design	Task 3: Chip / Board Assembly, Bonding & Logistics	Task 3: Testbeam Characterization, Simulation comparison	
	Activity 1: Submission Coordination & DRD7 Liaison	~2.5 FTE	~10 FTE	FTE t.b.c.
~2.5 FTE	~5 FTE			

Project tasks

Additional activities / collab. with other projects

OCTOPUS: participating institutes

Institute	Contact	Main areas of contribution
APC Paris	M. Bomben	Simulations, testing
Bonn University	J. Dingfelder	ASIC design, testing
CERN	D. Dannheim	Testing, DAQ, ASIC design support (through DRD7)
DESY	S. Spannagel	ASIC design, testing, DAQ, simulations
ETH Zurich	M. Backhaus	ASIC design, testing
FNSPE Prague	P. Svihra	ASIC design, DAQ, testing
GSI Darmstadt	M. Deveaux	Simulations, testing
HEPHY Vienna	T. Bergauer	DAQ, testing, ASIC design
IPHC Strasbourg	A. Besson	ASIC design, testing
Oxford University	D. Bortoletto	Powering, integration, testing
Zurich University	A. Macchiolo	Testing, DAQ, simulations

Newcomers are welcome!

Some contributions to OCTOPUS project

1. Performance studies of TPSCo 65 nm CMOS process

2. Simulation studies of in-pixel signal digitization

3. Asynchronous (clockless) matrix readout

1. Performance studies of TPSCo 65 nm CIS

CE65V2 – 48 × 24 pixel chip with analogue readout

- 3 process variants (STD, MOD, GAP) for depletion control

- 3 pixel pitches: 15, 18, 22.5 µm

- 2 pixel arrangements: SQ and HSQ

- AC pixels with V_{bias}= (0; 10) V

- Rolling shutter readout at 10 MHz

Lab and beam tests since
Aug 2023 by the international team:

APC Paris, CTU Prague, Hiroshima University, Tsukuba University, UZH, and IPHC

From "APTS paper" https://inspirehep.net/literature/2768850
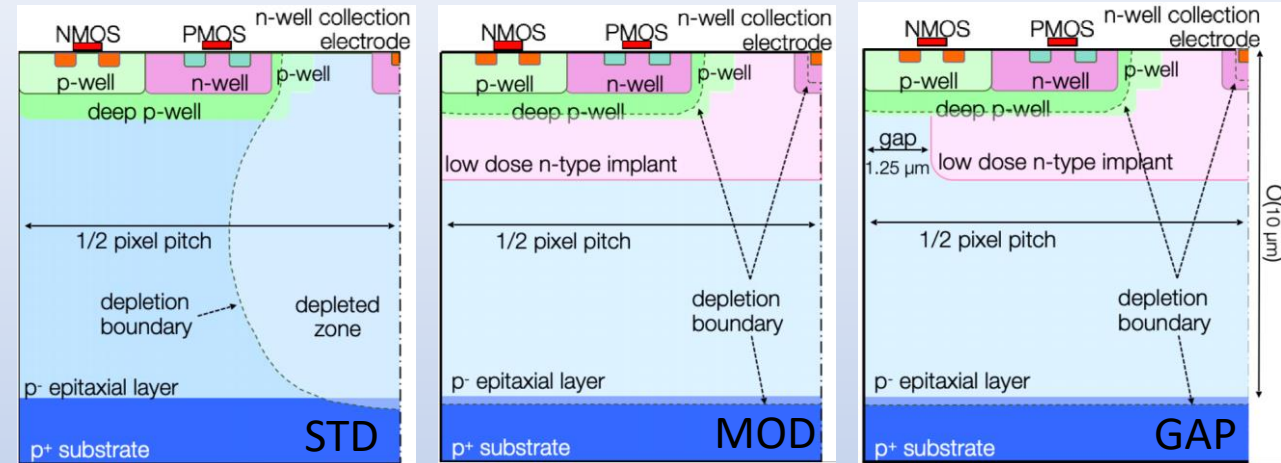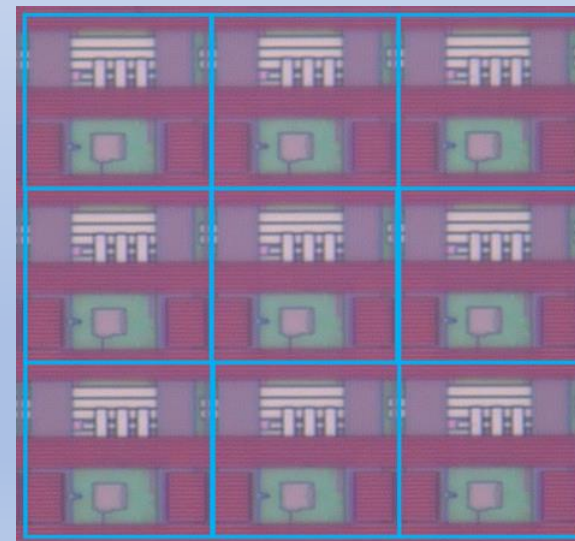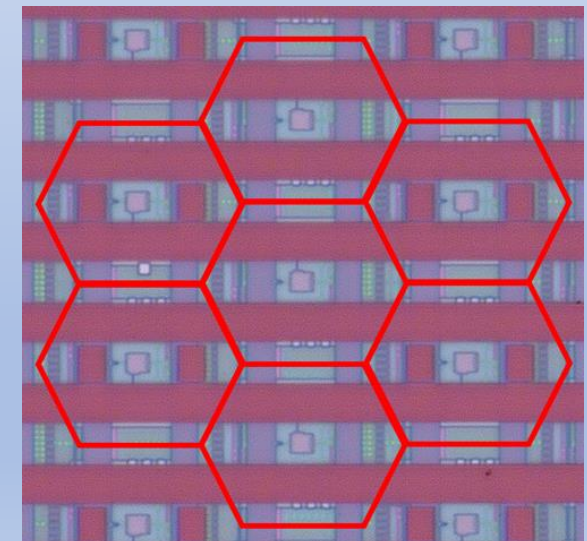
SQ pixels

HSQ pixels

2 μm resolution with 22.5 μm pitch*

GAP

STD
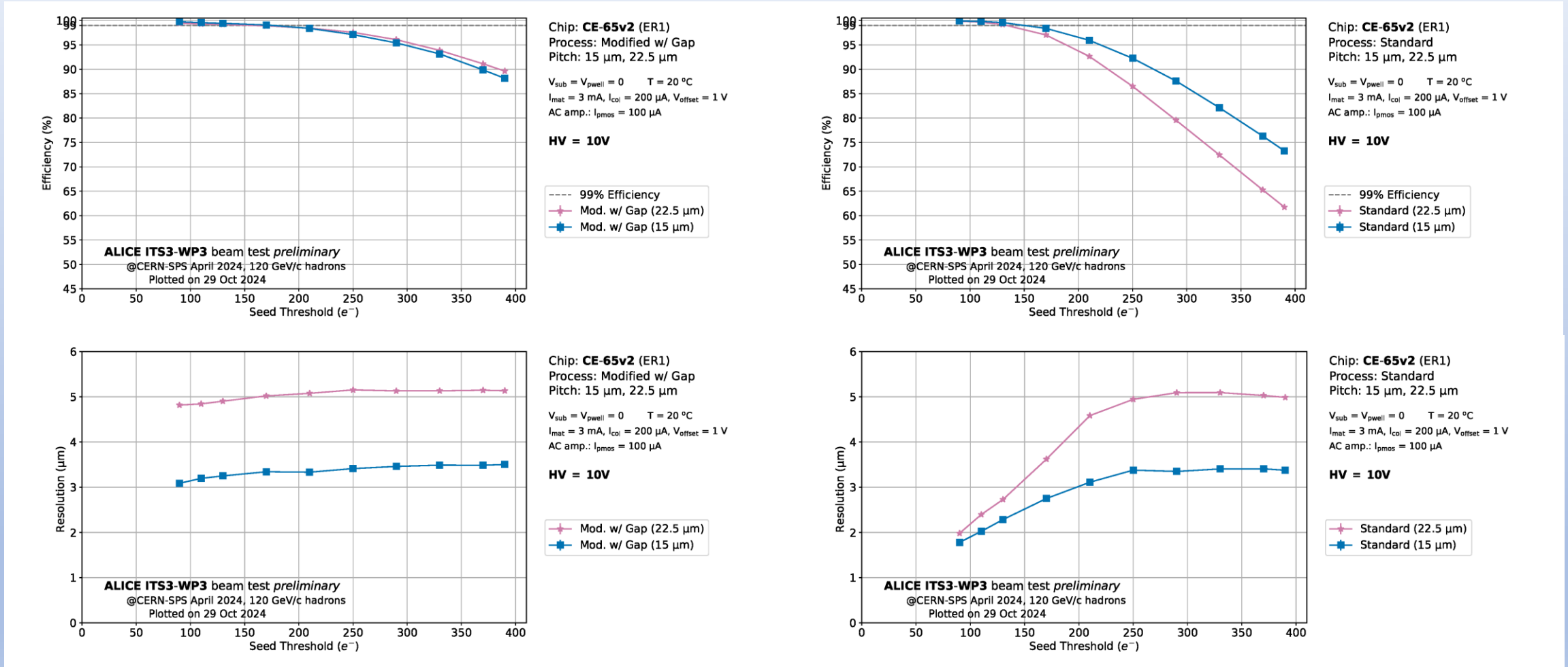
* With 16-bit analogue readout

2. Simulation studies of in-pixel digitization
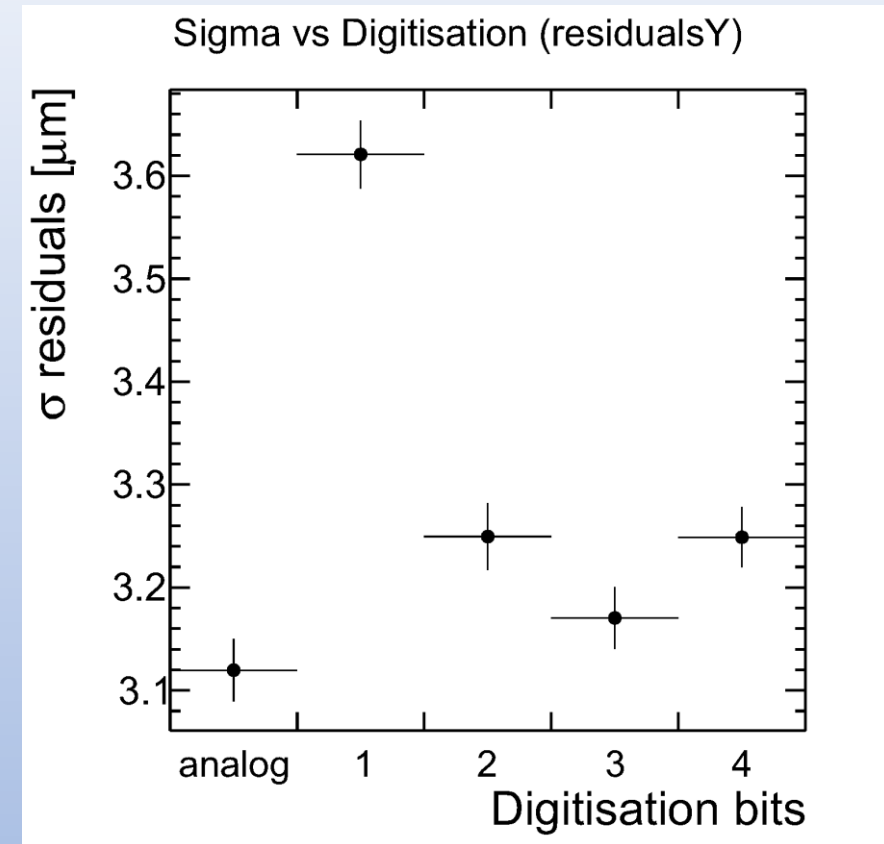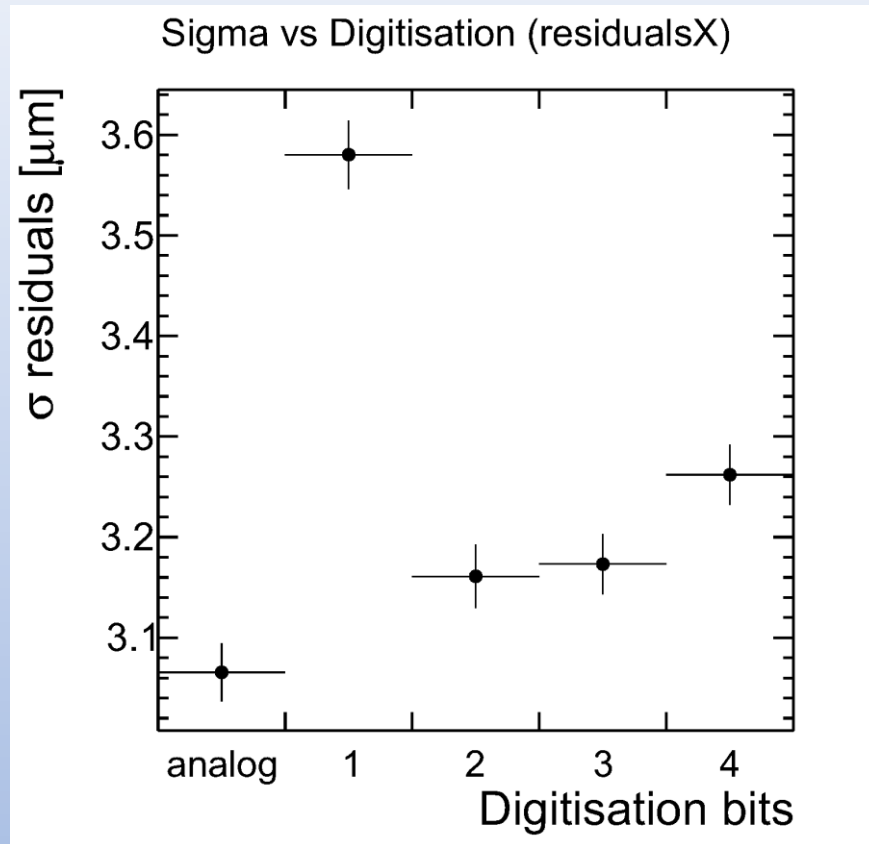
- Test beam data of CE65V2 was digitized offline using ADC of various precision (1-4 bits)
- Low bit number ADC can recover significant part of the resolution
- Study in progress by Gaelle Sadowski (IPHC Strasbourg)

3. Asynchronous (clockless) matrix readout

- Based on Fixed Priority Arbiter (link)
  FPA asynchronously translates signals from N inputs to 1 output based on priorities fixed in hardware

- Proposal to use a tree of FPAs to propagate each pixel of double column to periphery (link)

- Many possible tree structures in-between:
  - Many 2:1 FPAs (Better bandwidth)
  - One N:1 FPA (Less area)

- Simulations shows:
  - Mean pixel readout time 20 ns at 100 MHz/cm^2
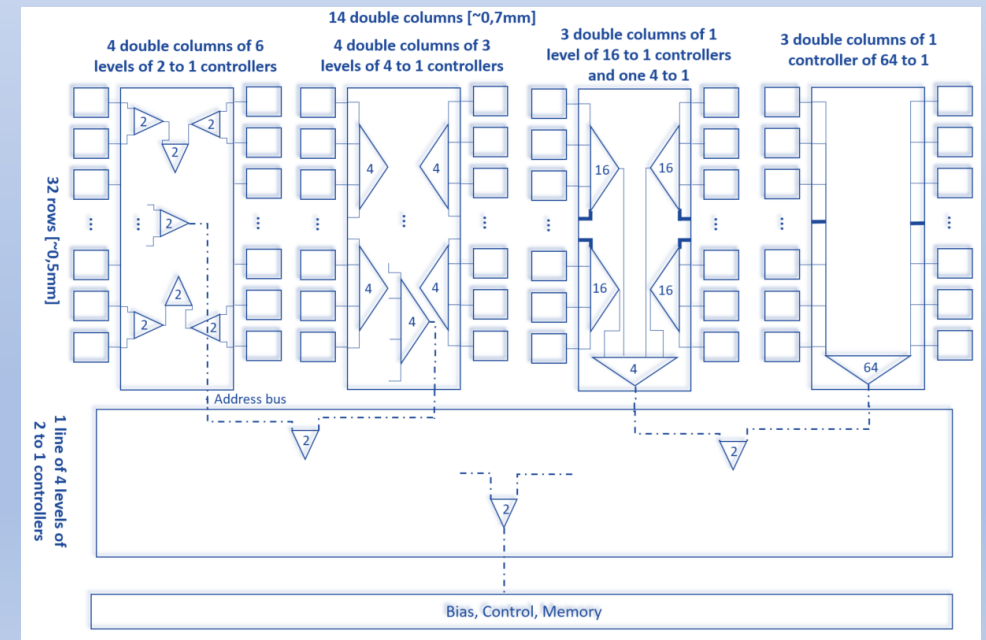 - Power consumption 10 mW/cm^2 (digital)
  - Time resolution 2 ns
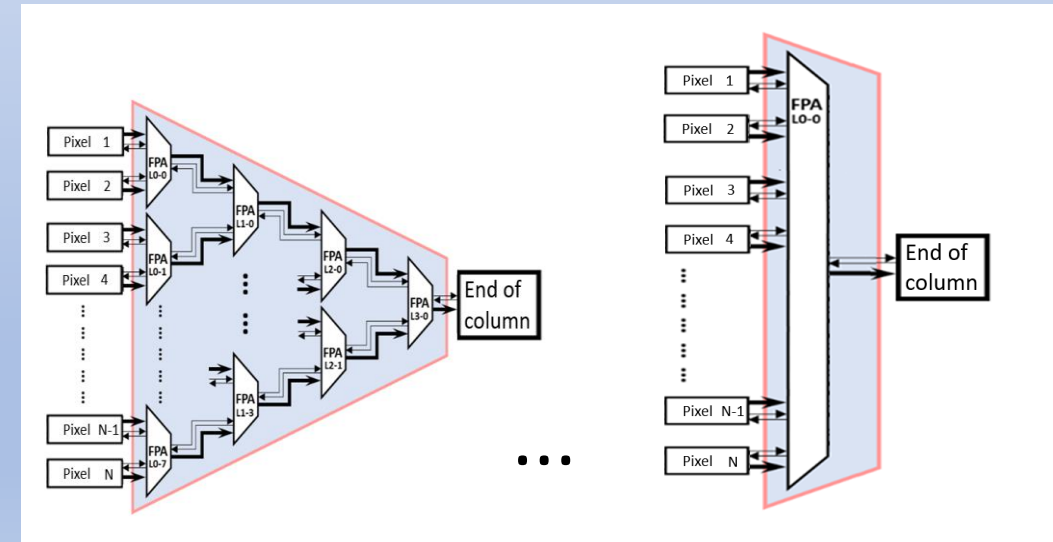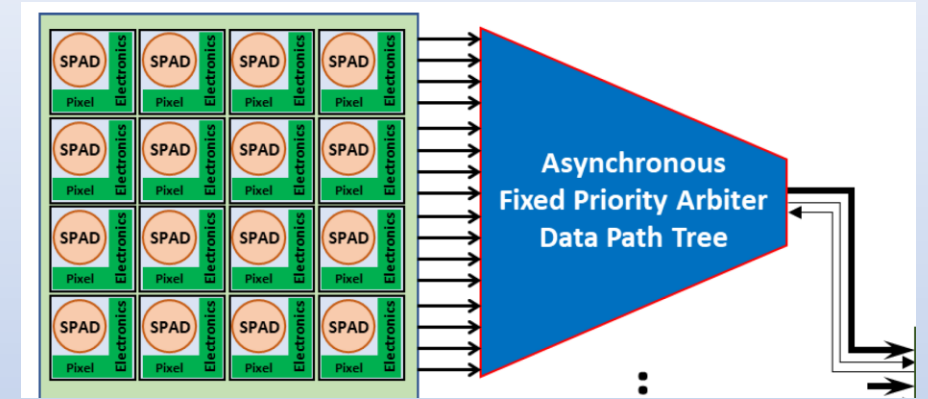
SPARC: first prototype of asynchronous readout

- Pixel matrix: 32 × 28
- Pixel pitch: 24 × 16 μm^2
- Pixel front-end: DPTS-like (CERN)
- FPA tree types: 2:1, 4:1, 16:1, 64:1
- Power dissipation: 5 mW/cm^2
- Mean readout time: 6.3 ns
- Designed by: IPHC, IRFU
- Submission: early 2025 (ER2)
- Test system in preparation
 for summer 2025
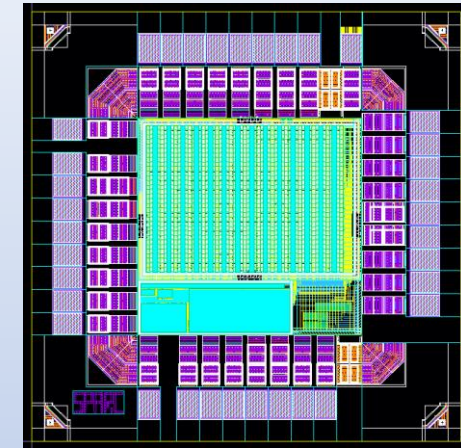
1.5×1.5 mm^2

Possible OCTOPUS architectures

- Option 1: Mid-size pixels
  - Standard process for charge sharing
  - ≥ 20 µm pitch
  - In-pixel digitization (2 Thresholds, 2-3 bits ADC, ToT)
  - Asynchronous readout of 1024-2048 pixels per double column
- Option 2: Small grouped pixels
  - Standard or modified process
  - ≤15 µm pitch
  - Binary output of each pixel
  - Asynchronous readout of 2×2 pixel groups
    - Readout sends 4-bit local address of fired pixels in the group
    - Reduced FPA tree size

OCTPUS schedule
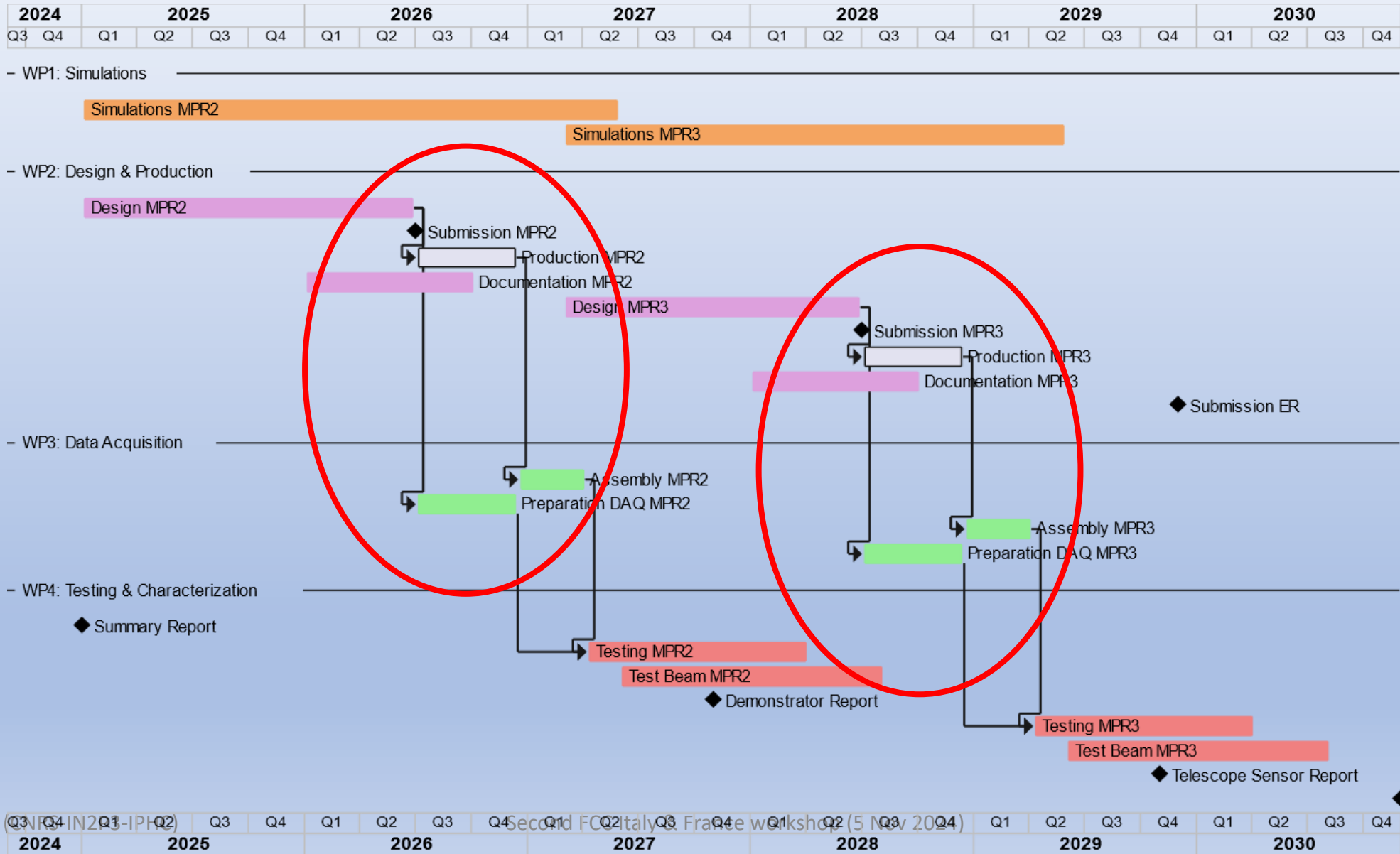
FCC-SEED: FCC Snail-shape vErtEx Detector (DRD8)

- Full silicon ladders of 6/8 reticles
  - With or without stitching along Z

- Ladders are bent:
  - Provide mechanical stiffness to build the layer
  - Reduce the material budget

- Advantages:
  - Full r-phi coverage
  - Stitching yield less critical
  - Less constrain on the layer radius

- Expression of interest in preparation:
  - IP2I Lyon
  - CPPM Marseille
  - IPHC Strasbourg

Beam pipe inner radius ~10 mm
Beam pipe thickness ~ 1.7 mm
Perimeter ~73.5 mm
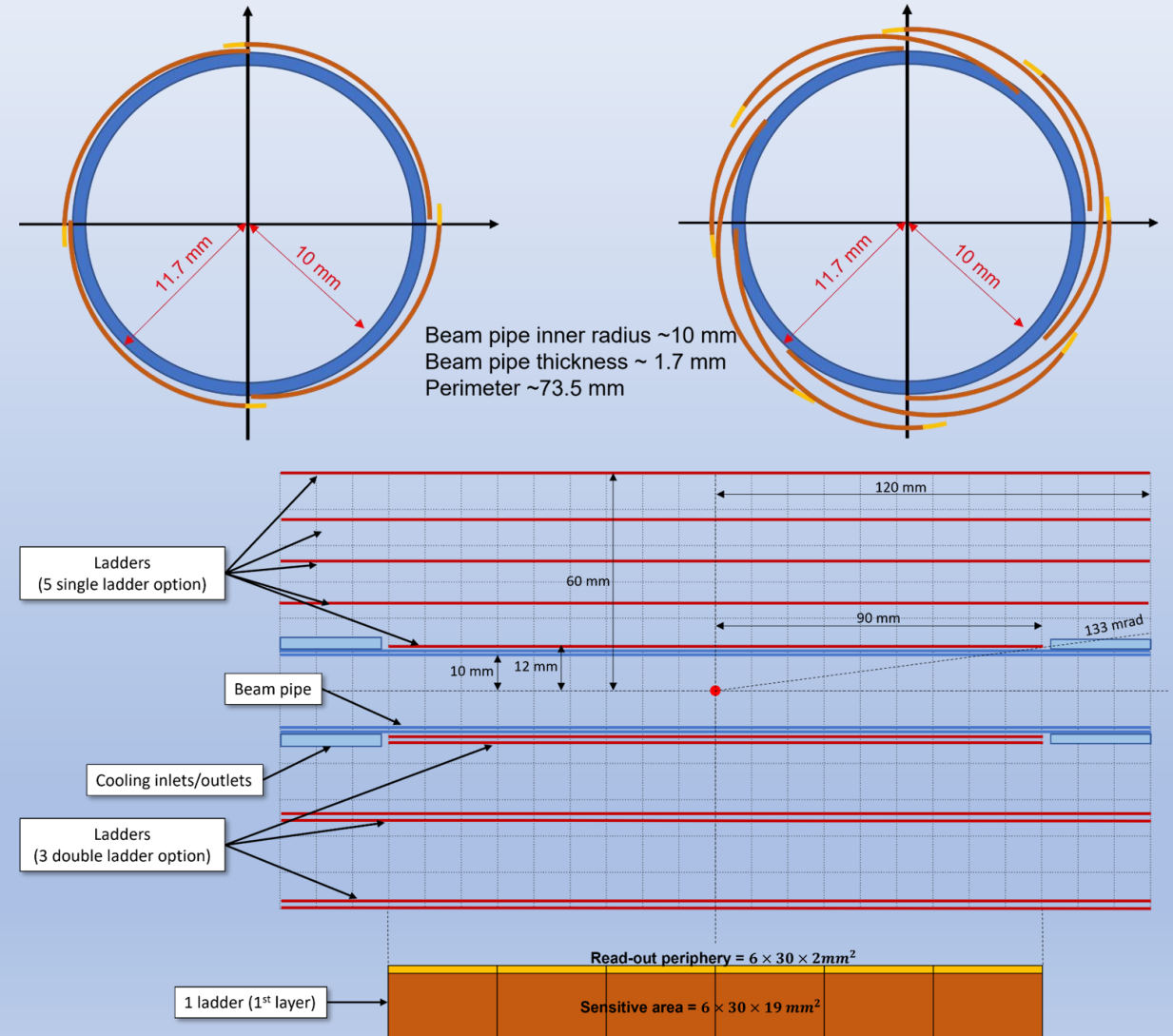
Silicon chip bending studies in IPHC

Project to build a prototype of a FCC-SEED layer using MIMOSIS chips:

Step 1: bending of single MIMOSIS chips

Different thicknesses: 30, 40, 50 µm

Different radii: 18, 15, 12, 10 mm

Step 2: bending of a strip of chips (Super-MIMOSIS)

Step 3: building of full layer demonstrator

Bending test of ALPIDE wafer in IPHC

Summary and outlook

Large experience with MAPS

- Complete set of expertise: simulation, chip design and mechanics
- 3 ongoing projects: MIMOSIS, OBELIX and MOSAIX

Started FCC oriented sensor project OCTOPUS with DRD3/7

Several innovative ideas to reach target specifications:

- Use of 65 nm CMOS process
- In-pixel digitization
- Asynchronous readout

Vertex detector project FCC-SEED in preparation for DRD8

- Silicon bending tests starting in IPHC

Thank you for your attention