

Discussion on Tracking Technology

2nd FCC Italy & France Workshop

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UNIVERSITÀ DEGLI STUDI DI MILANO
DIPARTIMENTO DI FISICA

DETECTOR LAYOUTS



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- A clear area for common work is simulation of detector performance
 - generic detector geometries
 - radial (barrel) and z (endcap) location
 - curved or stave-base geometry for inner vertex
 - number of layers
 - ...
 - parametric detector parameters
 - pitch size
 - depletion depth
 - dE/dx performance
 - timing resolution
 - ...
- But also open mechanical issues

Need also background simulation

"generic" digitizer?

- Minimal radius of the vertex detector
 - hit rate background dominated
 - define bandwidth/power consumption
 - may triggering on the Z or on-detector clusterization reduce service requirements?
- Intermediate silicon layers
 - low p_T particle acceptance and identification
 - forward tracking performance
- Inner radius of the drift chamber
 - performance background-dominated?
 - acceptance for particle ID

- Si-wrapper layout
 - mechanical structure
 - cooling distribution
 - how it is supported to guarantee alignment stability
- Module size
 - CMOS reticle size $\sim 2 \times 3$ cm²
 - Better module modularity: assume $n \times m$ cells (?) optimize per region and radial position (especially in the endcaps)
 - stitching and overlaps
- Particle ID
 - Acceptance of drift chamber for particle ID
 - Can the loss of hits in the forward regions be compensated by silicon measurements:
 - dE/dx by pulse height measurement in silicon layers
 - timing is fashionable, but is it really needed and where?

- Others?

TECHNOLOGY DEVELOPMENTS



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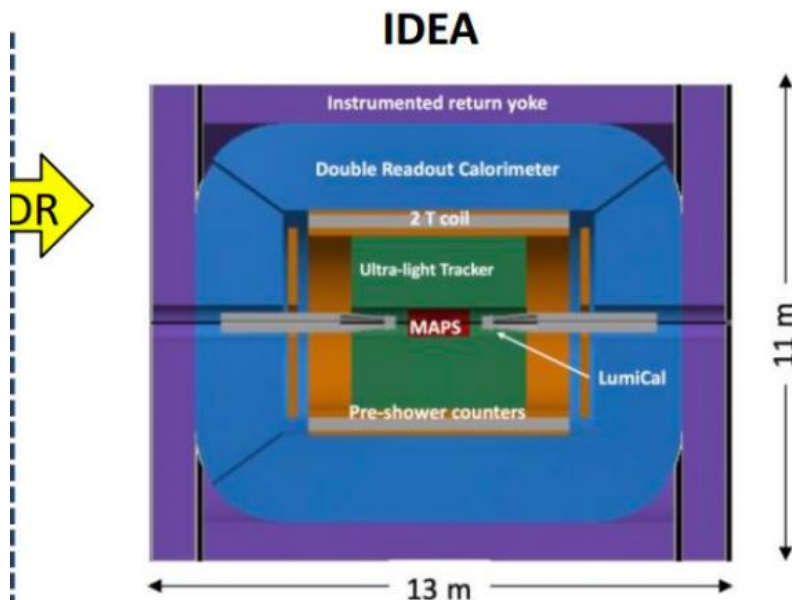
- Depleted MAPS
 - Two technologies presented today
 - TPSCo 65 nm
 - ARCADIA LFoundry 100 nm
 - **Platforms available through DRD7.6**
 - Others are on the market (HVCMOS 180 nm and 55 nm...)
 - Is it important to keep more options open?
compromise: **resources** ↔ **opportunities**
- Some technologies will also develop timing capabilities
 - LGAD and RSD will be discussed in the PID session

- TPSCo 65nm
 - strong drive from the ALICE upgrades
 - communities both in Italy and France
 - can be the seed for a common FCCee development
 - which detector area to target:
inner vertex, outer vertex, wrapper
- ARCADIA
 - mostly INFN developer team, open to international involvement
 - sensor technology demonstrate and scalable
 - may also target some shorter-term experiments, before FCCee
 - which detector area to target:
inner vertex, outer vertex, wrapper

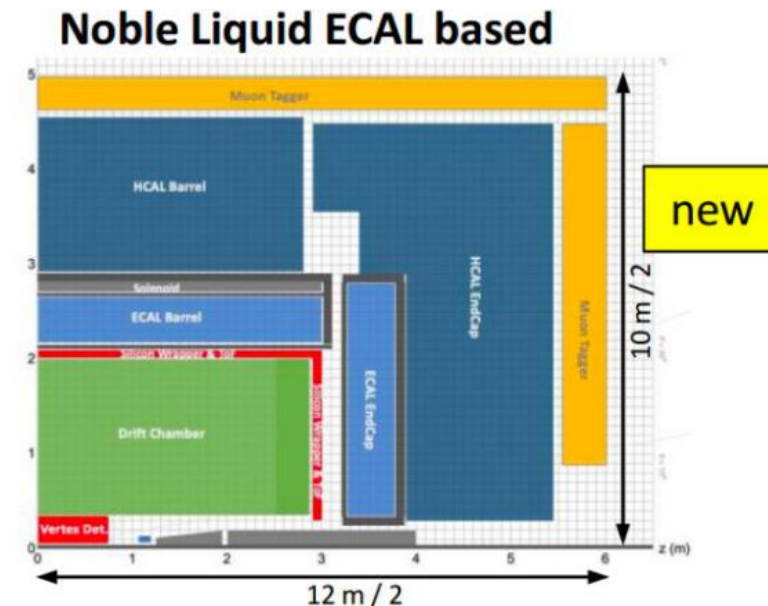
Features	Earlier experiments	FCC inner vertex	FCC outer vertex	FCC wrapper
10 um pitch				
"effective" 10 um pitch with charge sharing				
20 ns time-stamping				
30 ps time resolution				
Serial powering capability				
Chip-to-chip data transmission				
10 mW/cm ² power				
50 mW/cm ² power				
100 mW/cm ² power				
Extreme stitching (20 cm size sensors)				
Moderate stitching (4 cm size sensors)				

Central Gas Tracker

- IDEA and ALLEGRO communities share the Drift Chamber concept
- Which are possible synergies or work sharing?



- A bit less established design
 - But still ~15y history
- Si vtx detector; ultra light drift chamber w powerful PID; compact, light coil;
- Monolithic dual readout calorimeter;
 - Possibly augmented by crystal ECAL
- Muon system
- Very active community
 - Prototype designs, test beam campaigns, ...



- A design in its infancy
- Si vtx det., ultra light drift chamber (or Si)
- High granularity Noble Liquid ECAL as core
 - Pb/W+LAr (or denser W+LKr)
- CALICE-like or TileCal-like HCAL;
- Coil inside same cryostat as LAr, outside ECAL
- Muon system.
- Very active Noble Liquid R&D team
 - Readout electrodes, feed-throughs, electronics, light cryostat, ...
 - Software & performance studies

BACKUP



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