Summary VD and PiD detectors for FCC-ee

based on A. Andrezza, G. Boudoul, T. Papaevangelou,
E. Robuti, M. Rolo, S. Senyukov, D. Contardo/P. Schwemling

D. Contardo (IP2I)

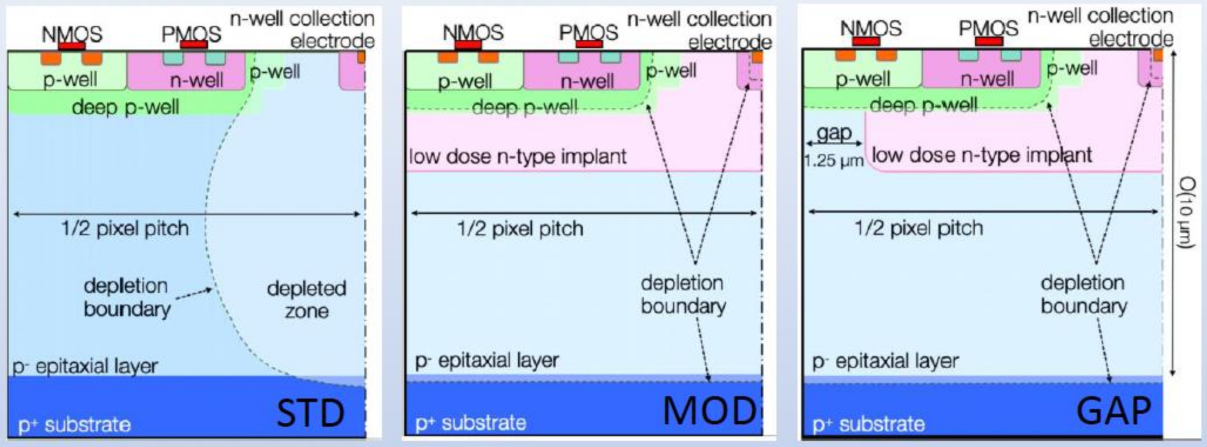
Vertex Detector

target precision ≃ 3 μm and X/X_0 /layer less than 0.1% at low power ≲ 50 mW/cm^2

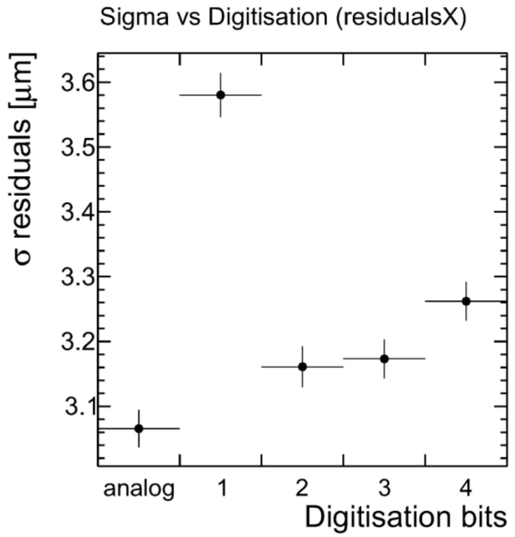
Monolithic CMOS technology is a unique solution to meet this performance

S. Senyukov developments in TPSCo 65 nm processes

- “small electrodes, thin epi-layer (10 μm), large size (ALICE-ITS3)
- “OCTOPUS” DRD3/7 project goal demonstrate best approach/alternatives toward 3 μm
  - process variants : STD ≃ 25 μm pitch, GAP ≲15 μm
  - STD/GAP 100/5 ns timing precision targets
  - Asynchronous readout, digitization few bits for STD higher pitch, pixel grouping for GAP lower pitch



From “APTS paper” https://inspirehep.net/literature/2768850



different processes provide differtent charge sharing, few digitisation bits can improve resolution

+ The project has several international collaborators

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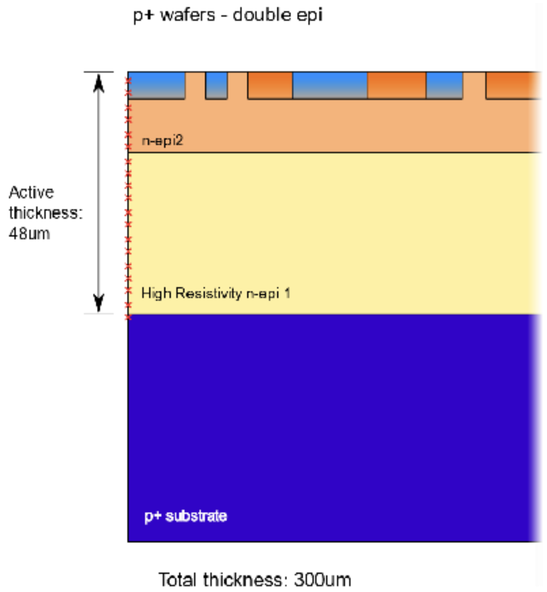
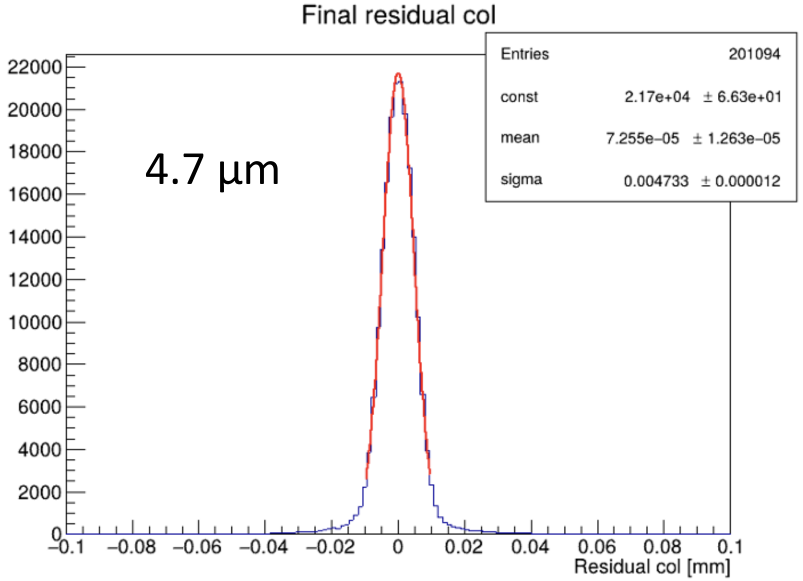
Monolithic CMOS technology is a unique solution to meet this performance

M. Rolo developments in LFoundry 110 nm processes

- large electrodes, HR wafers, active thickness down to 50 μm
- ARCADIA-MD3
  - pixels 25 x 25 μm^2, matrix 512 x 512, 1.28 x 1.28 cm^2 silicon active area, “side-abuttable”
    - < 30 mW/cm^2 at 100 MHz/cm^2
    - 4.7 μm resolution with binary readout (not deconvoluted from telescope resolution)



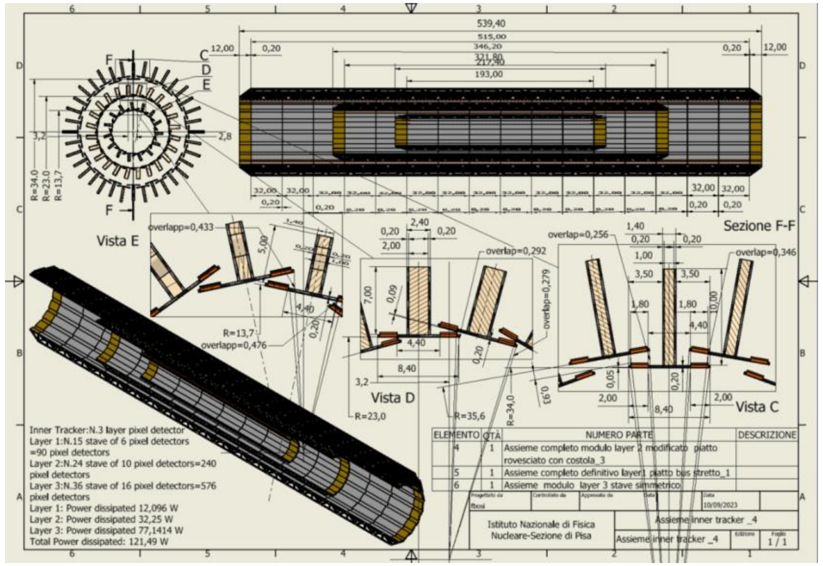


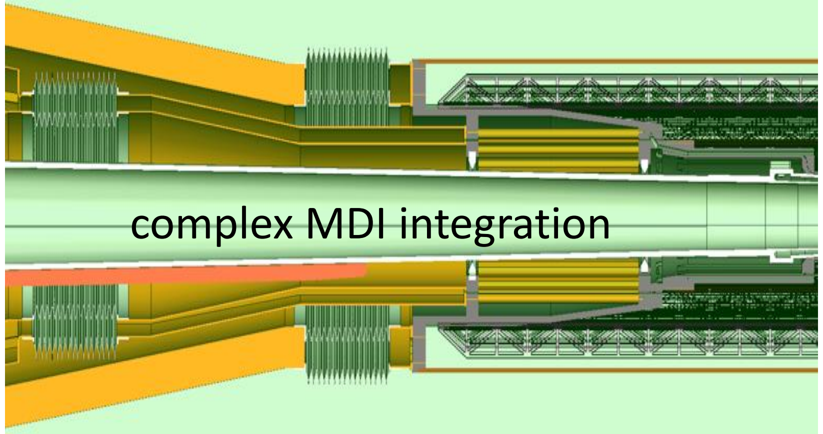
Also studies of 10 μm pitch and grouping in mini-strips

Vertex Detector mechanical designs

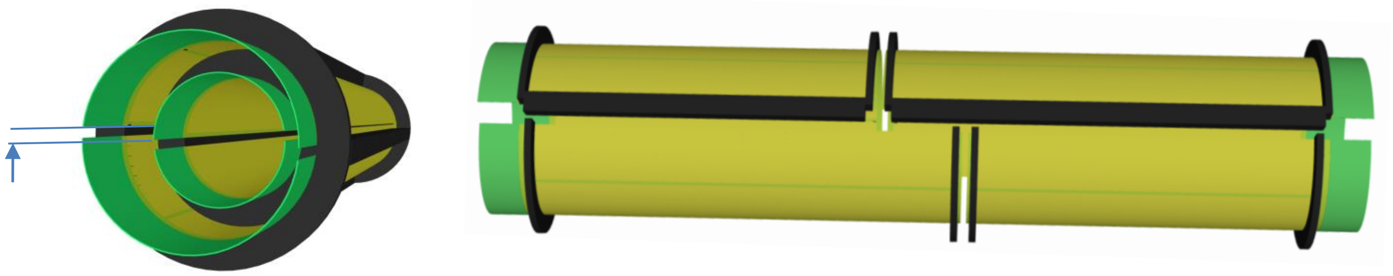
crucial to fully benefit from sensor performance (or to avoid over-designing)

F. Palla stave concept
small sensors, 0.25% X/X_0 /layer

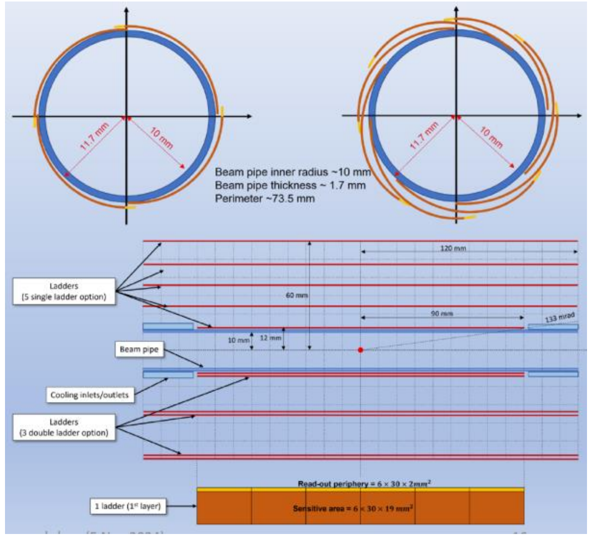




large bent sensors 2 in layer 1-2, 4 in layer 3 and 4
improved X/X_0, but fill factor and hermeticity issue



S. Senyukov SEED large sensors in snail shape allowing overlaps



Several other common challenges

- airflow cooling
- stability
- services
- MDI integration
- accessibility

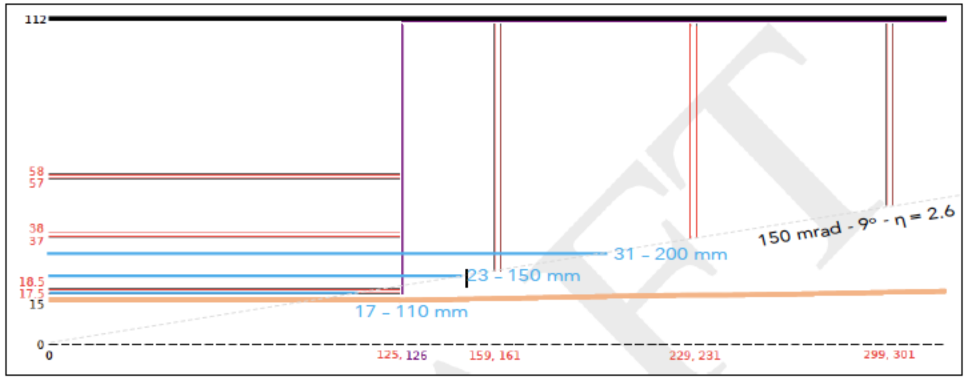
Vertex Detector simulations

G. Boudoul, A. Andreazza

- Provide guidance on overall configuration

  can be parametric
  - radius and lentgth of layers
  - single versus double layers
  - requirements / layer(disk) extended to outer pixel and wrapping layers…

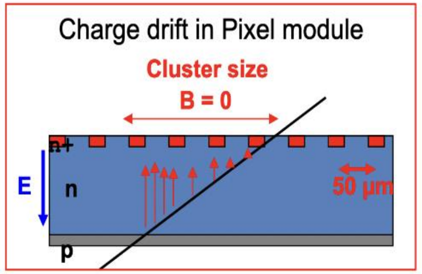
old plot of CLD and IDEA vd on top of each others

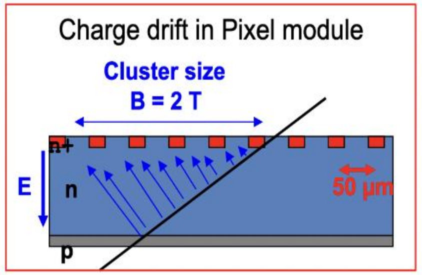


- Provide guidance for sensor and system R&D

  need detailed geometries, full GEANT simulations
  - operation condition, rates and occupancies at different sensor positions including background
    - input to readout architecture
  - realistic performance estimate with respect to
    - sensor parameters, system design (X/X_0, hermeticity, acceptance), mis-calibrations

➢ Essential piece is development of a digitizer (started)
  - produce realistic clusters for all tracks
    - eg correct hit positions and occupancies
  - should be usable in all sensor & detector configurations





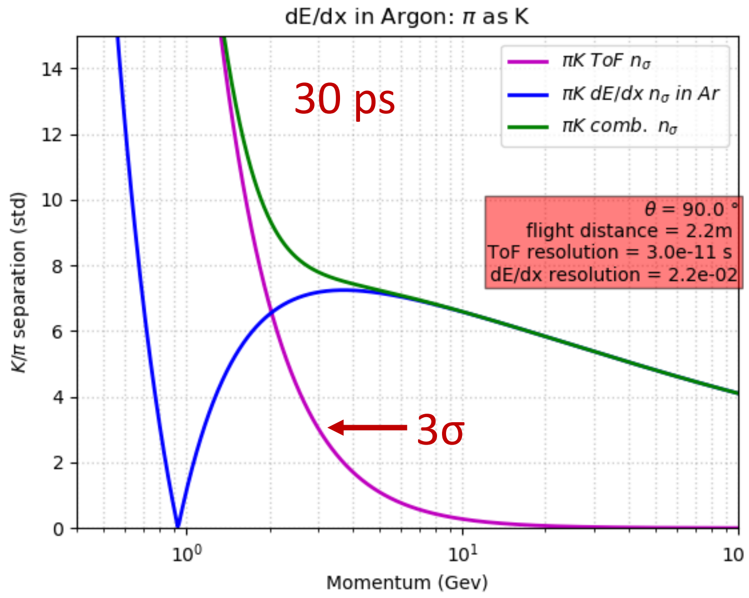
Motivation for PID

Flavor physics, Higgs decays to fermions, HNL mass…

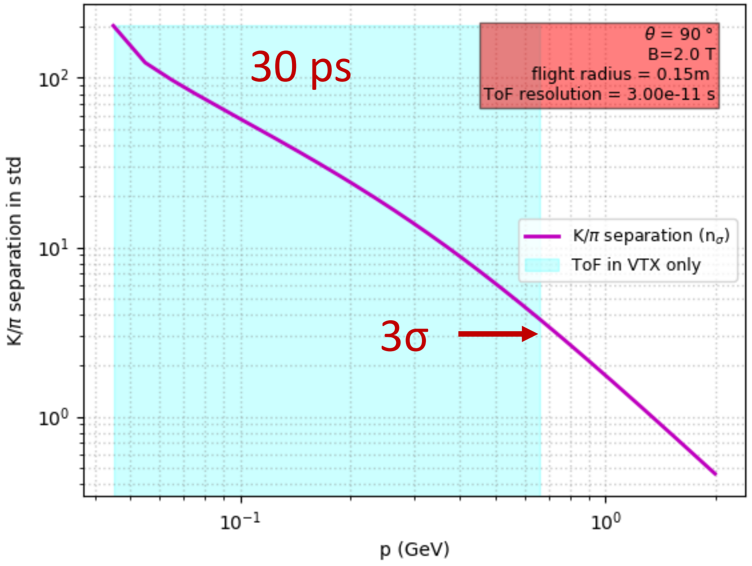
ToF ≃ 30 ps precision at ≃ 2.2(0.15) m provide 3σ π/K discrimination ≳ 3(0.66) GeV standalone

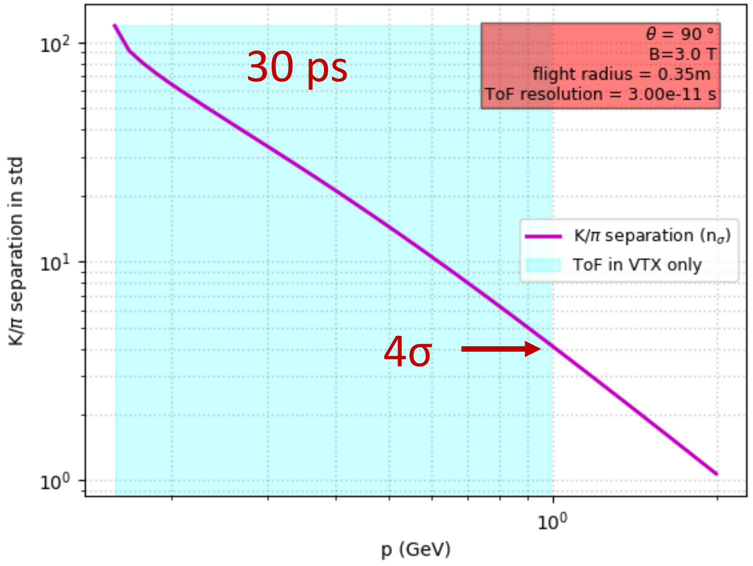
needed in the 1 GeV region to complete dE/dx and dN/dx in LGVD*

strong interest to have combined position and timing precision in a same sensor



courtesy R. Aleksan





a layer at 15 cm would allow 3σ discrimination up to the 2 T-field cutoff of 0.66 GeV at 2.2 m
at 3T the momentum cut-off is 1 GeV at 2.2 m a ToF layer would be useful in front of the LGVD at 35 cm
position precision target in r/Φ 5(7) µm at .35(2.2) m

** Large Gas Volume Detectors (Drift CHamber or Time Projection Chamber)*

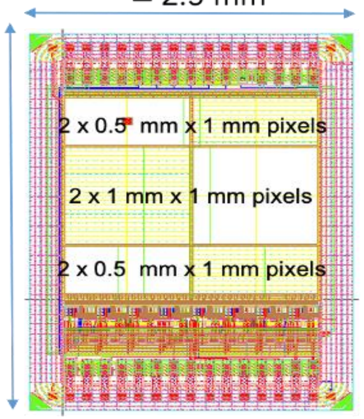
ToF PID / Tracking Layers

Monolithoc CMOS and LGADS

w/o gain | w/ gain

Mini CACTUS-V2 IRFU

LFoundry 150 nm,
175 µm, 0.5 x 0.5 mm^2
≃ 60 ps precision

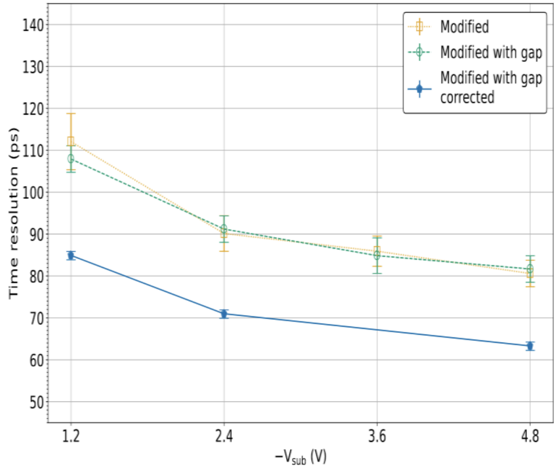


w/ gain layers started

P. Schwemling/D. Contardo

TPSCo 65 nm

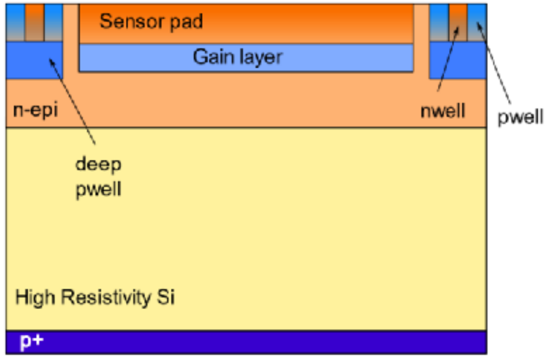
modified with gap
10 µm epi., pitch 10 µm
63 ps precision

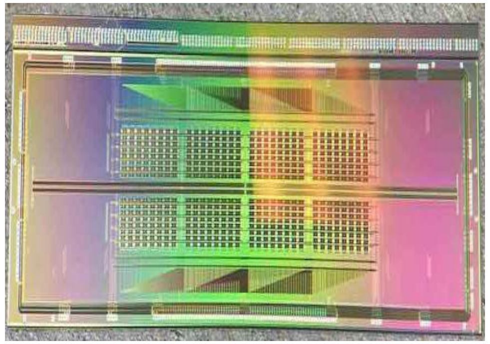


IP2I plans to develop
async. readout architecture
ToA/ToT at end of column

ARCADIA-MADPIX M. Rolo

LFoundry 110 nm, w/gain
48 µm, 250 x 100 μm^2
≃ 72 ps precision**

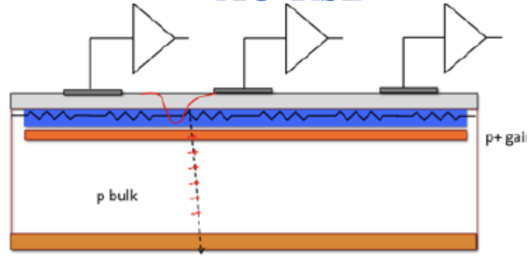




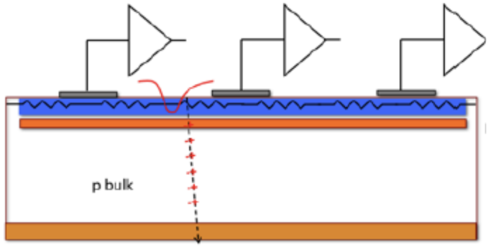
INFN-FBK LGADs E. Robuti

hybry design
50 µm, .45 x .45 mm^2
≃15/50 µm/ps precision

AC-RSD



DC-RSD



New design pads
trench isolated
to control charge sharing

** the technology could be deployed in first layers of a Si/W elctromagnetic calorimeter and a LumiCal, ** not correcteed for time reference resolution*

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Monolithoc CMOS and LGADS

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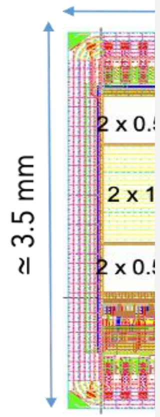
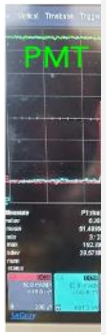
LFoun
175 µm,
≃ 60





w/ gain

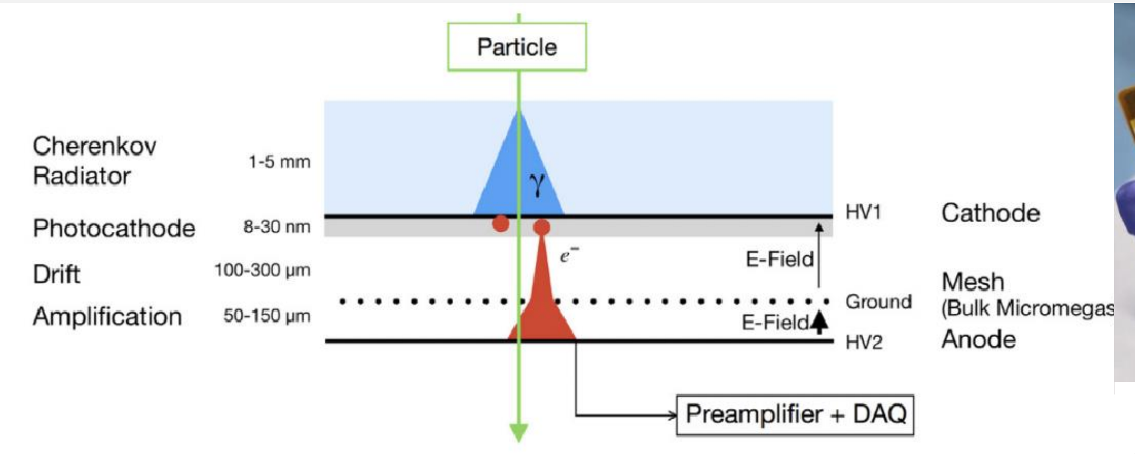
General MCMOS/LGAD technology problematics

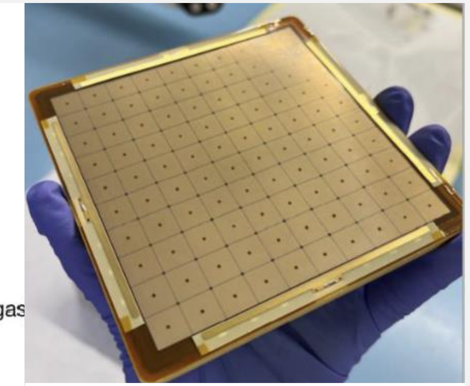
- Intrinsic time precision limit w/ and w/o gain layer
  - versus pixel size/pitch - active thickness - capacitance
- Position precision
  - channel density versus position/timing performance (driving power)
- low power premplification

Other MCMOS technology R&D

- TJ 180 nm CASSIA CERN, w/ amplification ≃ 50 x 50 µm^2
- SiGe tecnnology UniGe (not commercial), w/o and w/ amplifications

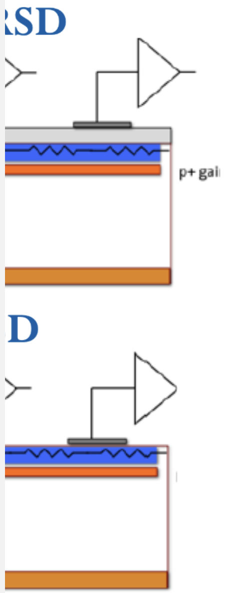
MPGD - ex. Picosec T. Papaevangelou





30 – 35 ps precision

s E. Robuti
5 x .45 mm^2
precision



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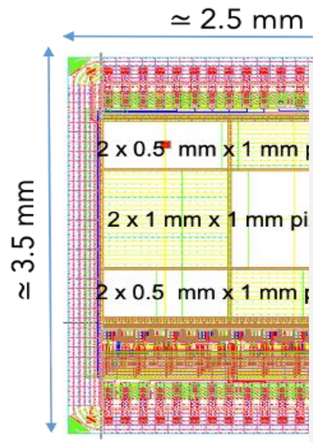

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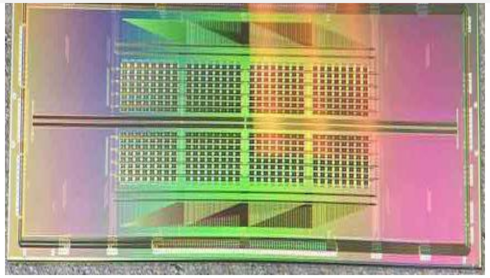

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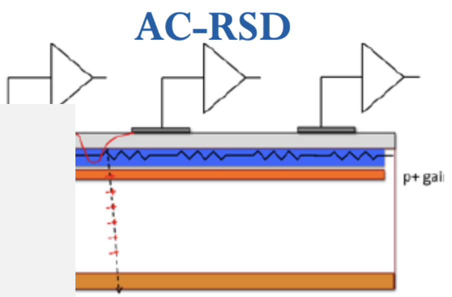

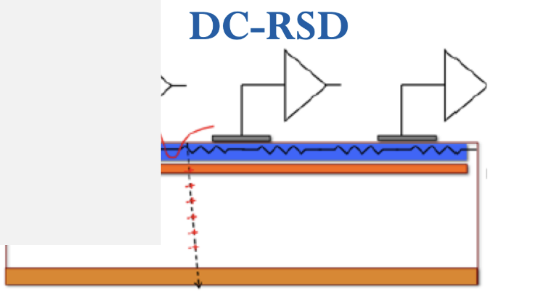

New design pads trench isolated to control charge sharing determined

System aspects

- Power management
  - number of layers versus standalone performance and power sum
  - X/X_0 versus power
- Mechanical structure and services similar as for VD
  - stave design - sensor size and thickness tbd
  - bent design – oriented to large and thin sensors

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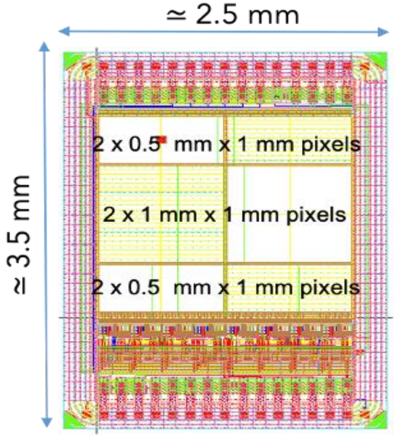

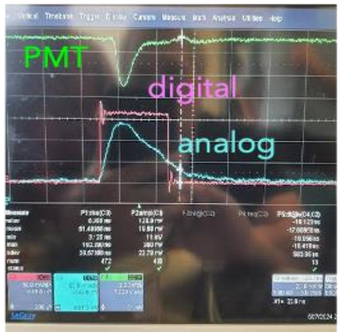

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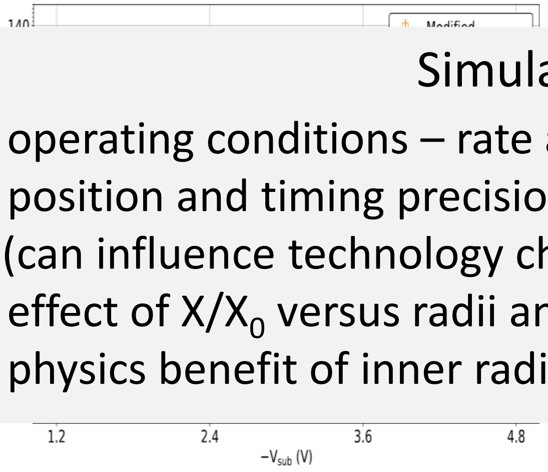

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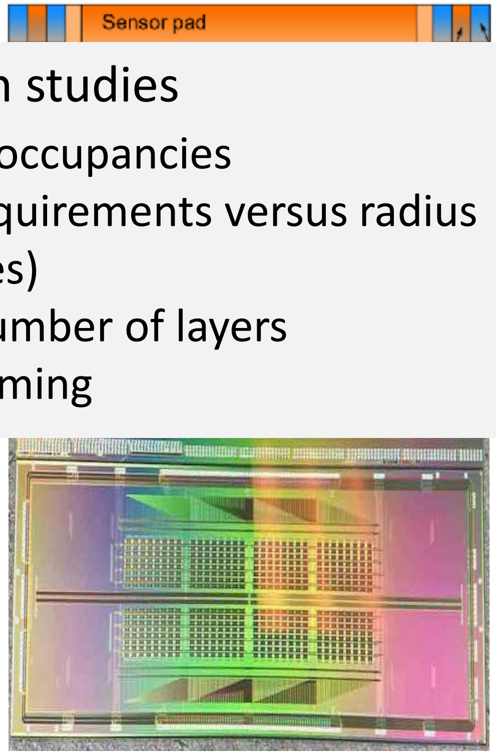

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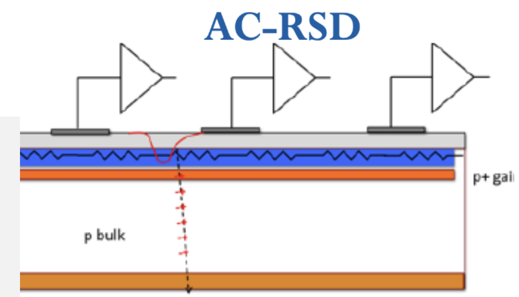

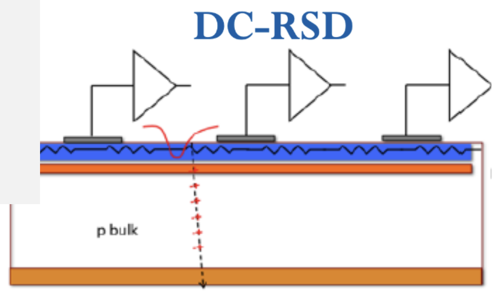

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Simulation studies

- operating conditions – rate and occupancies
- position and timing precision requirements versus radius (can influence technology choices)
- effect of X/X_0 versus radii and number of layers
- physics benefit of inner radius timing

** the technology could be deployed in first layers of a Si/W elctromagnetic calorimeter and a LumiCal, ** not correcteed for time reference resolution*

Outlook

- Sensor R&D
  - different technologies shoud eventually converge on similar performance for VD
  - technology alternative(s) to achieve PID/Tracking is (are) yet to be established
  - ➢ work will continue in the first 3-4 years DRD period for comparative evaluations
  - ➢ on longer term, 3D wafer stacking, finer foundry nodes, could shed new light for channel density and power consumption (DRD& mandate)

- System aspects are crucial, they may limit the performance
  - particularly for X/X_0, MDI integration and systematic effects

- Simulation studies are needed
  - to guide R&D
  - to define and refine detector configurations and requirments (as a function of r/η)
  - to assess effects of hermeticity, acceptance, mis-calibrations

France and Italy are developing complementary technologies
and system approaches, synergies can be exploited
EoIs foressen on VD, tracking Wrapping Layers and ToF/Tracking Layers

Outlook

- Sensor R&D
  - different
  - technolo
  - ➢ work w
  - ➢ on long … annel density and pov
- System aspe
  - particula
- Simulation (
  - to guide
  - to define
  - to assess

Features	Earlier experiments	FCC inner vertex	FCC outer vertex	FCC wrapper
10 um pitch				
"effective" 10 um pitch with charge sharing				
20 ns time-stamping				
30 ps time resolution				
Serial powering capability				
Chip-to-chip data transmission				
10 mW/cm2 power				
50 mW/cm2 power				
100 mW/cm2 power				
Extreme stitching (20 cm size sensors)				
Moderate stitching (4 cm size sensors)				

Monolithic CMOS
common technology matrix
A. Andreazza
can be connected to system and
simulation aspects

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EoIs foressen on VD, tracking Wrapping Layers and ToF/Tracking Layers