Development and performance of the Real-Time Muon Reconstruction for the L0 Trigger in HL-LHC ATLAS

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Abstract

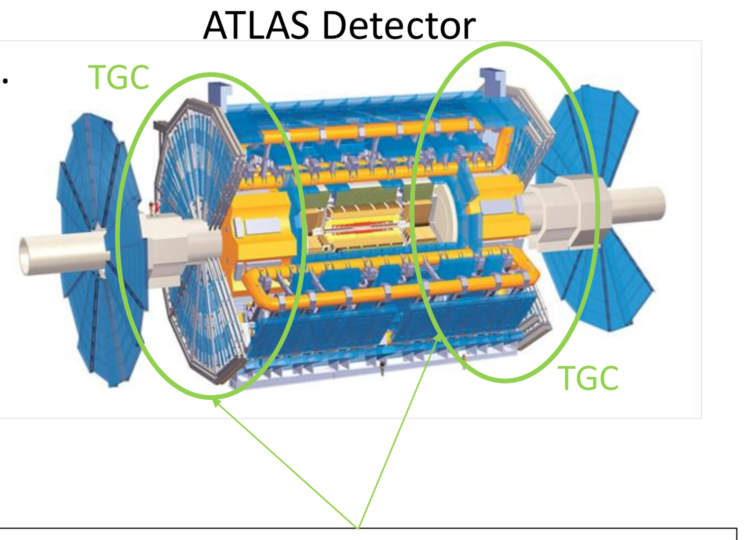
We will present a detailed performance assessment of the implemented logic and provide an in-depth discussion of the validation strategy and methodology, which has been successfully integrated into our development workflow for the muon reconstruction in the Level-0 (L0) trigger for the High-Luminosity LHC (HL-LHC). The muon trigger will be fully upgraded with a real-time reconstruction system. The new logic, implemented on a large-scale FPGA, identifies and reconstructs muon tracks using hit coincidences within the same bunch crossing and pattern-finding algorithms realized with Look-Up Tables in RAM. Designed as a pipeline trigger logic, it processes all the events at the 40 MHz collision rate with a fixed latency. To ensure reliability, we have developed a comprehensive verification framework consisting of a test vector generator, bitwise simulator, firmware RTL (register transfer level) simulator and actual hardware. The firmware has undergone extensive validation using test vectors derived from Monte Carlo simulations. Intensive debugging has resulted in significant improvements, represented by enhanced plateau efficiency and momentum resolution in RTL simulation. The final performance has been evaluated in terms of efficiency as a function of transverse momentum, pseudorapidity and azimuth angles using a high-statistics dataset of simulated tracks. The evaluated performance is consistent with the expected one and the results from bitwise and RTL simulators are in agreement.

1. TGC Electronics for the High-Luminosity LHC

The ATLAS Experiment at the LHC

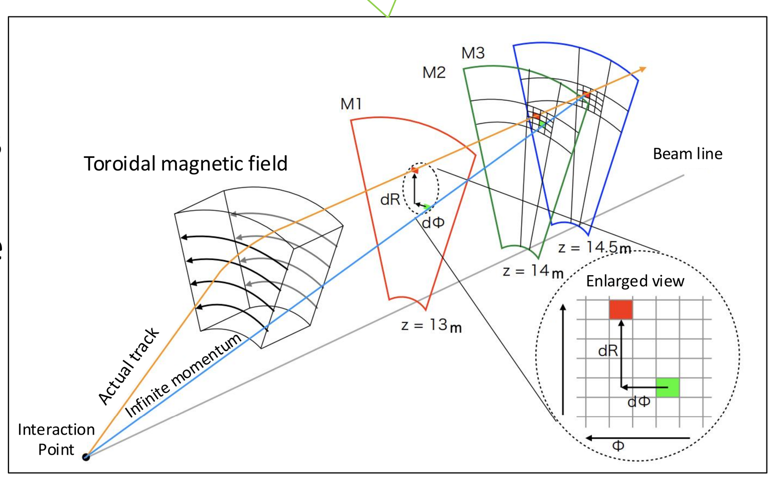
- $\sqrt{s}$ = 13.6 TeV and proton bunch crossing at 40 MHz.
- ATLAS detector consists of Inner Trackers, Calorimeters and Muon Detectors.
- The aim is to measure Standard Model (SM) and explore beyond SM scenarios.

ATLAS Detector



The L0 Muon Trigger

- Thin Gap Chamber (TGC) detector is used as muon trigger owing to its high-speed response gas.
- It covers endcap region (1.05 < |η| < 2.4).
- It performs real-time high-speed muon reconstruction by hit coincidence among three stations, each consisting of seven detection layers (M1, M2, M3 on the figure).
- It estimates transverse momentum by point angle measurement with toroidal magnetic fields.

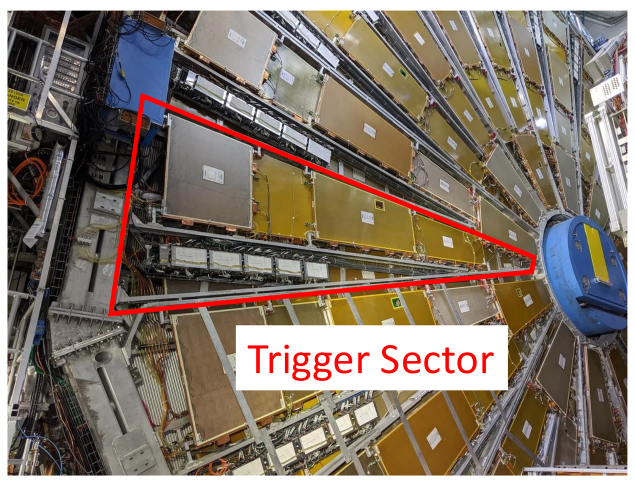


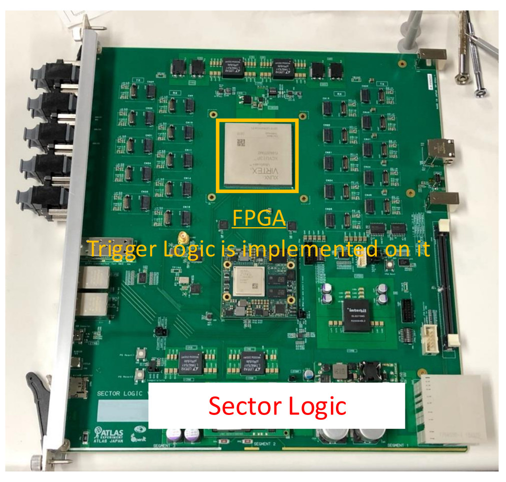
The HL-LHC and Phase-2 ATLAS Upgrade

- The HL-LHC will deliver an instantaneous luminosity roughly three times higher than the LHC in Run3.
- 1 MHz readout and a 10 µs latency for L0 trigger will be supported.

L0 Muon Trigger Electronics System Upgrade

- The muon trigger electronics system will be entirely replaced to cope with the new TDAQ specification.
- Every bunch crossing, frontend electronics will send all the hit bitmaps without reduction to the backend electronics i.e. Sector Logic (SL).
- In the new design, the full chain of trigger logic will be implemented in the SL.
- One SL board will cover one trigger sector, for a total of 48 SL boards covering the entire endcap region (1.05 < |η| <2.4).





Sector Logic

- The SL receives all channels' hit binary information for each bunch crossing.
- Pattern finding is performed with the received hit bit maps for every bunch crossing.
- Muon track candidates are identified and transverse momentum is evaluated with fixed latency.

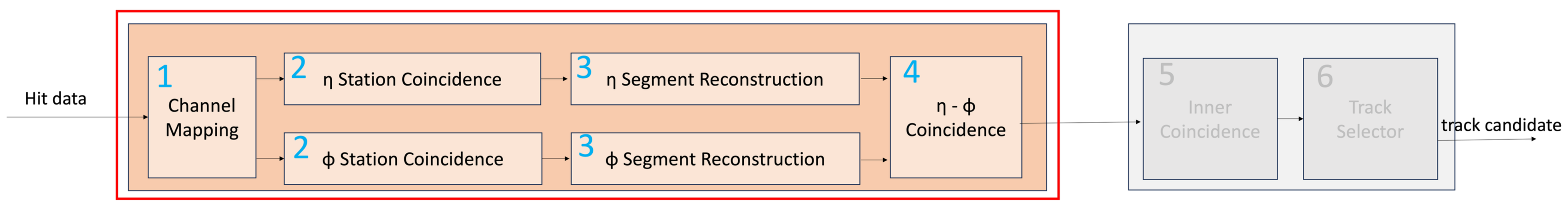
2. Trigger Logic and Development status

The trigger logic consists of the following six major components:

1. Channel Mapping: formats hit data into trigger logic input.
2. Station Coincidence: selects hit positions using the coincidence of hit channels in each station out of three stations.
3. Segment Reconstruction: a pattern-finding algorithm identifies the combination of hit positions among the three stations. The combination should be consistent with a straight track through the three stations. Two dimensions are separately treated (i.e. η and ϕ direction), and the IP-pointing information (dη, dϕ) of the identified patterns is delivered.
4. η – ϕ Coincidence: the combination of two dimensions that are consistent with trajectories from IP are formed. Using the (dη, dϕ) information, transverse momentum p_T is evaluated with Look-Up-Tables.
5. Inner Coincidence: filters out fake muon backgrounds using other detectors inside the toroidal magnetic fields.
6. Track Selector: prioritizes track candidates and selects six candidates.

2. Trigger Logic and Development status

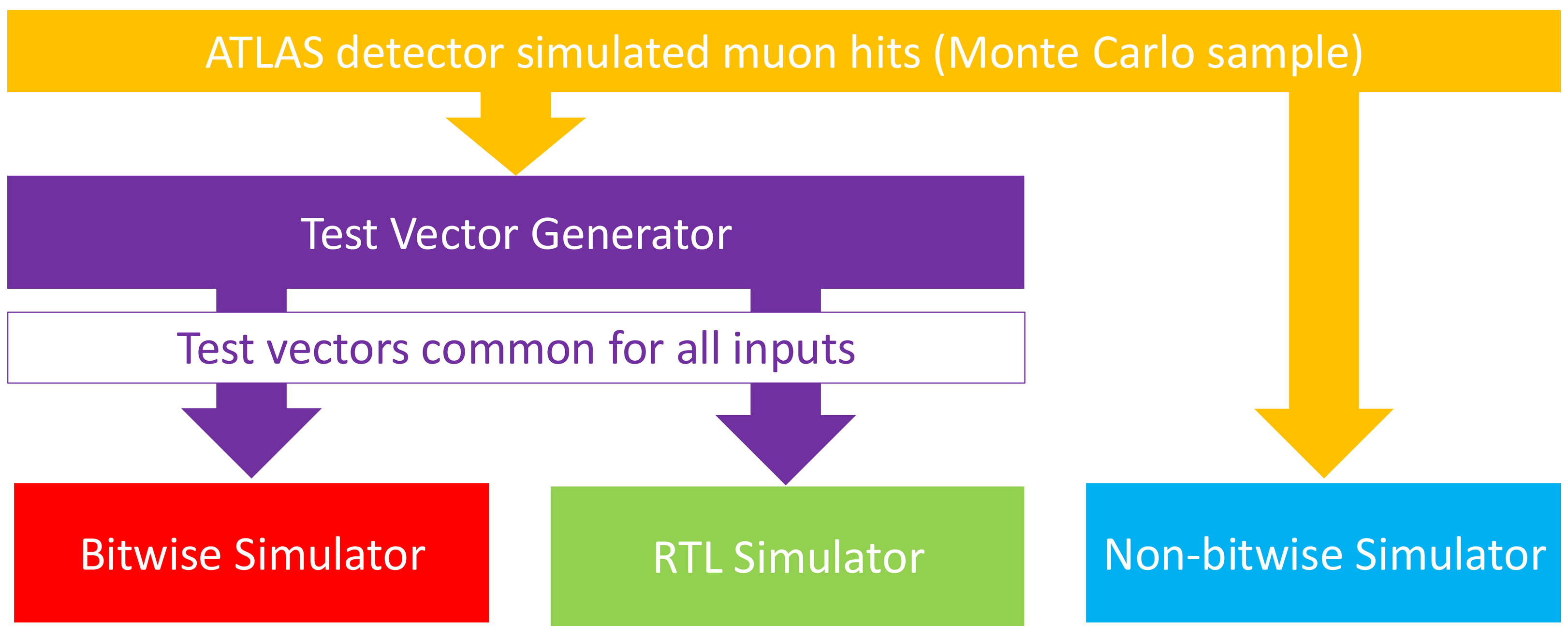
The integrated logic chain up to η – ϕ coincidence has been extensively tested with software, firmware and actual prototype electronics.



3. Verification System Overview

- The Test Vector Generator converts simulation muon data into the input format required by trigger logic.
- The Bitwise Simulator is a C++ program that reproduces the trigger logic behavior at the bit level.
- The Register Transfer Level (RTL) Simulator models the behavior of the trigger logic firmware using the implemented Hardware Description Language (HDL) code.

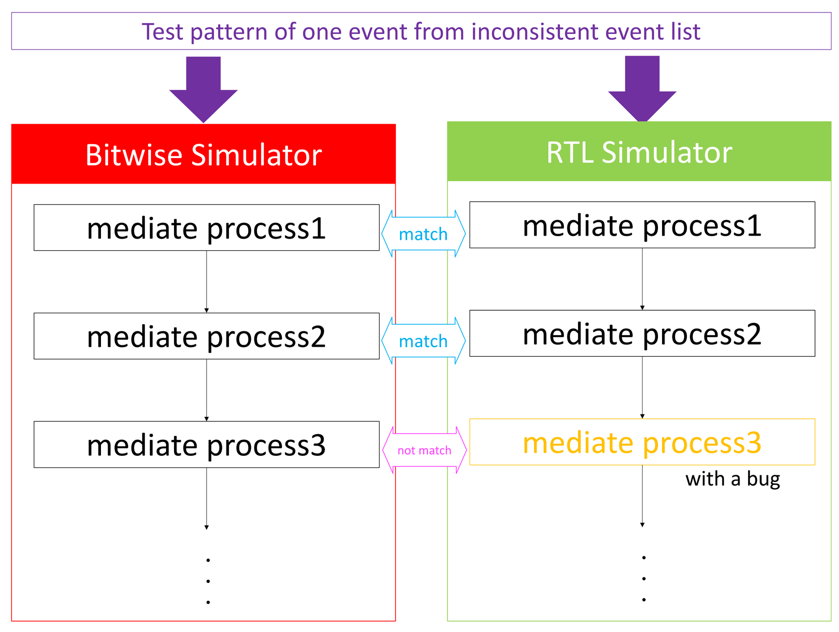
Full agreement between the Bitwise Simulator and the RTL Simulator is required.
Additionally, the Non-bitwise Simulator is used to evaluate the ideal performance of the trigger algorithm before firmware development begins, serving as a performance reference.



4. Debugging Process

The Bitwise Simulator and the RTL Simulator can both probe all signal lines within the trigger logic. We used these tools in the following way:

1. Test vectors were prepared using single-muon Monte Carlo simulations.
2. A bitwise comparison was performed, and events showing discrepancies between RTL and Bitwise Simulator were identified.
3. Intermediate outputs were thoroughly examined to locate the source of inconsistencies and appropriate fixes were applied.



Result of Fixes:
The number of inconsistent events before and after the fixes is shown below.

The number of inconsistent events out of 8,603 events		
Trigger logic	Before	After
Segment Reconstruction	O(1000)	0
Wire Strip Coincidence	O(1000)	0

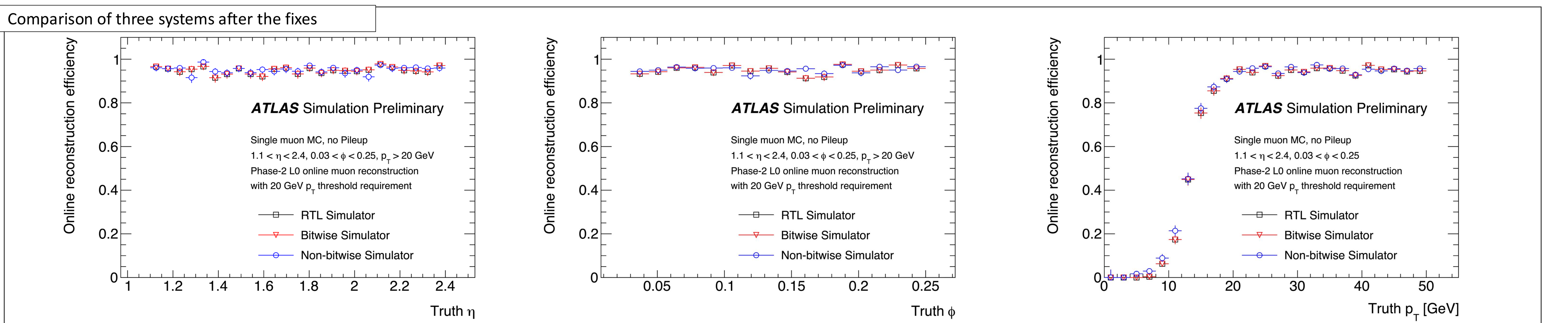
This confirms that the firmware and software match perfectly.
An example of a bug: the selector logic in Segment Reconstruction and η – ϕ Coincidence. Trigger logic includes modules selecting the most truth-like track out of many track candidates. The selection condition was incorrect, causing the loss of the true track.

5. Evaluation of Performance

Precise consistency between the RTL and Bitwise Simulators is observed, demonstrating bitwise accuracy of the implementation. In addition, both RTL and Bitwise performances show good agreement with the Non-bitwise simulation, confirming the correctness of the firmware-level implementation relative to the idealized algorithm. The plateau efficiency (p_T > 20 GeV) reaches about 95%.

The Monte Carlo samples used: Single muon events with p_T< 50 GeV, 1.1 < η < 2.4, 0.03 < ϕ < 0.25 and no pileup.

Comparison of three systems after the fixes



※Online reconstruction efficiency = the fraction of muons satisfying the above conditions whose reconstructed pT exceeds 20 GeV.

The developed verification system significantly enhances the performance of the muon trigger logic for HL-LHC and serves as a robust framework for future upgrades!

The details of the plots: ATLAS collaboration, *L0 Muon Trigger Public Results*, https://twiki.cern.ch/twiki/bin/view/AtlasPublic/L0MuonTriggerPublicResults