



CRU IpGBT fPLL Status

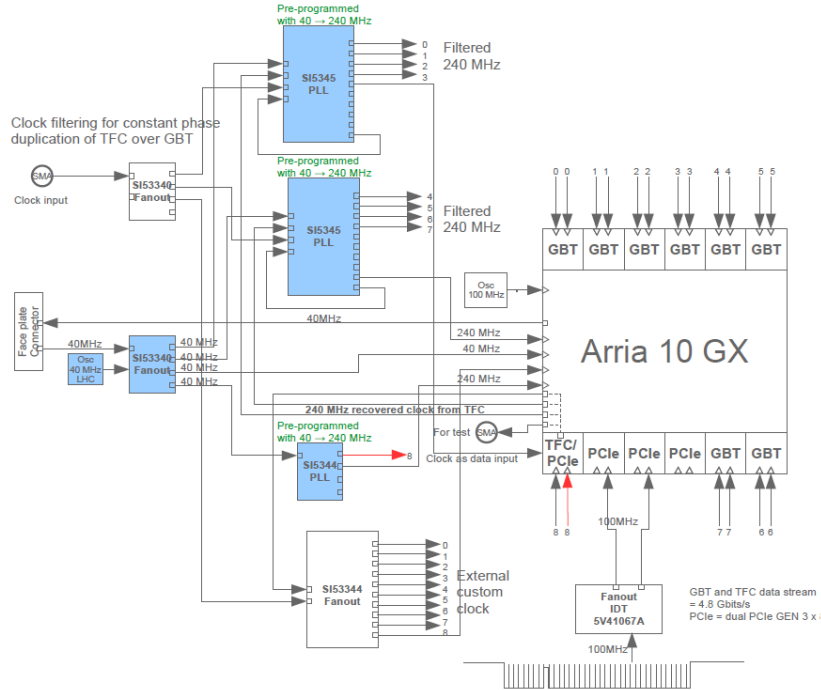
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CRU clocking scheme

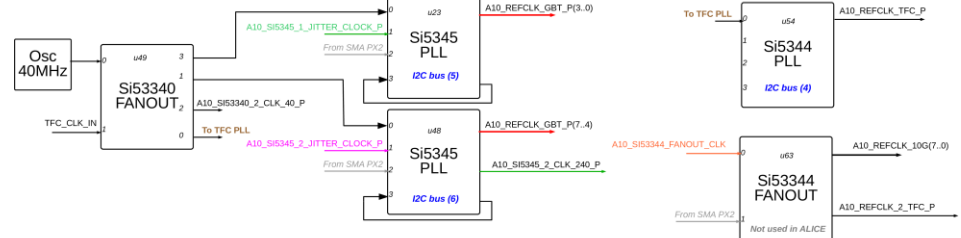


ALICE

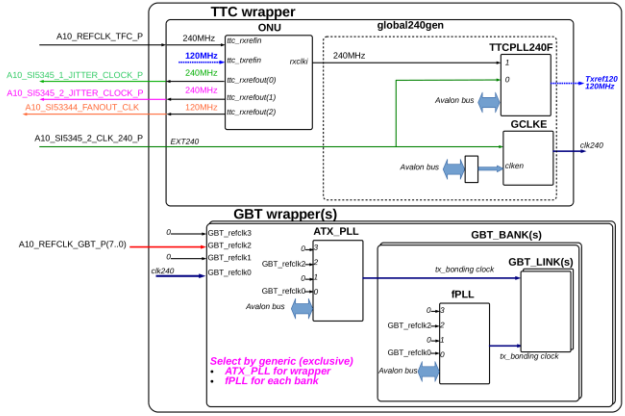
Clock Tree PCIe40V2



FW clocking



FPGA



ATXPLL vs. fPLL

