Contribution ID: **47** Type: **Poster**

The ANTARES4 Readout ASIC for the Second Flight of the GAPS Experiment

Tuesday 13 May 2025 22:26 (2 minutes)

The General Antiparticle Spectrometer (GAPS) is a stratospheric balloon experiment designed to search for low-energy cosmic-ray antinuclei as potential indirect evidence of dark matter annihilation or decay. Flying over Antarctica, GAPS will complete three flights for a combined mission duration of approximately 100 days. By targeting the largely unexplored sub-250 MeV/n energy range, GAPS will enhance sensitivity to antideuterons and antihelium while also extending low-energy antiproton measurements below 100 MeV.

The GAPS instrument consists of a segmented tracker composed of over 1000 custom lithium-drifted silicon (Si(Li)) detectors, which enable x-ray spectroscopy and charged-particle tracking of antimatter interactions. The readout of the Si(Li) strip detectors is performed by a full-custom application-specific integrated circuit (ASIC), for which an upgraded version has been designed for the second flight.

This work will present ANTARES4 (ANTiparticle Asic REadout for SiLi detectors), a prototype ASIC designed in a commercial 65 nm CMOS technology, which includes eight analog channels, each featuring a Charge Sensitive Amplifier (CSA) with dynamic signal compression. A key innovation in this design is the implementation of a non-linear feedback capacitor using a dynamic threshold MOSFET (DTMOS) in the CSA. In this prototype, four different configurations of the DTMOS-based feedback capacitor have been included to be studied and compared with simulations, which indicate increased performance over a traditional MOS device employed as a nonlinear capacitor. This is required to handle the wide input dynamic range from 10 keV to 100 MeV, while preserving the necessary sensitivity for x-rays below 100 keV. Each silicon strip is expected to exhibit approximately 5 nA of leakage current at the operating temperature of -40 ℃. To accommodate this, charge restoration in the feedback capacitor is performed using a Krummenacher network, capable of handling up to 100 nA of leakage current. This ensures proper operation of the readout electronics both in flight and during ground testing at room temperature. Following the CSA, the signal is processed by a time-invariant CR–RC semi-Gaussian unipolar shaper with eight selectable peaking times.

The design for the chip has been submitted to the foundry. This work will present the readout channel of ANTARES4, detailing its architecture, noise optimization strategies, calibration capabilities, and the novel design solutions implemented in the ASIC.

Eligibility for ”Best presentation for young researcher” or ”Best poster for young researcher” prize

Yes

Author: GHISLOTTI, Luca (University of Bergamo and INFN Pavia)

Co-authors: Mr LAZZARONI, Paolo (University of Bergamo & INFN Pavia); MANGHISONI, Massimo (Università di Bergamo - Italy); RICEPUTI, Elisa

Presenter: GHISLOTTI, Luca (University of Bergamo and INFN Pavia)

Session Classification: Posters