ePIC Silicon Vertex Tracker

Overview, layout, production and integration

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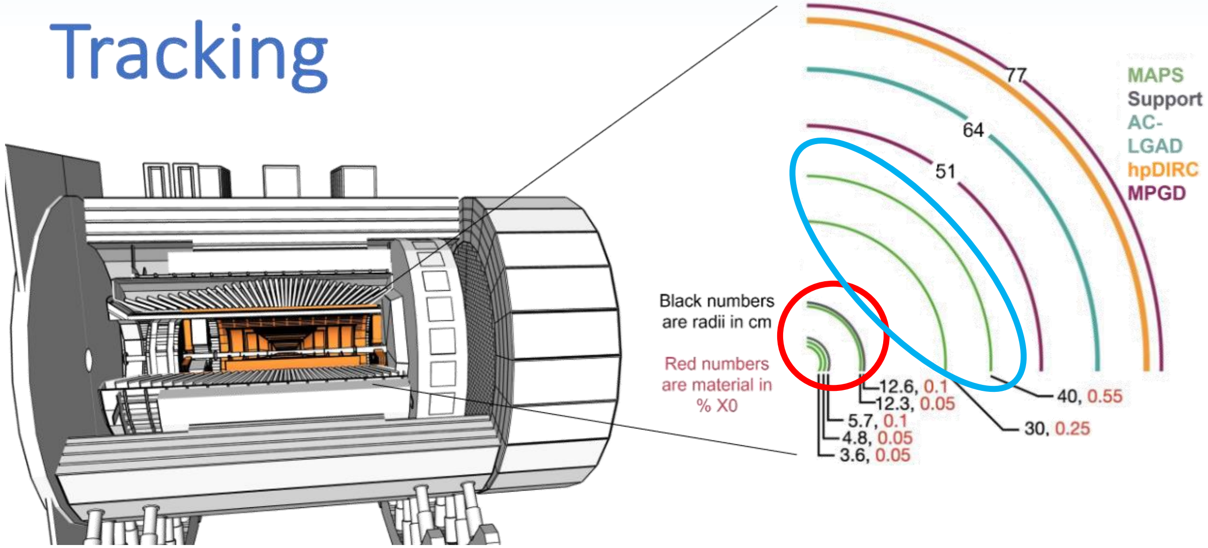
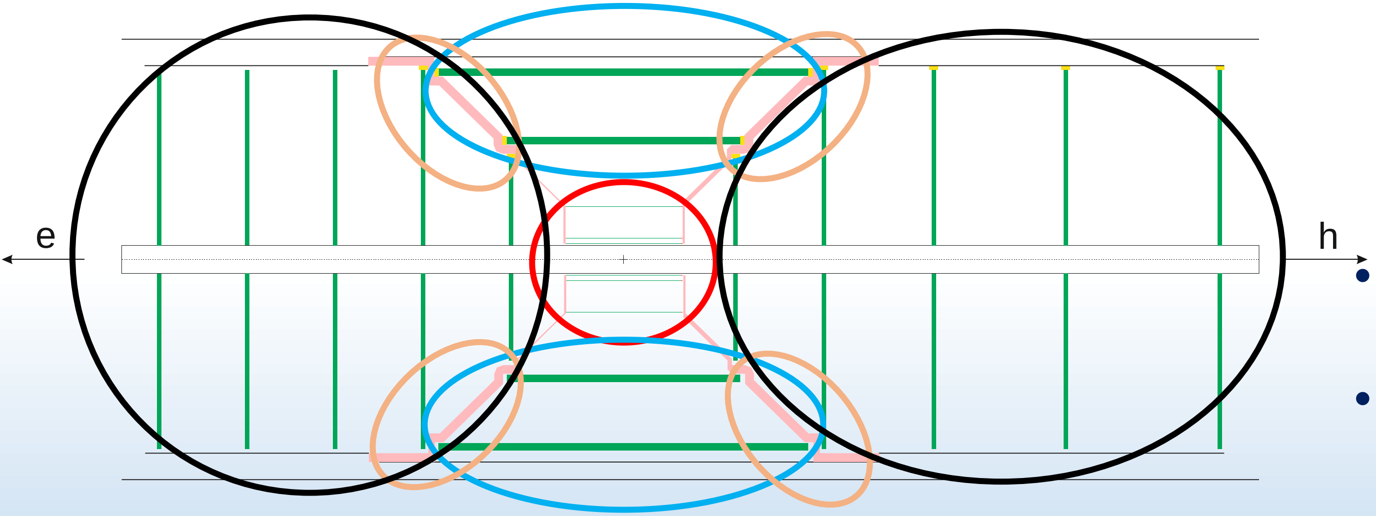
SVT

Tracking



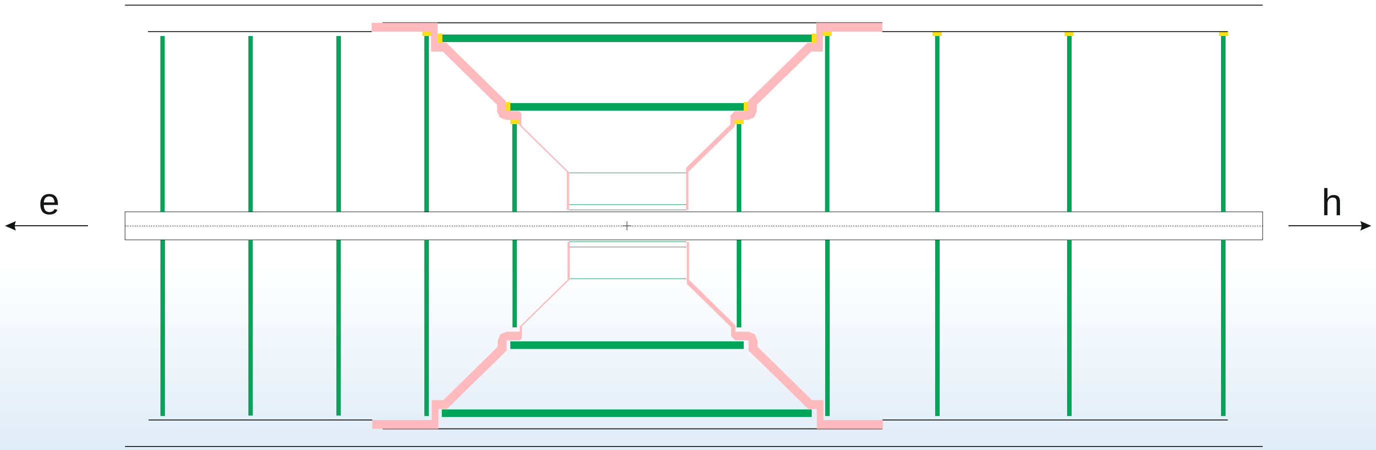


- 5 barrels, 5 disks (each end)
- Barrel
  - 3 layers inner barrel (IB): Half-cylinders out of bent silicon (like ALICE ITS3) – IT and US
  - 2 layers outer barrel (OB): Individual staves with carbon fibre structure – UK
    - ~1/3 of SVT
  - All barrel layers supported by carbon fibre support cone
- Disks: corrugated carbon-fibre half-disks - US
- Sensor will be an ultra-thin (40 μm), wafer-stitched CMOS sensor
  - Developed by ATLAS ITS3: MOSAIX
  - We will use MOSAIX for IB, and modification (EIC-LAS) for OB and disks
- Air cooling with flow contained in local support structures
- Radiation levels at EIC are significantly below LHC

Layer properties

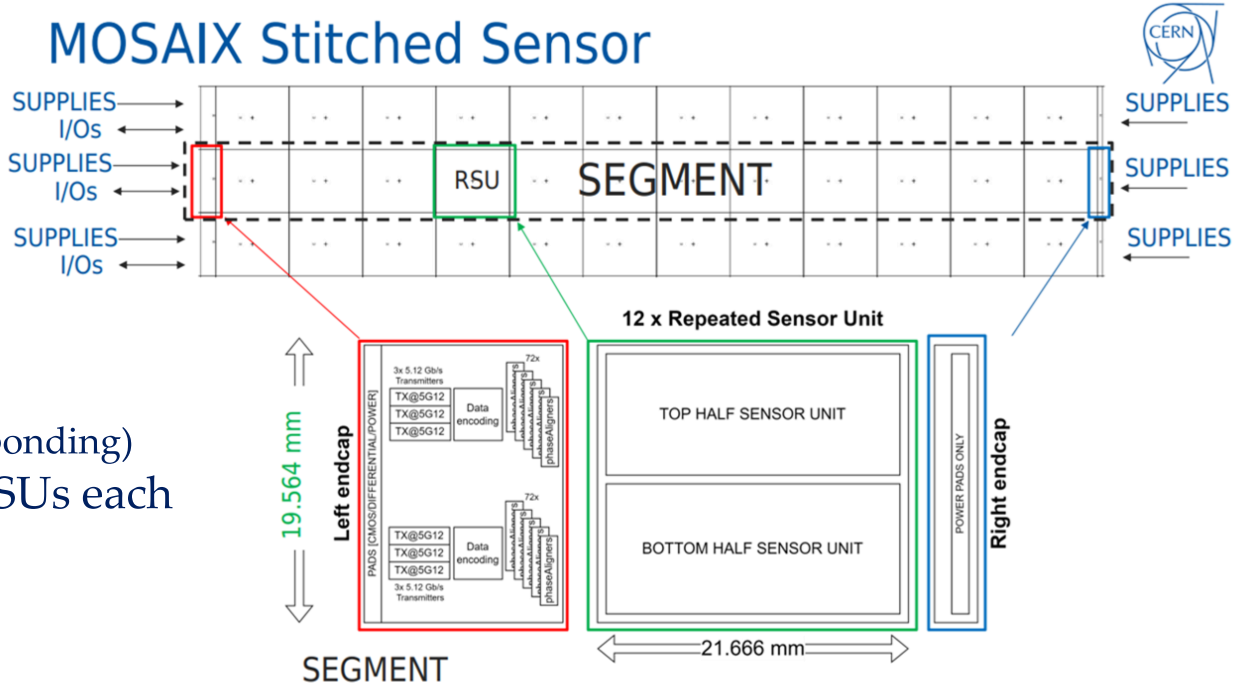
Barrel nominal dimensions		Layer radius [mm]	Layer lengths [mm]	X/X_0 [%]
IB	L0	36	270	0.05
	L1	48	270	0.05
	L2	120	270	0.05
OB	L3	270	540	0.25
	L4	420	840	0.55

	disk	z [mm]		disk	z [mm]	Outer radius [mm]	X/X_0 [%]
Electron side	ED1	-250	Hadron side	HD1	250	240	0.25
	ED2	-450		HD2	450	415	0.25
	ED3	-650		HD3	750	421	0.25
	ED4	-850		HD4	1000	421	0.25
	ED5	-1050		HD5	1350	421	0.25

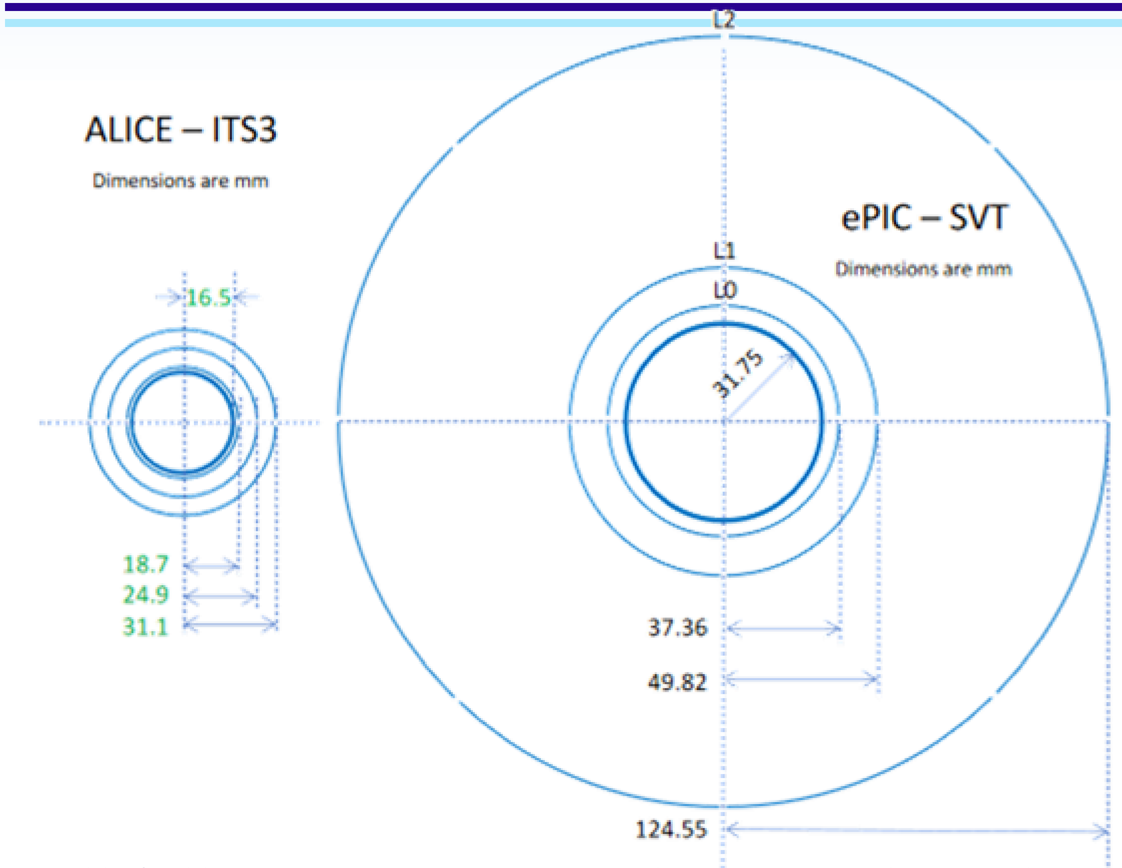


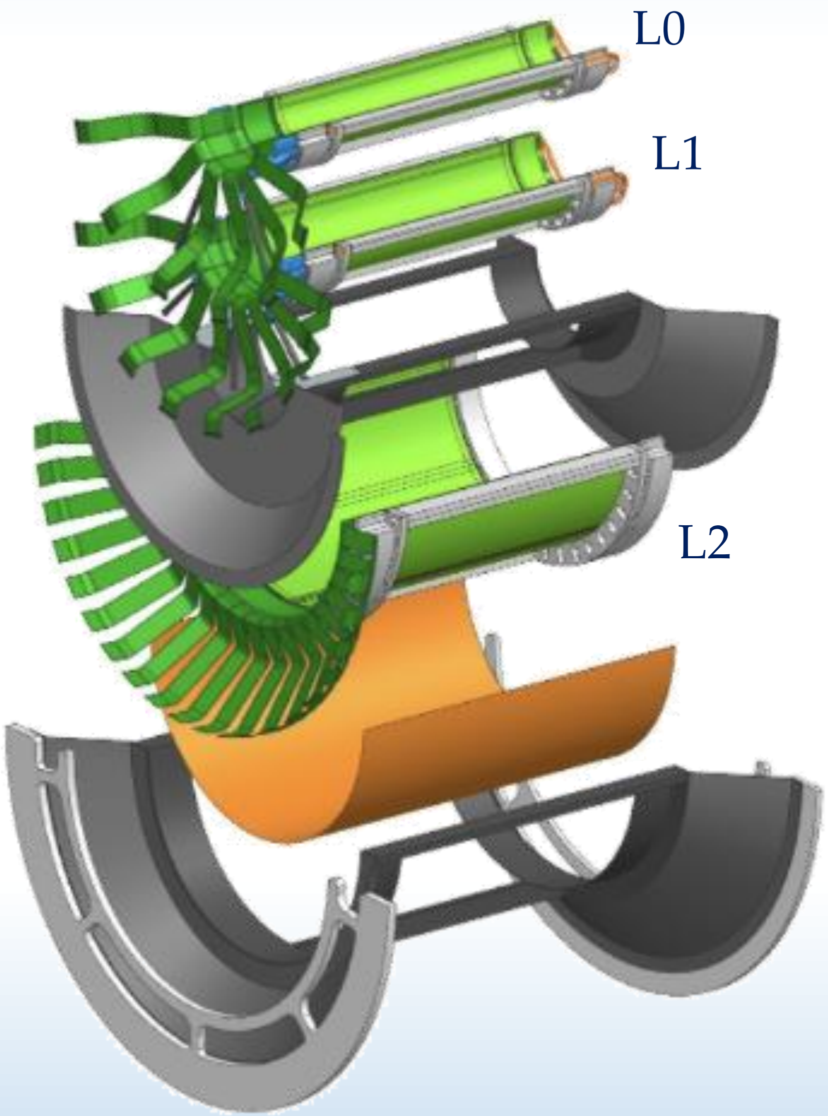
Sensors

- MOSAIX (ALICE ITS3)
  - CMOS Monolithic Active Pixel Sensors
    - Front-end electronics is integrated with sense elements
  - Repeated Sensor Unit (RSU) – 12 off
    - Contains sense elements & power/read-out distribution
  - Left and Right End-cap (LEC and REC)
    - Chip-common functions (control, power, multi-plexing, etc.)
  - Internal connections between sections by stitching
    - No external cables required, connections only to LEC (by wire-bonding)
  - MOSAIX sensors with 3, 4 or 5 segments (rows) of 12 RSUs each
  - Silicon is thinned down to 40 µm
    - This makes it flexible enough that it can be bent
- EIC-LAS
  - MOSAIX is developed for a small size (0.12 m^2) vertex detector
    - ePIC SVT is much larger (about ×50) → yield becomes a significant concern
    - Also need more flexibility to cover complex shapes (in particular disks)
  - EIC-LAS will consist of one segment of 5 or 6 RSUs each with a LEC
  - Modifications to the chip design (mostly in LEC) required (UK involved)



ALICE ITS3 and ePIC IB





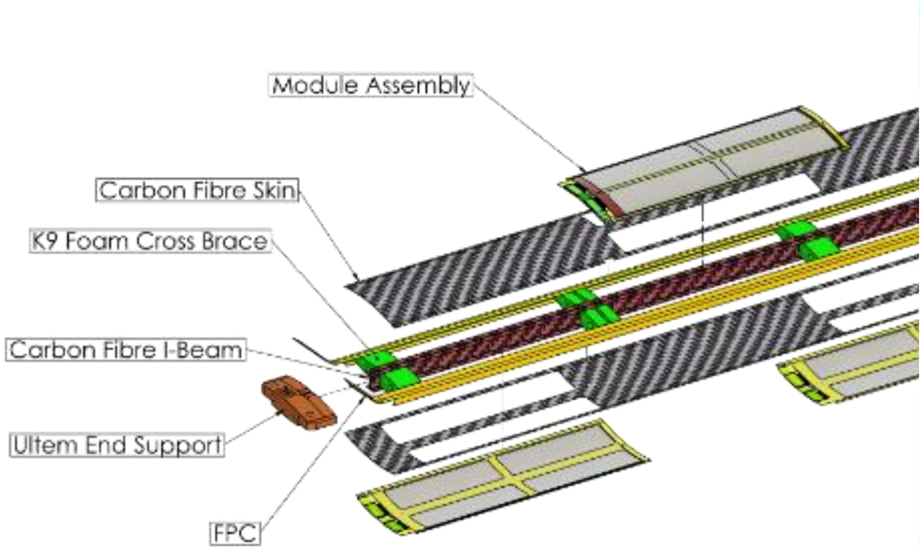
- IB will follow ALICE ITS3 design in barrel
- But already with significant changes
  - ePIC IB is more than 2 times larger than ITS3
  - Due to the beam pipe geometry, and the need for full disk acceptance services need to be routed along service cones

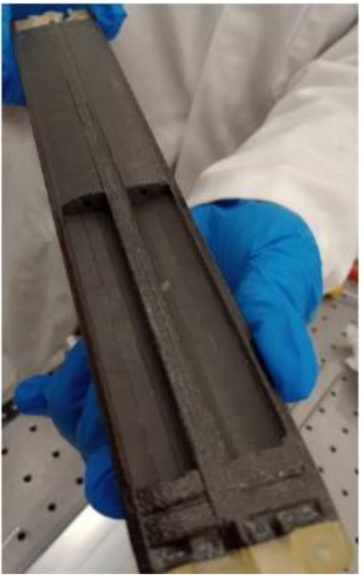
Power and cooling

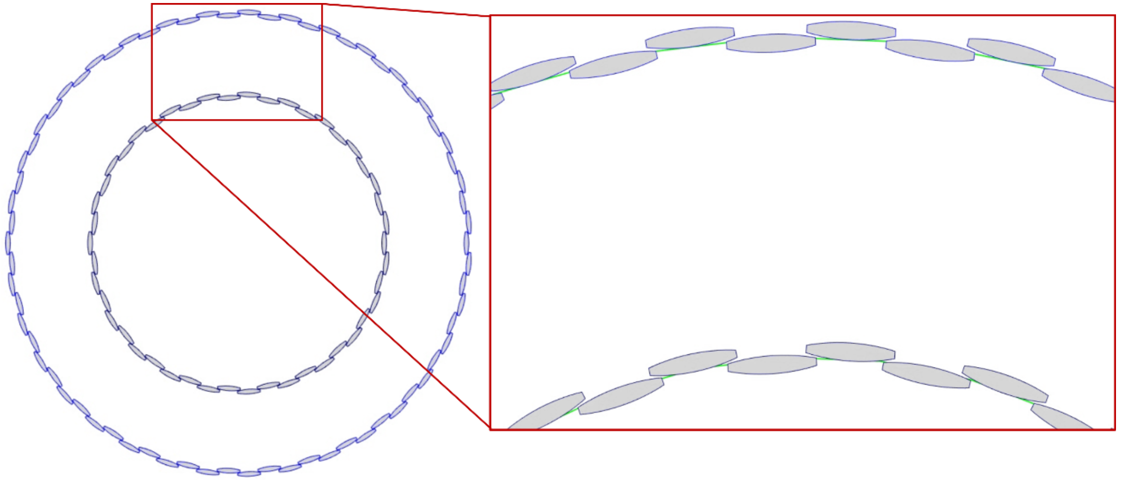
- Due to large size of SVT we need to supply individual LAS with cables
  - Flexible Printed Circuits (FPCs) – 14 µm Al traces on 25 µm Kapton carrier
  - To reduced number of lines (material) use serial powering
    - Supply current flows through four consecutive LAS
    - To cope with load variations this requires a set of auxiliary electronics, called a shunt Low-Drop-Out (LDO) regulator
    - This, and other circuitry required for control and powering will be integrated into an ancillary chip (AncASIC) – designed for ePIC with UK involvement
      - One AncASIC per LAS
- The heat generated by the sensors (1-2 W per LAS), and AncASIC (35-45% of LAS power), and by ohmic losses in the FPC (20-30% of LAS power) needs to be removed by a cooling system
  - Like ALICE ITS3 we plan to do this by flowing air close to the heat sources
    - Eliminates material associated with liquid or evaporative cooling
  - In ePIC SVT this air flow will be contained within mechanical support structures of OB staves and disks
    - This gives us reliability and predictability
  - Required air speeds (for a coolant ΔT=10°C between input and output) will be around 10 m/s
    - This is significant, and will induce mechanical loads on the support structures

OB

- Segmented into staves as long as each barrel
  - Supported from support cones at each end – this includes service connections
- Modules (2 LAS side-by-side + 2 AncASICs on common carrier)
  - Glued on openings in stave skin
- Hollow stave core with CF central spar and face sheets
- Cross-ribs from thermally conductive carbon foam
- Side close-outs from Kapton (FPCs)
- Current design has curved surfaces (with curved silicon modules)
  - Evaluate layout benefits vs manufacturing challenges (bonding)





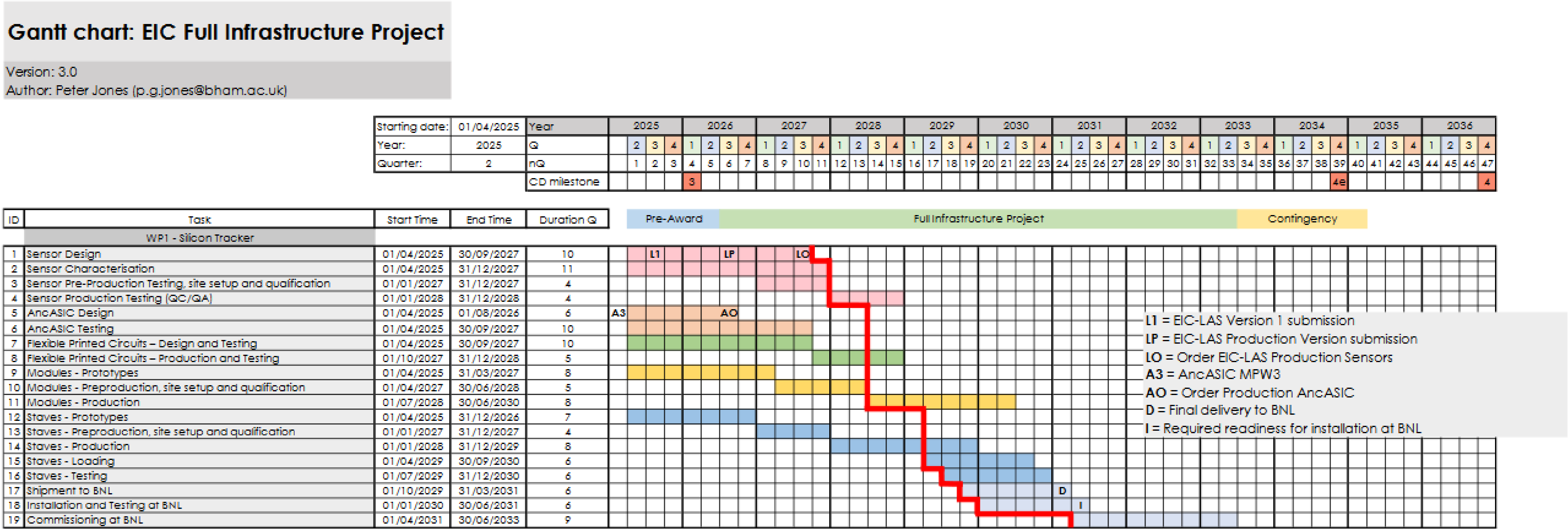


Layer	Innermost radius [mm[	Outermost radius [mm]	RSU/LAS	Staves/layer	LAS/stave AncASIC/stave	LAS/layer AncASIC/layer	Power/stave (max) [W]
L3	264.75	279.25	6	46	8	368	22.0
L4	416.75	431.2	5	70	16	1120	47.3

The UK SVT project

- The UK deliverable to the SVT will be the L3 and L4 staves
  - All aspects: modules (with LAS and AncASICs), FPCs + RDOs, stave structures, all electrical connections bonded
  - Fully tested
  - Will be shipped to BNL for integration on support cones
    - We probably also want to be part of that integration
- Within the UK two centres of construction activity
  - Modules, module wire bonding, module testing: Birmingham, Daresbury Lab, Liverpool
  - Staves, stave integration (incl. TAB) and testing: Oxford, RAL
  - Other test activities (wafer probing etc.): Birmingham, Daresbury, RAL, Brunel
- The wide field of construction activities, and of the expertise we bring to the project means that we are already involved in the project at all levels
  - One co-TC and in almost all international WPs one WP coordinator from the UK

Timeline



Gantt chart: EIC Full Infrastructure Project

Version: 3.0
Author: Peter Jones (p.g.jones@bham.ac.uk)

Starting date:	01/04/2025
Year:	2025
Quarter:	2

CD milestone: 3 (2026 Q1), 4e (2034 Q4), 4 (2036 Q4)

Pre-Award | Full Infrastructure Project | Contingency

ID	Task	Start Time	End Time	Duration Q
	WP1 - Silicon Tracker			
1	Sensor Design	01/04/2025	30/09/2027	10
2	Sensor Characterisation	01/04/2025	31/12/2027	11
3	Sensor Pre-Production Testing, site setup and qualification	01/01/2027	31/12/2027	4
4	Sensor Production Testing (QC/QA)	01/01/2028	31/12/2028	4
5	AncASIC Design	01/04/2025	01/08/2026	6
6	AncASIC Testing	01/04/2025	30/09/2027	10
7	Flexible Printed Circuits – Design and Testing	01/04/2025	30/09/2027	10
8	Flexible Printed Circuits – Production and Testing	01/10/2027	31/12/2028	5
9	Modules - Prototypes	01/04/2025	31/03/2027	8
10	Modules - Preproduction, site setup and qualification	01/04/2027	30/06/2028	5
11	Modules - Production	01/07/2028	30/06/2030	8
12	Staves - Prototypes	01/04/2025	31/12/2026	7
13	Staves - Preproduction, site setup and qualification	01/01/2027	31/12/2027	4
14	Staves - Production	01/01/2028	31/12/2029	8
15	Staves - Loading	01/04/2029	30/09/2030	6
16	Staves - Testing	01/07/2029	31/12/2030	6
17	Shipment to BNL	01/10/2029	31/03/2031	6
18	Installation and Testing at BNL	01/01/2030	30/06/2031	6
19	Commissioning at BNL	01/04/2031	30/06/2033	9

L1 = EIC-LAS Version 1 submission
LP = EIC-LAS Production Version submission
LO = Order EIC-LAS Production Sensors
A3 = AncASIC MPW3
AO = Order Production AncASIC
D = Final delivery to BNL
I = Required readiness for installation at BNL

- Aligns with the EIC Project Schedule and UKRI/STFC profile restrictions
- Production starts 2027/2028
- Stave delivered to BNL 2030-2031

Summary

- The ePIC SVT is an extremely challenging project
  - Very aggressive material requirements
- It involves state-of-the-art (and beyond) technologies
- It builds on developments for ALICE ITS3, but is a project with its own challenges
- The UK is committed to deliver an critical part of the SVT, the OB staves
  - This constitutes about 1/3 of the silicon area
  - We will deliver components which will contain all components of the system (sensors, ancillary chips, FPC, cooling) and will be fully tested in the UK
    - We participate in all aspects of the project
  - The UK project is shared among several UK institutions
- However, the project is US driven, and we rely on them providing critical infrastructure
  - And we rely on the ALICE collaboration for design of and access to the MOSAIX chip
  - These exposures are out biggest project risks
- The other big challenge will be competing demands from LHC upgrades