Science and Technology Facilities Council

Sensor and AncASIC Updates

Introduction

Introduction

- Background and Overview

MOSAIX

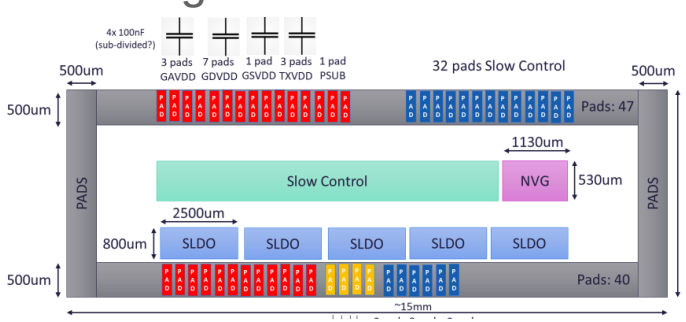
- Overview of MOSAIX
- Progress

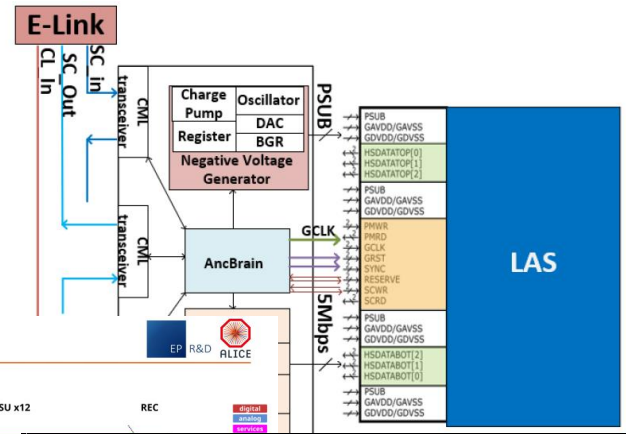
EIC-LAS

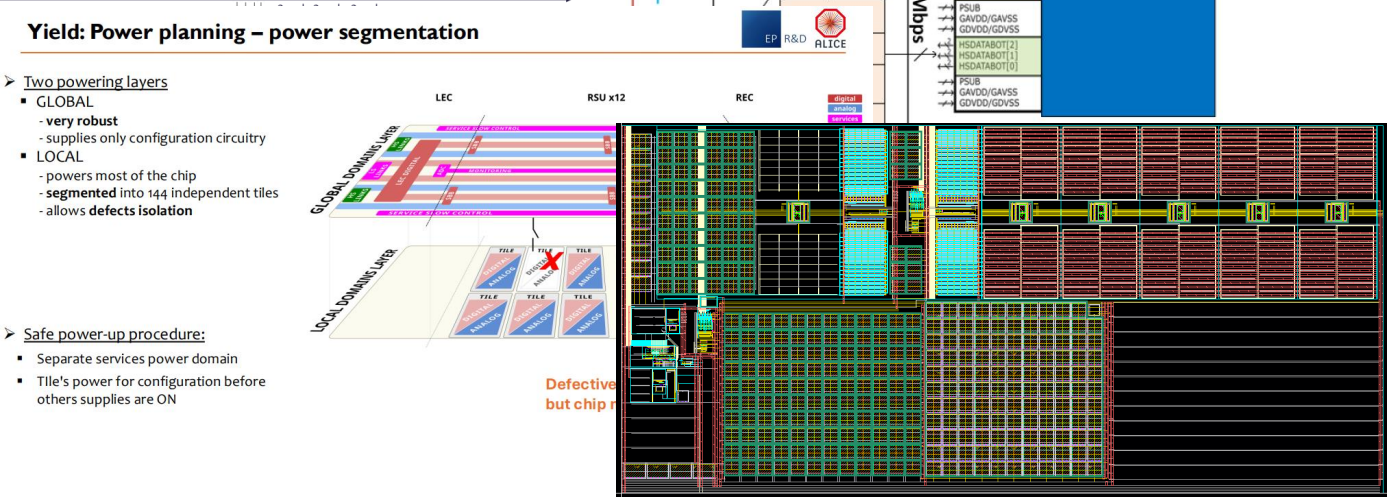
- Changes to MOSAIX
- Assist with Stave Design
- Progress

AncASIC

- Background and Features
- NVG
- SLDO
- Size and Pads
- Progress

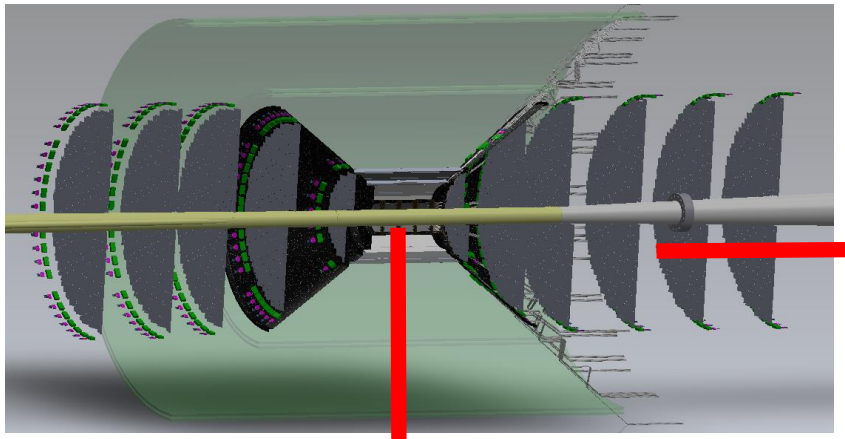




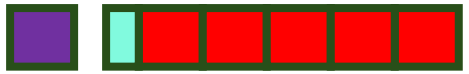


Science and Technology Facilities Council

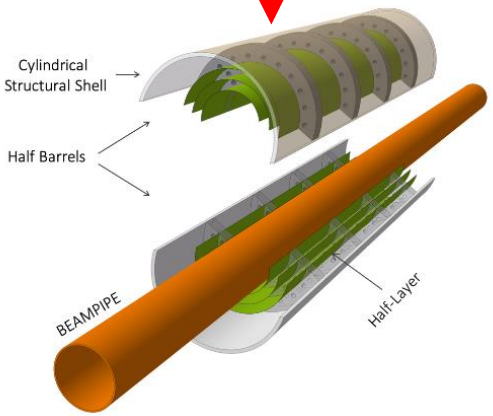
Introduction



Outer Barrel and Discs



- Smaller Verion of MOSAIX with minimal changes (EIC-LAS)
- Supporting AncASIC



Inner Barrel

- Thinned silicon bent around beampipe
- USE MOSAIX from ITS3

Science and Technology Facilities Council

Introduction

Three strands

- Partner with ITS3 for MOSAIX access
- Develop EIC-LAS based on MOSAIX
- Develop AncASIC to support EIC-LAS

	Requirement for ePIC	Work currently under way	Institutes involved
ITS3 Partnership (WBS 1.1)	Partner with ITS3	LLDFM logic cells Cross-RSU data transmission VFM ADC SRAM Digital design – RSU serialiser	RAL, LBNL BNL BNL MIT
EIC-LAS (TPSCo 65nm) (WBS 1.2)	Reduced number of RSUs	N/A – requires database	????
	Multiplexing to single data link	N/A – requires database	????
	TX Voltage reduction for SP	N/A – requires database	????
Ancillary Chip (XFAB 110nm) (WBS 1.3/4/5/6)	Multiplexed slow control	Definition	BNL
	Serial powering	110nm schematic complete	RAL/Oxford/LBNL
	Negative bias generation	First layout complete	BNL

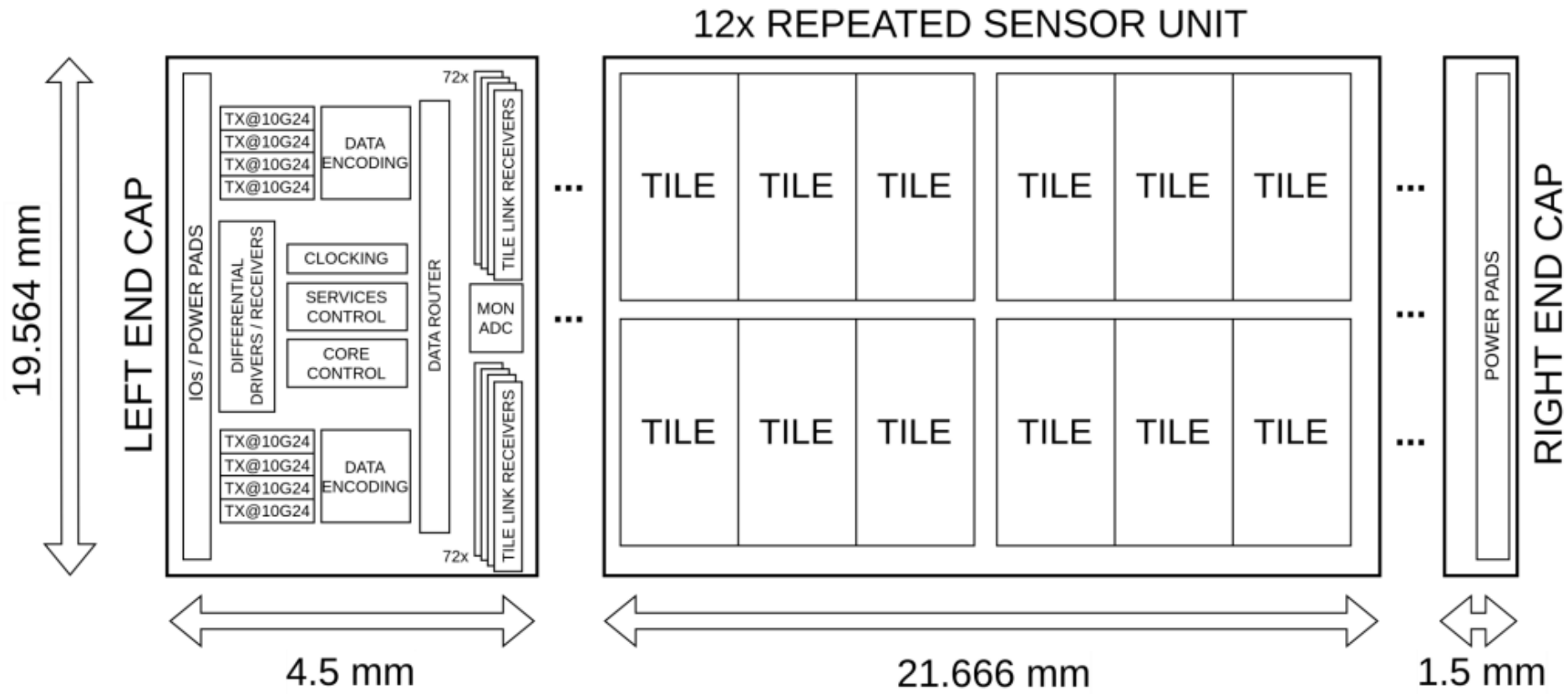
Science and Technology Facilities Council

Science and Technology Facilities Council

MOSAIX

Science and Technology Facilities Council

MOSAIX Overview



Science and Technology Facilities Council

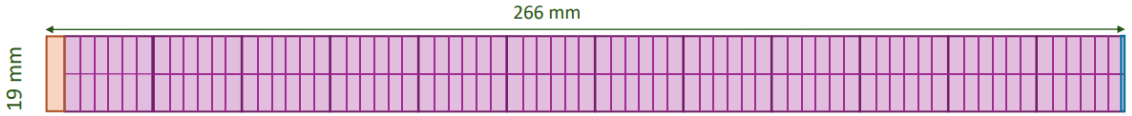
MOSAIX Progress

Progress

- ER1 has been taped out and is in testing
  - Development of a Stitched Monolithic Pixel Sensor prototype (MOSS chip) towards the ITS3 upgrade of the ALICE Inner Tracking System
  - The Monolithic Stitched Sensor (MOSS) Prototype for the ALICE ITS3 and First Test Results
  - Yield Characterisation and Failure Analysis of the Monolithic Stitched Sensor MOSS for ALICE ITS3
  - Evaluation of efficiency, radiation hardness, and timing performance of the Analogue Pixel Test Structure for ALICE ITS3
- ER2 (the first MOSAIX chip) is currently being finalised. Tapeout Q4 23/Q1 24
  - Development of the MOSAIX Chip for the ALICE ITS3 Upgrade
  - Power Distribution over the Wafer-Scale Monolithic Pixel Detector

MOSAIX Progress

MOSAIX is the full size, fully functional, stitched sensor prototype for the ITS3



93 % sensitive region
0.7 % sensor area modularity
144 tiles (independent units)

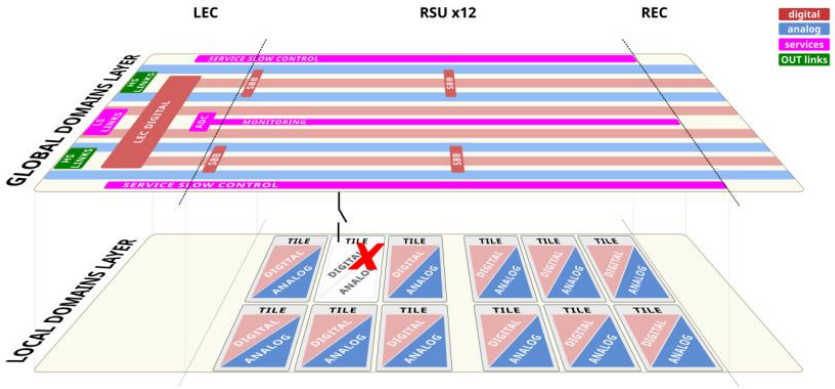
10^{13} NIEL (1 MeV neq cm^{-2})
10 kGray TID
Triple modular redundancy

4.4 MHz/cm^2 particle rate
30.72 Gb/s off-chip data transmission
minimum 2 µs integration time
< 40 mW/cm^2

20.8 x 22.8 µm^2 pixel size
Detection Efficiency > 99 %
Fakehit rate < 0.1 $pixel^{-1}s^{-1}$

Yield: Power planning – power segmentation

- Two powering layers
  - GLOBAL
    - **very robust**
    - supplies only configuration circuitry
  - LOCAL
    - powers most of the chip
    - **segmented** into 144 independent tiles
    - allows **defects isolation**



- Safe power-up procedure:
  - Separate services power domain
  - TIle's power for configuration before others supplies are ON

Defective tile adds 0.7% of dead area, but chip maintains functional!

6

Science and Technology Facilities Council

Key Physics/Engineering Interface Question:

- **How many tiles can we lose?**

Science and Technology Facilities Council

EIC-LAS

Science and Technology Facilities Council

EIC-LAS

Changes to MOSAIX

- To reduce risk, we try and limit ourselves to three changes from MOSAIX to LAS:
  - Reduce number of RSUs
  - Edit data multiplexer to put everything on one link
  - Alter serialiser power scheme to match serial powering

EIC-LAS (TPSCo 65nm) (WBS 1.2)	Reduced number of RSUs	N/A – requires database	????
	Multiplexing to single data link	N/A – requires database	????
	TX Voltage reduction for SP	N/A – requires database	????

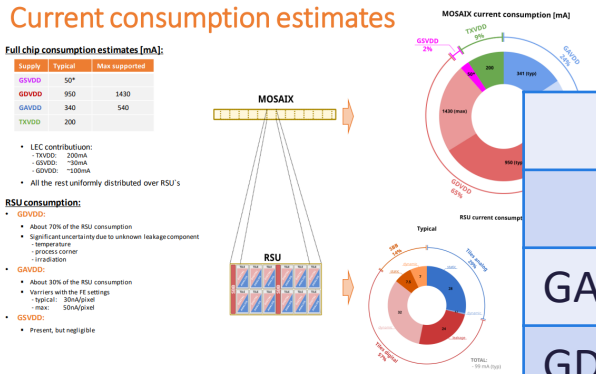
Science and Technology Facilities Council

Requires DOE-CERN agreement – currently in negotiation

EIC-LAS

Assist with Stave Design

- In spite of challenges, need to provide some numbers (esp. power) to allow AncASIC and stave design
- Make some assumptions based on available data:
  - Latest MOSAIX Power numbers
  - Assume 6 RSU LAS
  - Numbers in red do not have “Max” estimates in the previous slide, so assumed +50% on typ number (since this is true for supplies that do have it)
  - EIC-LAS is one LEC and 6 RSU



	Voltage(V)	Typ Current Consumption (mA)			Max Current Consumption (mA)		
		RSU	LEC	EIC-LAS	RSU	LEC	EIC-LAS
GAVDD	1.32	28		168	45		270
GDVDD	1.32	71	100	526	111	150	816
GSVDD	1.32	1.6	30	40	2.4	45	59.4
TXVDD	1.2		200	200		300	300
Total				934			1445

Science and Technology Facilities Council

EIC-LAS Progress

Progress

- What we want to do is clear
- Further understanding (esp. of the LEC) is needed to determine how to handle link reduction
- Making any changes to the MOSAIX design other than stitching plan changes requires database access. Currently in negotiation at DOE-CERN level
- Fallback options could exist in case this is not forthcoming or we have timeline/risk/effort issues:
  - Settle for non-optimal numbers of links
  - Different scheme to power serialiser

Science and Technology Facilities Council

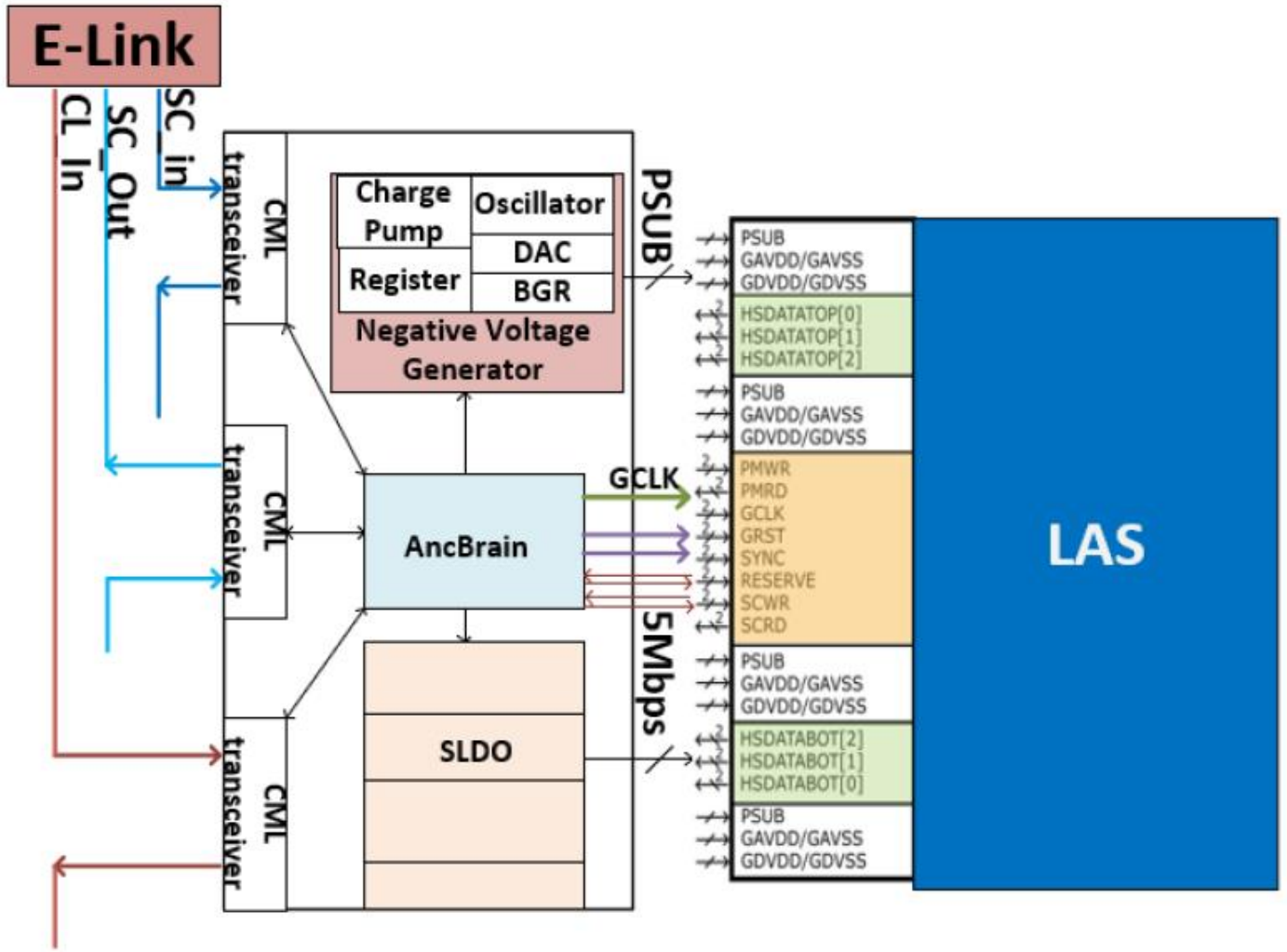
Ancillary ASIC

Science and Technology Facilities Council

Ancillary ASIC

Background

- Some features of EIC-LAS not amenable to stave operation:
  - Point-to-point slow control
  - Point-to-point powering
- Adding these to the EIC-LAS/MOSAIX design is high risk, complex and perhaps technically unfeasible
- Develop supporting ASIC instead

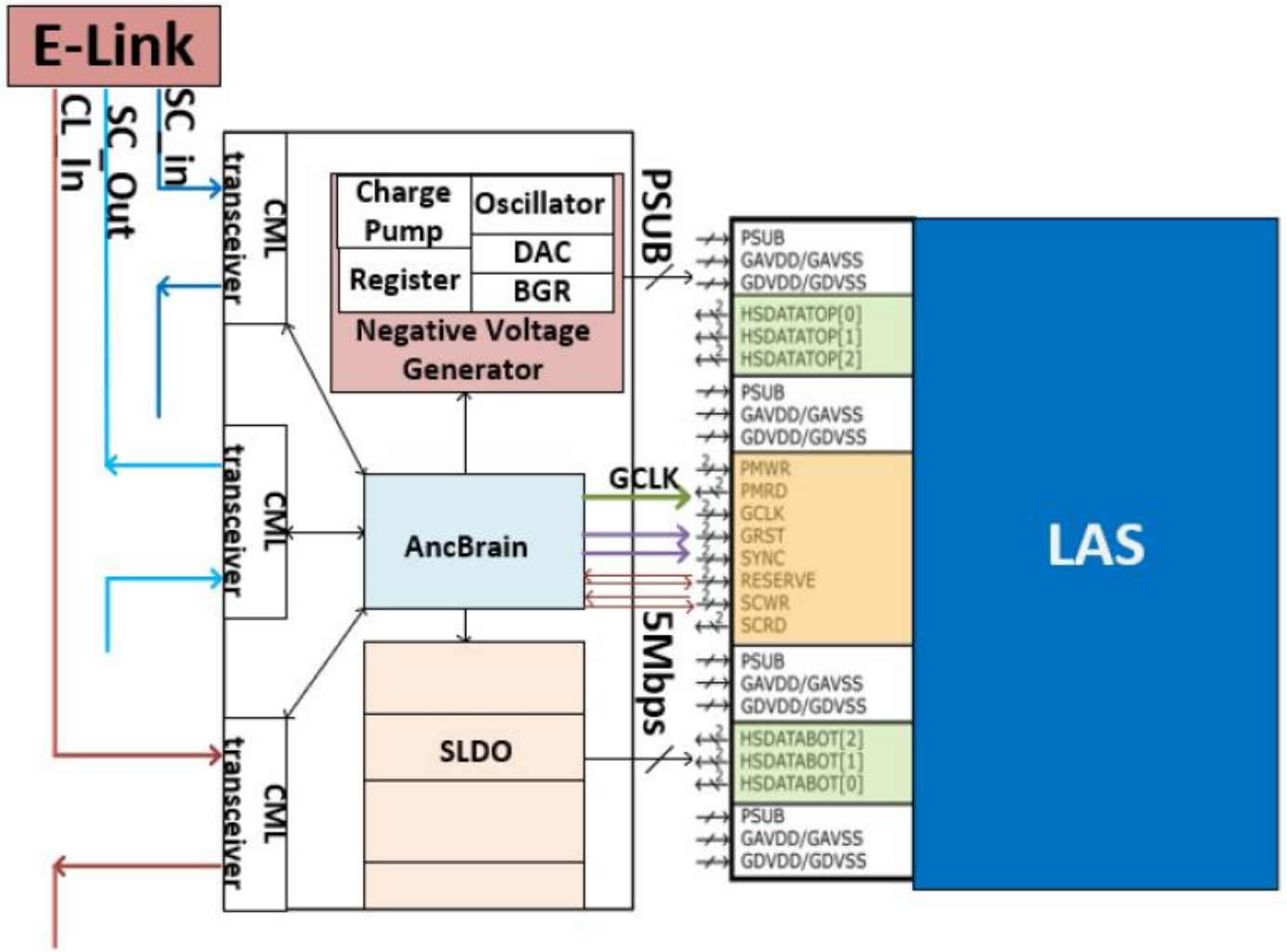


Science and Technology Facilities Council

Ancillary ASIC

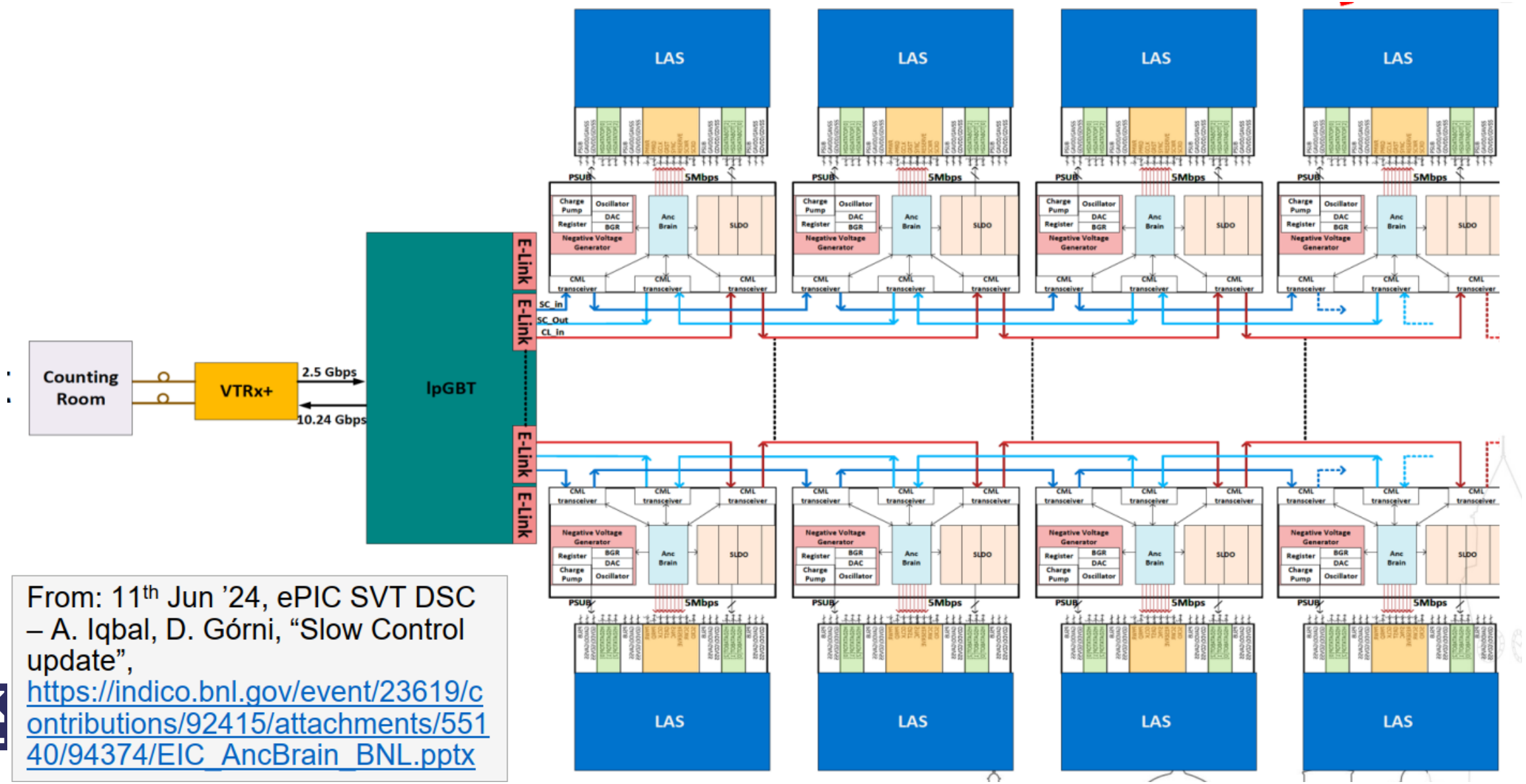
Features

- Shunt-LDO (SLDO)
  - For serial powering
  - 5 per AncASIC (4 EIC-LAS supplies and AncASIC)
- Negative Voltage Generator (NVG)
  - MOSAIX/EIC-LAS need small negative back bias
- AncBrain
  - Slow Control Multiplexing
  - Control of rest of AncASIC



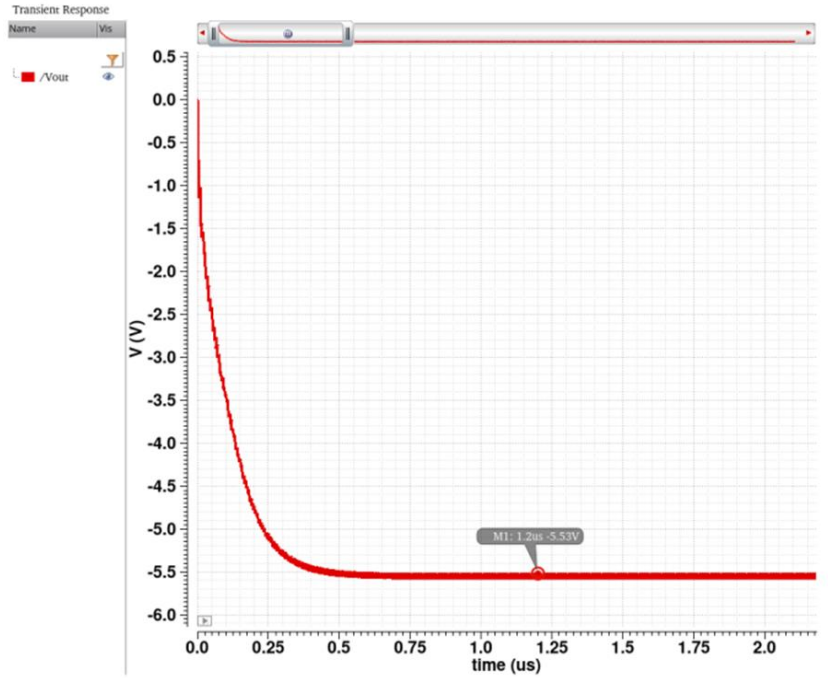
Science and Technology Facilities Council

Ancillary ASIC Stave



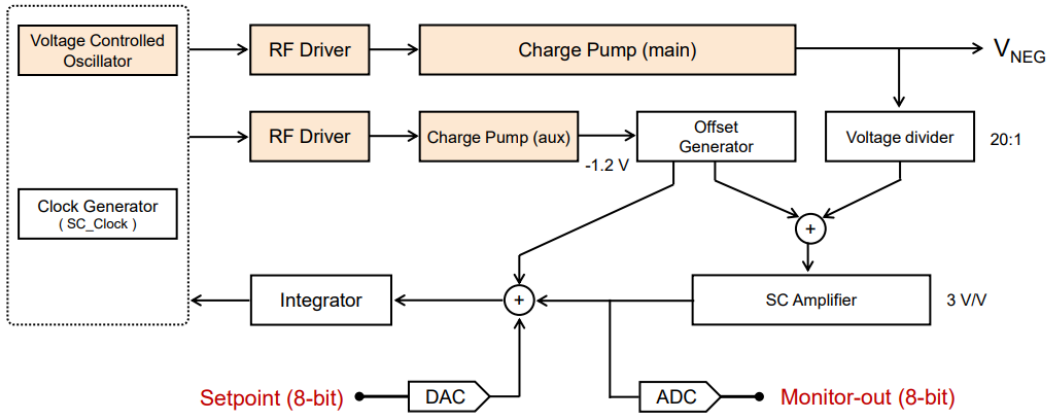
From: 11th Jun '24, ePIC SVT DSC – A. Iqbal, D. Górni, "Slow Control update", https://indico.bnl.gov/event/23619/contributions/92415/attachments/55140/94374/EIC_AncBrain_BNL.pptx

Negative Voltage Generator



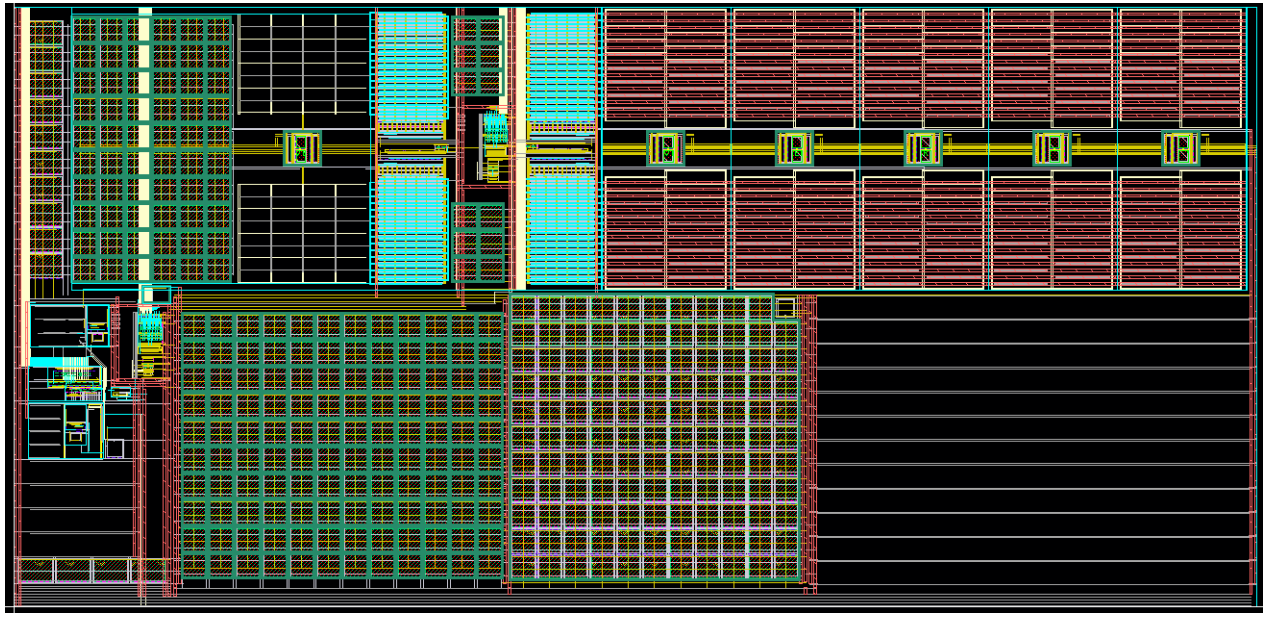
Negative Voltage Generator (NVG)

(with feedback control)



Brookhaven National Laboratory

Blocks planned for September 2024 fabrication run

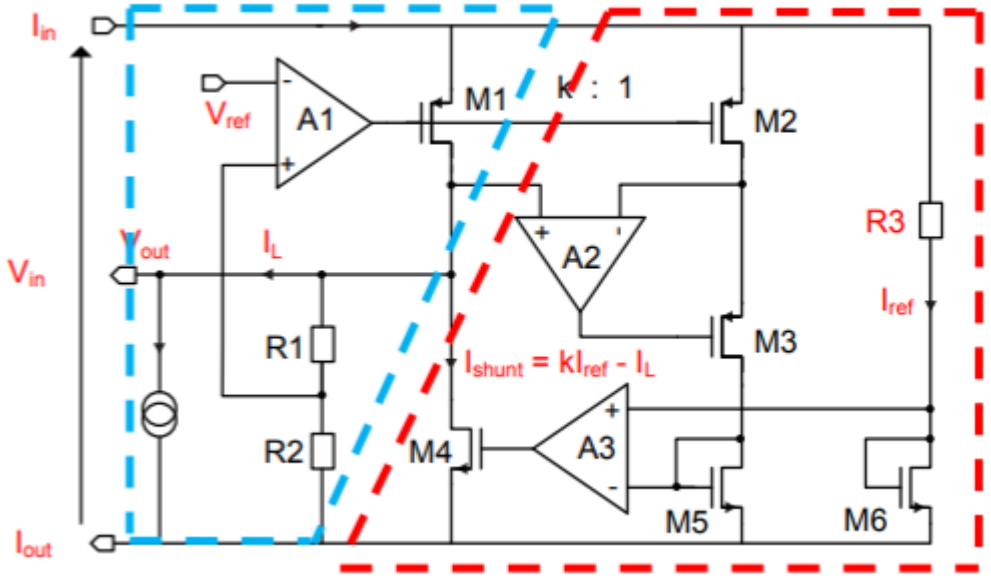


Science and Technology Facilities Council

SLDO

What is an SLDO?

- The Shunt-LDO (SLDO) is a combination of a **Low Drop Out (LDO) regulator** and a **Shunt Regulator**.
- The LDO loop keeps the output voltage constant and the shunt loop ensures the correct corresponding load current is supplied.
- The LDO loop keeps Vout constant by dropping the difference between the desired output voltage and the input voltage across a pass transistor.
- The shunt regulator loop makes sure the same current is always drawn by the SLDO by shunting the difference between the load and input current.
- The SLDO has an ohmic IV characteristic.



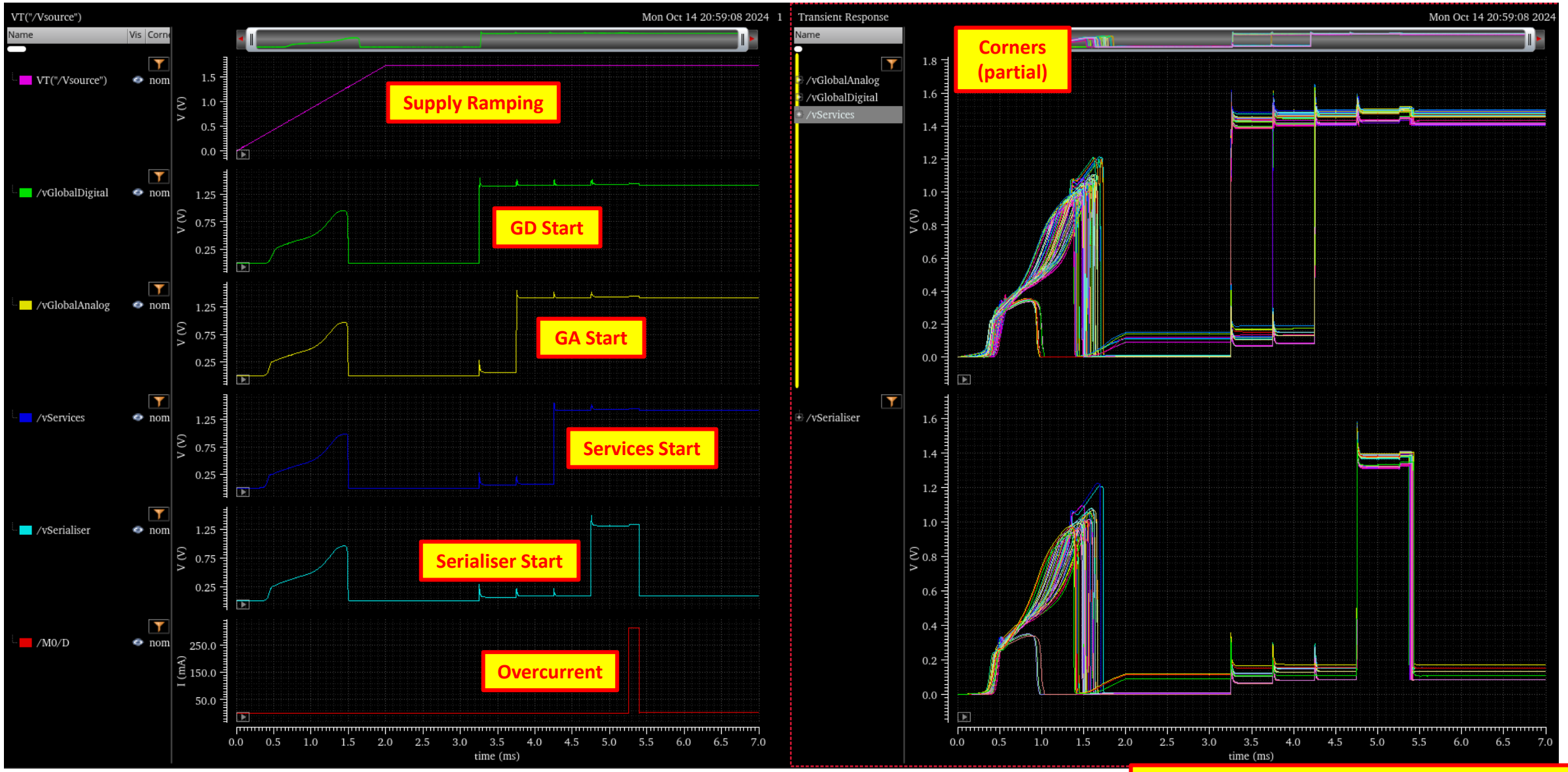
$$I_{in} \approx kI_{ref} \approx k\frac{V_{in} - V_{thM6}}{R3}$$

$$R_{in} \approx \frac{V_{in}}{I_{in}} \approx \frac{R3}{k}.$$

[1]

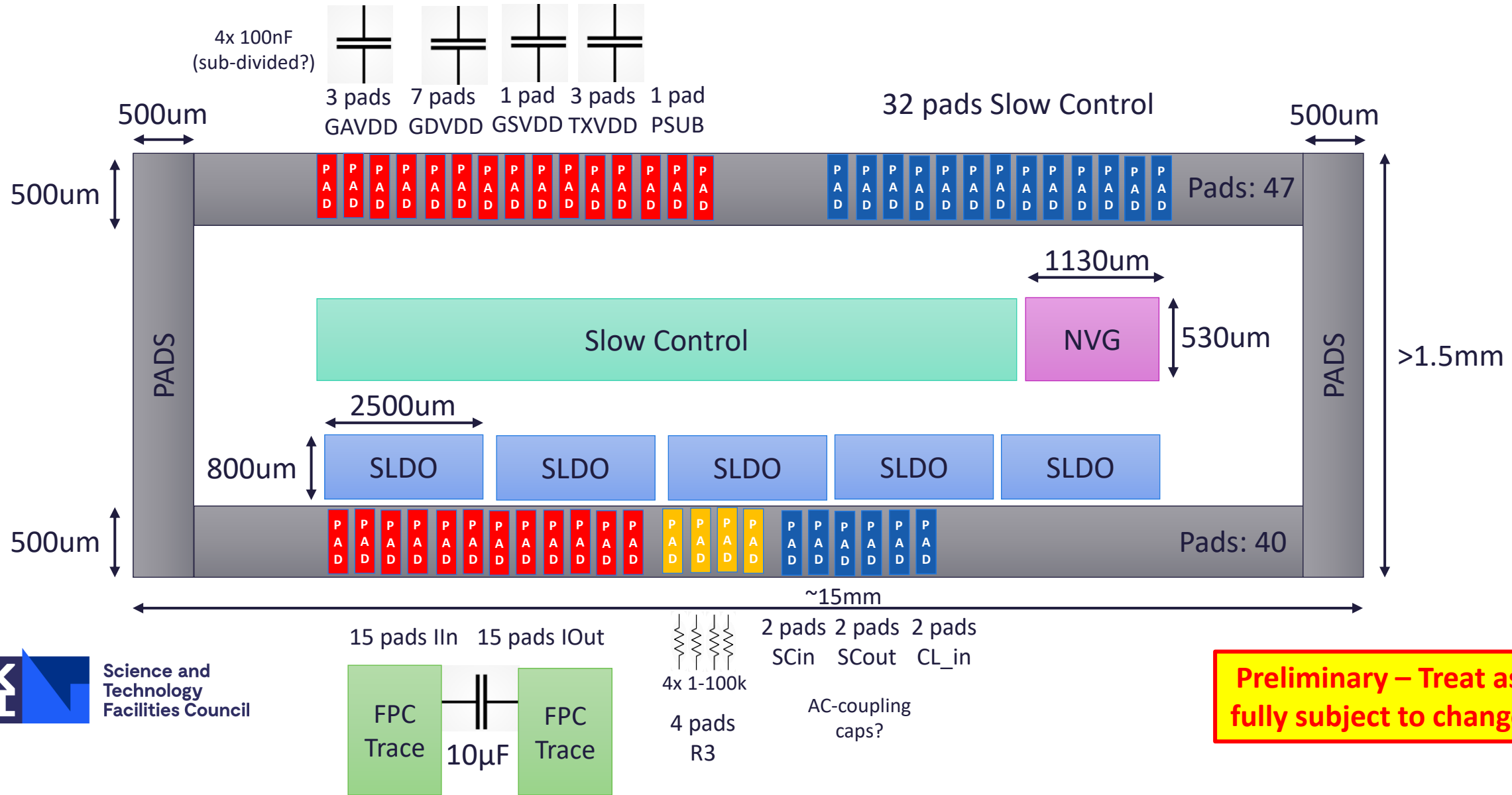
Science and Technology Facilities Council

SLDO



MODE 0 – overcurrent on serialiser

AncASIC Size and Pads



Science and Technology Facilities Council

Preliminary – Treat as fully subject to change

AncASIC Progress

Transistor Test Structures

- Complete
- Planned for November Submission

Negative Voltage Generator

- First version complete
- Planned for November Submission
- More Detail

Shunt LDO

- Schematically Complete
- Layout underway
- Pre-reg complete and planned for November Submission
- More Detail

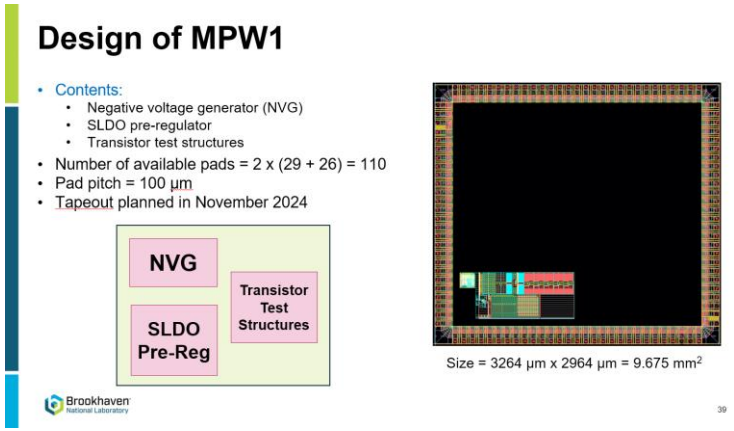
AncBrain

- Scoping
- FPGA Emulator Planned

Science and Technology Facilities Council

Towards higher level design

- Much AncASIC work so far focussed on providing information to higher level designs:
  - Stave Power Consumption
  - Cooling
  - FPC Design
- But be aware all the underlying numbers are still subject to change!



AncASIC assembly requires DSA
November Submission at risk due to procurement issues

Conclusion

MOSAIX

- Watching brief
- Waiting for DOE-CERN Agreement
- Starting to think about resource allocation

Negative Voltage Generator

- Well advanced, first layout ready

AncBrain

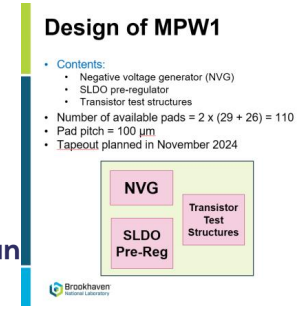
- Scoping
- Hopefully funding for BNL emulator this FY

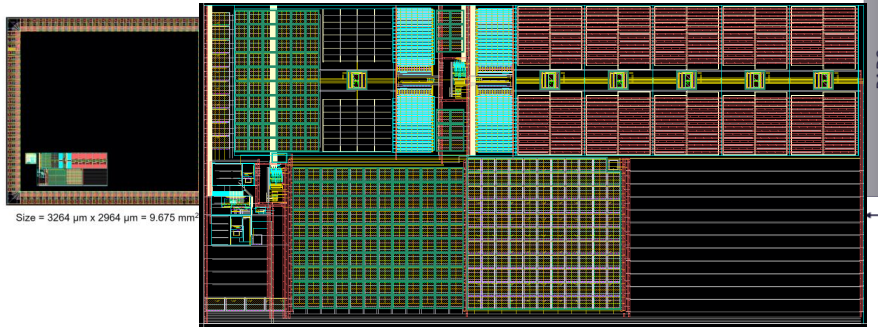
Shunt LDO

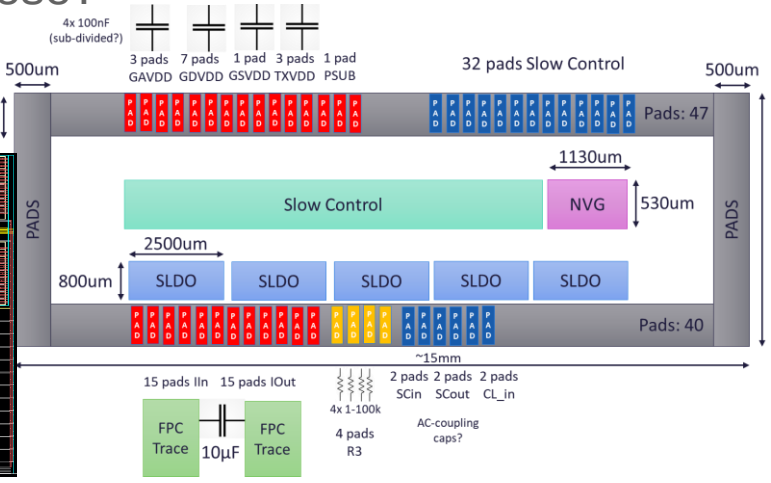
- Well advanced, first layout in preparation

Overall

- Good technical progress
- A number of legal and administrative concerns:
  - DOE-CERN Agreement
  - Design Share Agreement
  - Procurement Issues
- Do we need to be thinking about mitigations for some of these?







Science and
Technology
Facilities Council

Questions?

Science and
Technology
Facilities Council

Backup

MOSAIX Supply Complexities

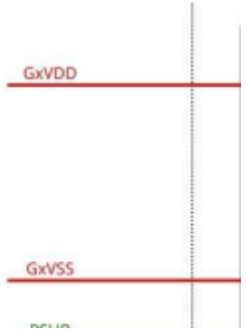
GA, GD and Services

- Remaining voltages are all driven at 1.32V
- It is necessary that services should always be above the other two, but this is handled internally by assuming that only GA and GD droop.
- Therefore we assume GA, GD and Services at 1.32V.

Tile power switches

Operating conditions:

- Supplies:
  - GSVDD: 1.2 -- 1.32 V (nominal 1.32V)
    - * have to be larger than GAVDD and GDVDD
    - * no significant supply drops [<20mV] (DC and transient)
  - PSUB: 0 --- 2 V
  - GAVDD: 0 -- 1.3 V
  - GDVDD: 0 -- 1.3 V
- Nominal tile currents:



Testing MOSAIX with AncASIC

- James suggested it would be useful to be able to test the AncASIC powering MOSAIX when ER2 returns
- Ran some simulations to check if it is possible
- Seems that it is (for the Expected 25 case) because designing for Max45 EIC-LAS leaves a lot of headroom

Science and Technology Facilities Council

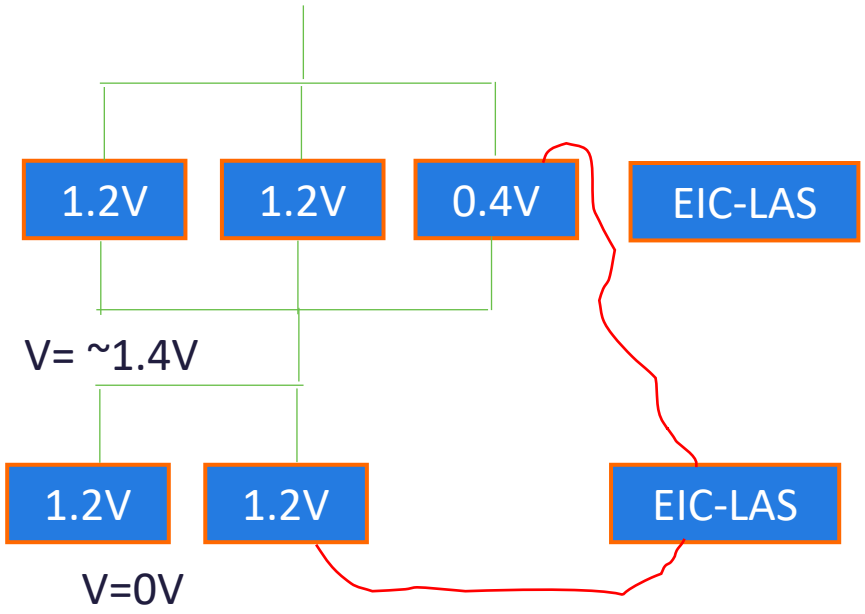
MOSAIX Supply Complexities…

The 1.8V Problem…

- MOSAIX requires not just a 1.2V supply, but also 1.8V to run the serialisers
- The AncASIC itself will need a 1.8V supply for logic and the NVG
- However, all SLDOs need to be in parallel, and if we run them at 1.8V, the 1.2V supplies will waste considerable power

What can we do?

- Run the SLDOs at 1.8V Considerable waste of power - ~1.1W
- Two serial powering chains Impossible – shared ground at various points
- Use the NVG? Could it step 1.2V up to 1.8V? Noise issues?
- Tap power from the next stage? Routing complexity. Stability? Still a power waste - ~300mW. What about the last one?
- Remove serialiser LDO from 65nm IP (serialiser itself is 1.2V)
- Supply 1.8V externally to each LAS Would need 8 lines (supply and return for each of 4 LAS).



Science and Technology Facilities Council

MOSAIX Supply Complexities…

The 1.8V Solution?

- João's idea to edit the 65nm database to skip the LDO seems like a good one.
- We do not yet have a solution to powering the AncASIC circuits that run at 1.8V.
- It does seem that the serialiser could be separated from it's LDO

https://indico.cern.ch/event/1376523/contributions/5785064/attachments/2789901/4865135/ALPIDE_65_30_01_2024.pdf

- So for the rest of this presentation, I will assume that the serialiser can be powered at 1.2V in order to get an overall power number.
- We should perhaps suggest to the higher SVT that they think about point-to-point powering of the 1.8V system just in case (would mean 8 extra wires)

LAS Power Consumption – Earlier Estimates

		Power Consumption		
	Unit	5 RSU LAS	6 RSU LAS	MOSAIX
LEC	mW	696	696	696
RSUs	mW	543	651	1303
Total	mW	1240	1348	2000

Expected 25

		Power Consumption		
	Unit	5 RSU LAS	6 RSU LAS	MOSAIX
LEC	mW	696	696	696
RSUs	mW	889	1066	2133
Total	mW	1585	1763	2829

Max 25

		Power Consumption		
	Unit	5 RSU LAS	6 RSU LAS	MOSAIX
LEC	mW	696	696	696
RSUs	mW	1280	1536	3072
Total	mW	1976	2235	3768

Max 45

2 published sources of data (power densities, and supply current breakdown)

LEC does not vary at all in the power density figures

Separation into supplies does not include Expected/Max variation

How to reconcile?

Supply purpose	Nets	Voltage [V]	Current [mA]	Pads on LEC	Pads on REC
Services	SDVDD-SDVSS	1.2 to 1.32	227	Yes	Yes
Global analog	GAVDD-GAVSS	1.2 to 1.32	540	Yes	Yes
Global digital	GDVDD-GDVSS	1.2 to 1.32	1369	Yes	Yes
Serializers	TXVDD-TXVSS	1.8	200	Yes	No
Substrate bias	PSUB	−1.2 to 0			

Science and Technology Facilities Council

LAS Power Consumption – Earlier Estimates

Towards individual supply estimates

N.B. We can make better case assumptions if we like, but we should do it consciously

- Can only really make worst case assumptions:
  1. 6 RSU LAS
  2. Expected 25 to Max 45 is 65% variation.
  3. Apply this also to the LEC and assume published number is Expected 25.
  4. Worst case numbers are then 1536mW for the RSUs and 1148mW for the LEC.
  5. Total 2684mW

- How does this compare to the published supply numbers (MOSAIX – 12RSU)?

Supply purpose	Nets	Voltage [V]	Current [mA]	Pads on LEC	Pads on REC
Services	SDVDD-SDVSS	1.2 to 1.32	227	Yes	Yes
Global analog	GAVDD-GAVSS	1.2 to 1.32	540	Yes	Yes
Global digital	GDVDD-GDVSS	1.2 to 1.32	1369	Yes	Yes
Serializers	TXVDD-TXVSS	1.8	200	Yes	No
Substrate bias	PSUB	−1.2 to 0			

	Scale to EIC-LAS ->	+65% ->
272mW	272mW	449mW
648mW	270mW	445mW
1643mW	821mW	1354mW
360 mW	360 mW	594 mW
XXXXXX	XXXXXX	XXXXXXX
Total: 2923mW	1723mW	2842mW

Good match to our worst case Max45 estimate, so can probably assume the original numbers are for the Expected 25 case

Science and Technology Facilities Council

LAS Power Consumption – Earlier Estimates

LAS, Best and Worst

- Knowing the EIC-LAS current requirements is key for the SLDO design
- Since the SLDO dominates the AncASIC (we need a better name…) power consumption, it is also key to get a power number for that chip
- Current numbers needed for simulation

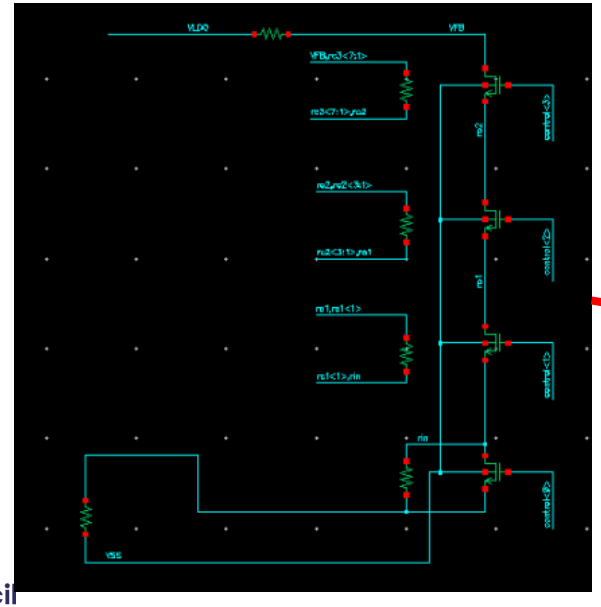
	Power		Voltage	Current	
	Expected 25	Max 45		Expected 25	Max 45
Services	272mW	449 mW	1.32V	206 mA	340 mA
Global Analog	270mW	445 mW	1.32V	205 mA	337 mA
Global Digital	821mW	1354 mW	1.32V	622 mA	1026 mA
Serialisers	360 mW	594 mW	1.2V	300 mA	495 mA

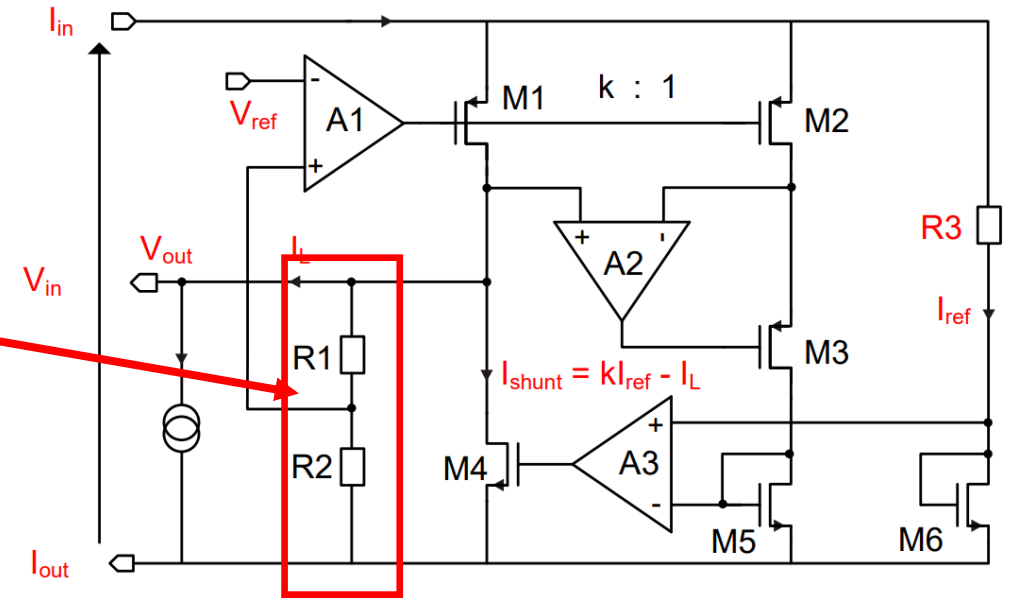
Assume 1.2V for serialisers (if we can skip the on-chip LDO)

Ancillary Chip Adjustability

Programmable Output Voltage

- Compared to earlier presentations (v7 and before), need to simulate case where GA=GD=Services=1.32V and Serialiser=1.2V. Requires adjustable SLDO output.
- Since we also want some control over SLDO output to allow adjustment in real world, prefer to implement real circuit.
- Implemented variable resistor (4bit) to allow this. Should give swing between 1.1 – 1.5V





Science and Technology Facilities Council

Science and Technology Facilities Council

AncASIC Power Consumption

Science and Technology Facilities Council

Towards Increased Realism

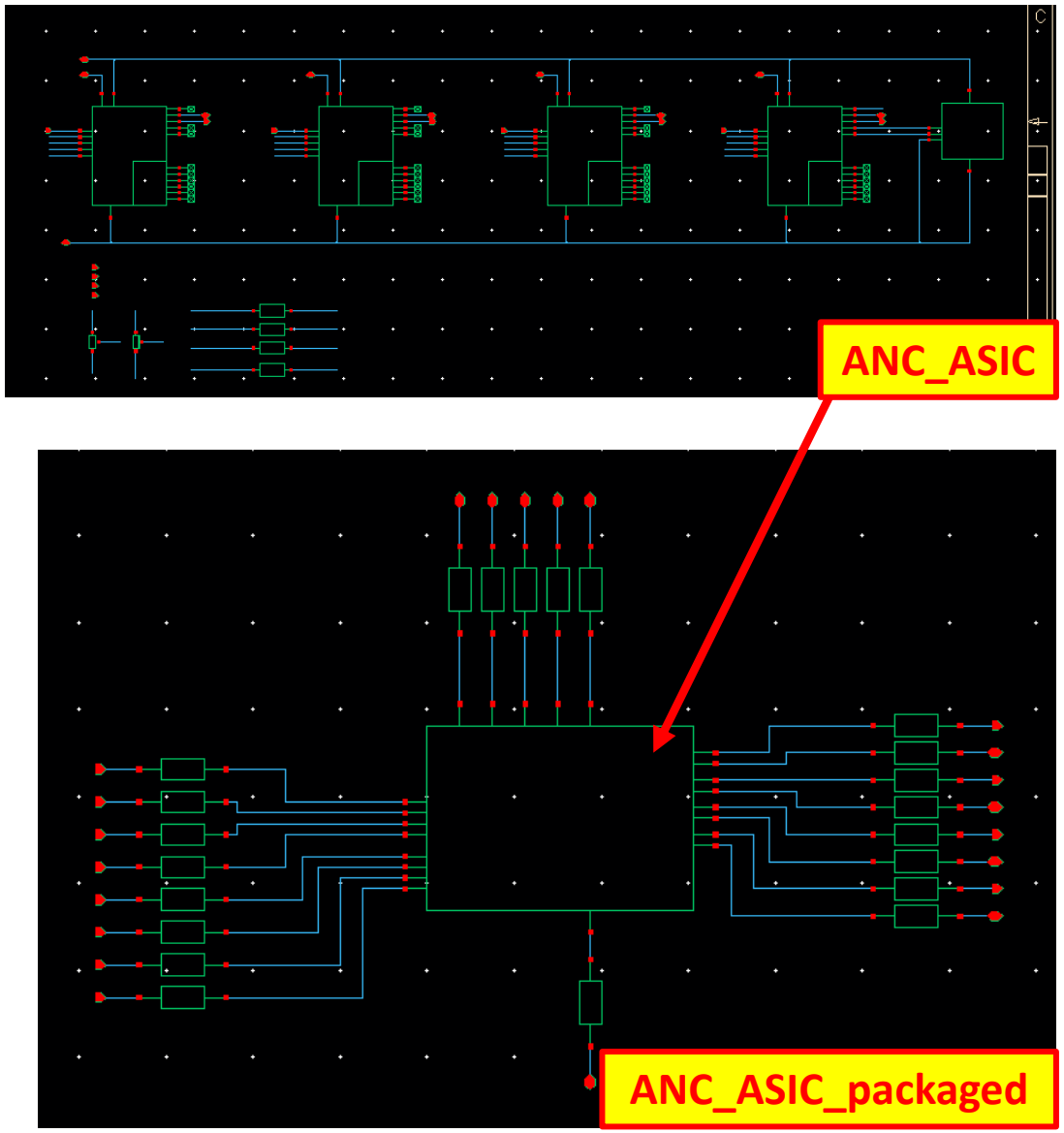
Build an "AncASIC"

- 4x SLDO plus OVP
- No NVG, slow control, AncASIC SLDO

AncASIC Packaging

- Determine number of pads per supply based on EM limits
- Assume Max condition and 20% shunt overhead
- Iout must equal Iin to cover case where all current is shunted
- **N.B. These are only the supply pads**. Does not includes controls, NVG, Slow Control etc.

Supply	Current (mA)	Pads Required
Iin/Iout	1734	15/15
GAVDD	270	3
GDVDD	816	7
Services	59.4	1
Serialiser	300	3



Science and Technology Facilities Council

MOSAIX Power Consumption

MOSAIX Engineering Specification Review

- Current consumption numbers for MOSAIX were updated in the engineering review.

Current consumption estimates

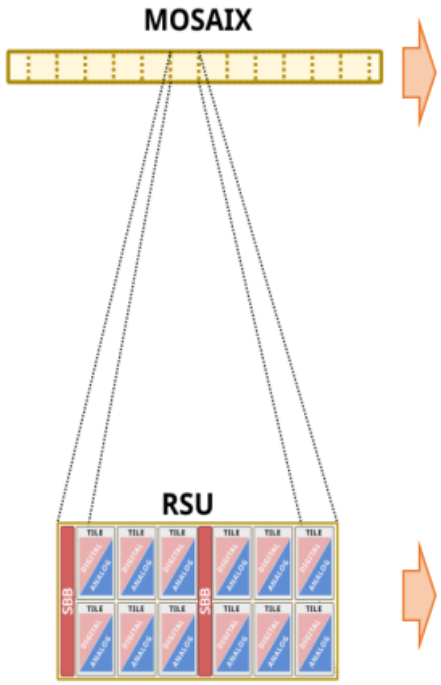
Full chip consumption estimates [mA]:

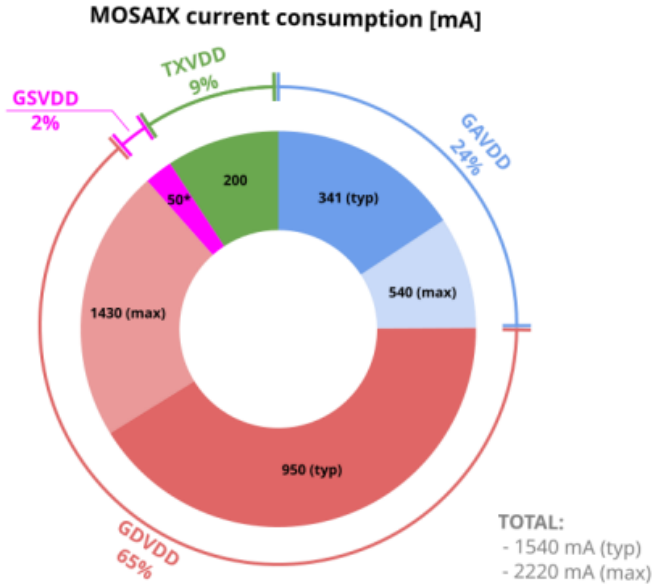
Supply	Typical	Max supported
GSVDD	50*	
GDVDD	950	1430
GAVDD	340	540
TXVDD	200	

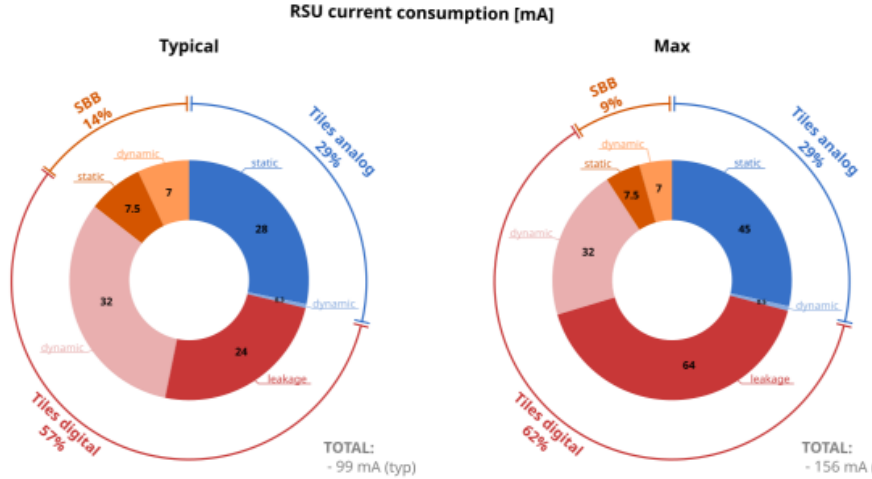
- LEC contributiuon:
  - TXVDD: 200mA
  - GSVDD: ~30mA
  - GDVDD: ~100mA
- All the rest uniformly distributed over RSU`s

RSU consumption:

- GDVDD:
  - About 70% of the RSU consumption
  - Significant uncertainty due to unknown leakage component
    - temperature
    - process corner
    - irradiation
- GAVDD:
  - About 30% of the RSU consumption
  - Varriers with the FE settings
    - typical: 30nA/pixel
    - max: 50nA/pixel
- GSVDD:
  - Present, but negligible







Science and Technology Facilities Coun

Towards Increased Realism

FPC Trace Resistance

- Using input and output trace resistance provided by Marcello – 94.6mOhm

Decoupling

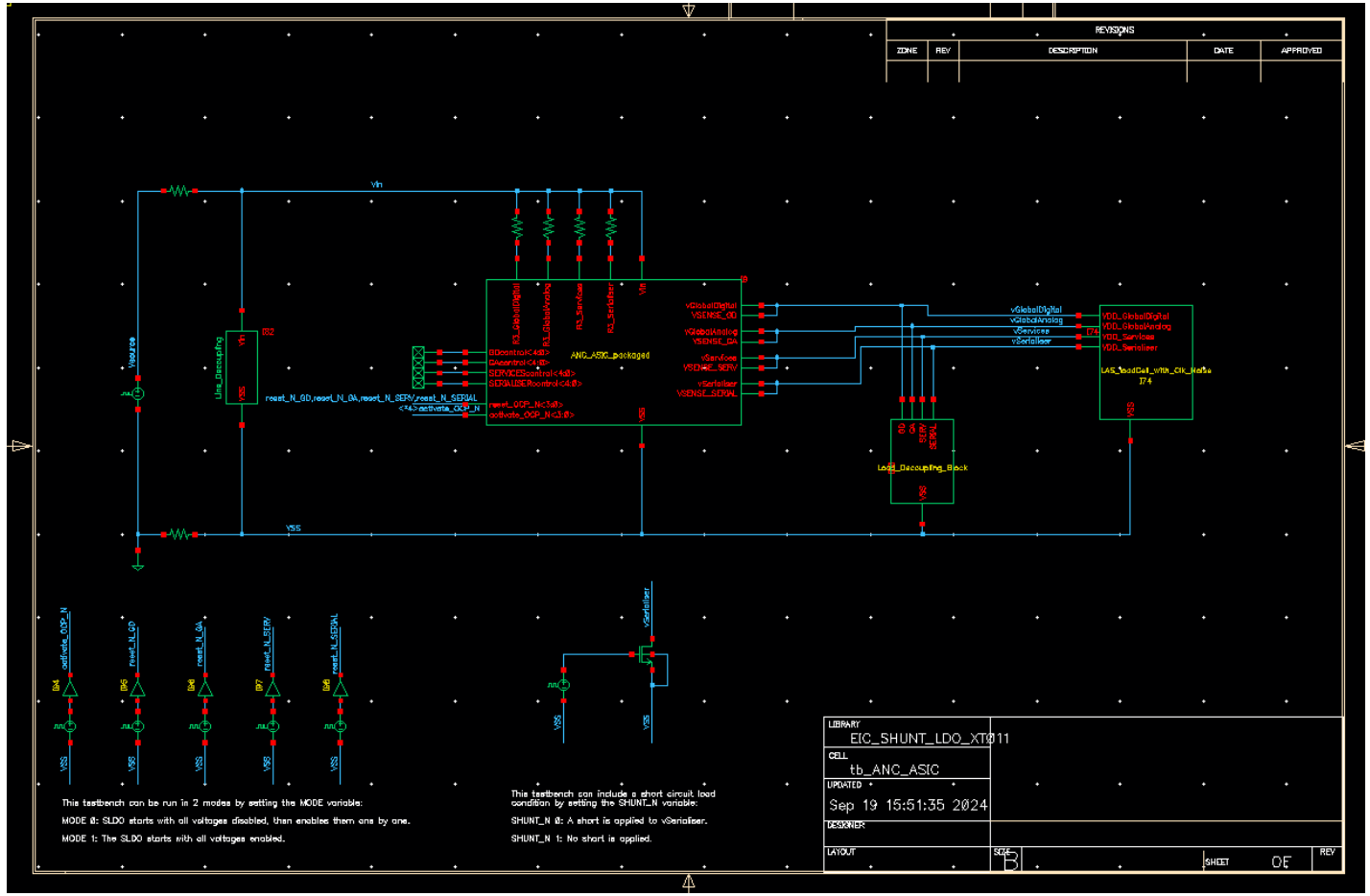
- 10uF Line Decoupling
- 100nf Load Decoupling

MOSAIX Loads

- Unknown, so using:
  - capSerialiser – 10nF
  - capServices – 100nF
  - capGlobalAnalog – 1uF
  - capGlobalDigital – 10uF

R3 Values

- Ideal (no tolerance or E series)
- Tolerance and non-ideal value will reduce power efficiency



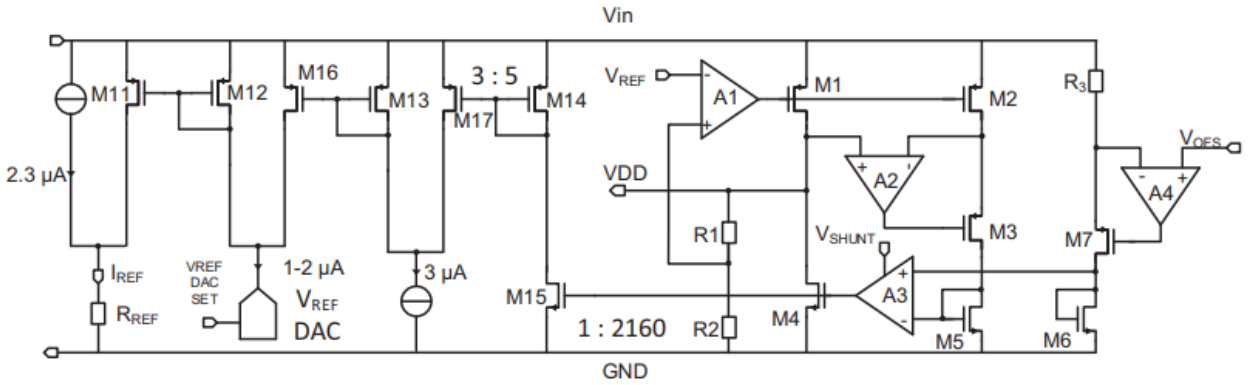
Science and Technology Facilities Council

Overcurrent Protection

Over-current protection

- Change from that described in this paper
  - Detect under-shunt condition
  - Voltage limit by output voltage reduction
  - Still some short circuit current

- Use more traditional LDO overcurrent protection
  - Detect under-shunt condition
  - Short pass transistor
  - Effectively make output high impedance, and shunt behaves like an open circuit
  - Some transient immunity

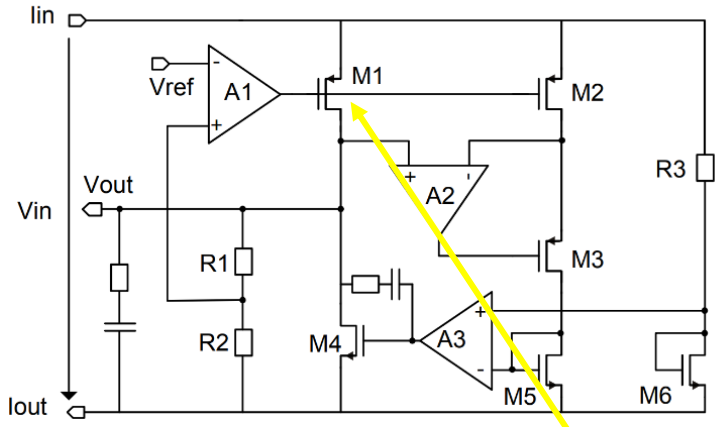


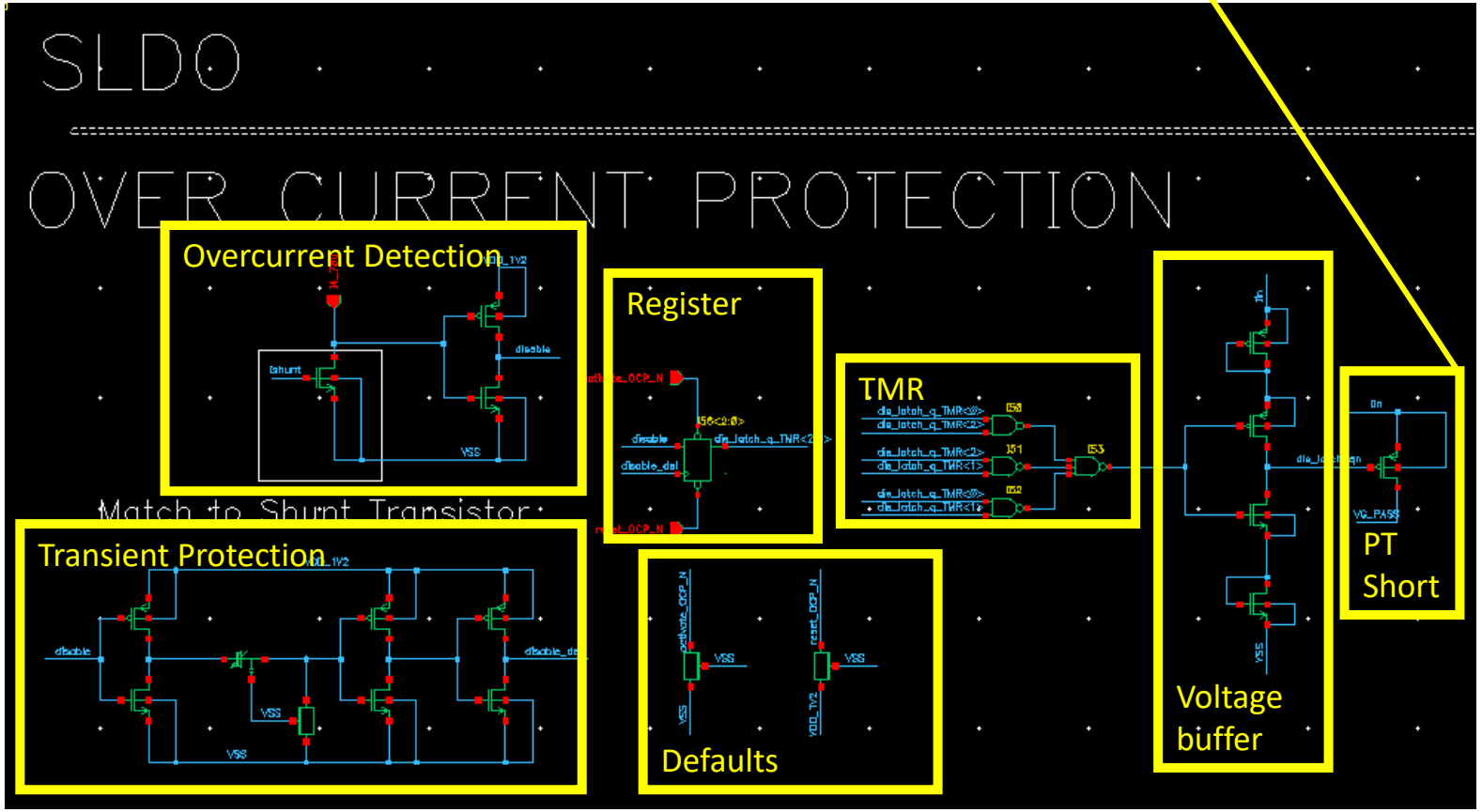
Science and Technology Facilities Council

Overcurrent Protection

Over-current protection

- Use more traditional LDO overcurrent protection
  - Detect under-shunt condition
  - Short pass transistor
  - Effectively make output high impedance, and shunt behaves like an open circuit
  - Some transient immunity
  - Locks into overcurrent state until reset
  - TMR protection
  - Pull-ups for default operation



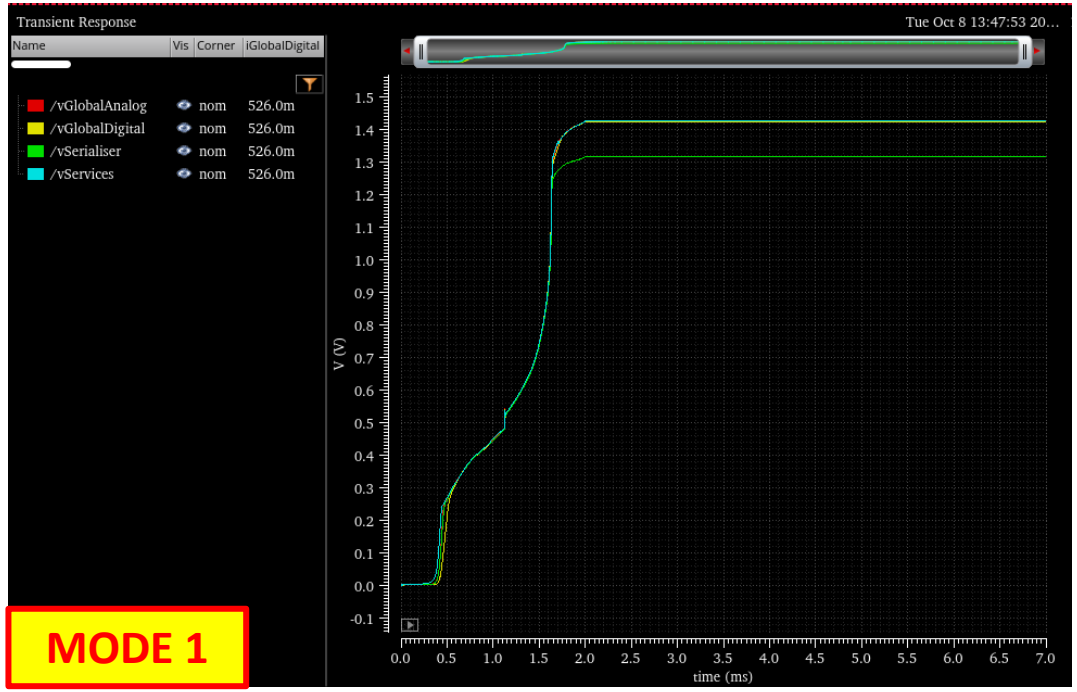


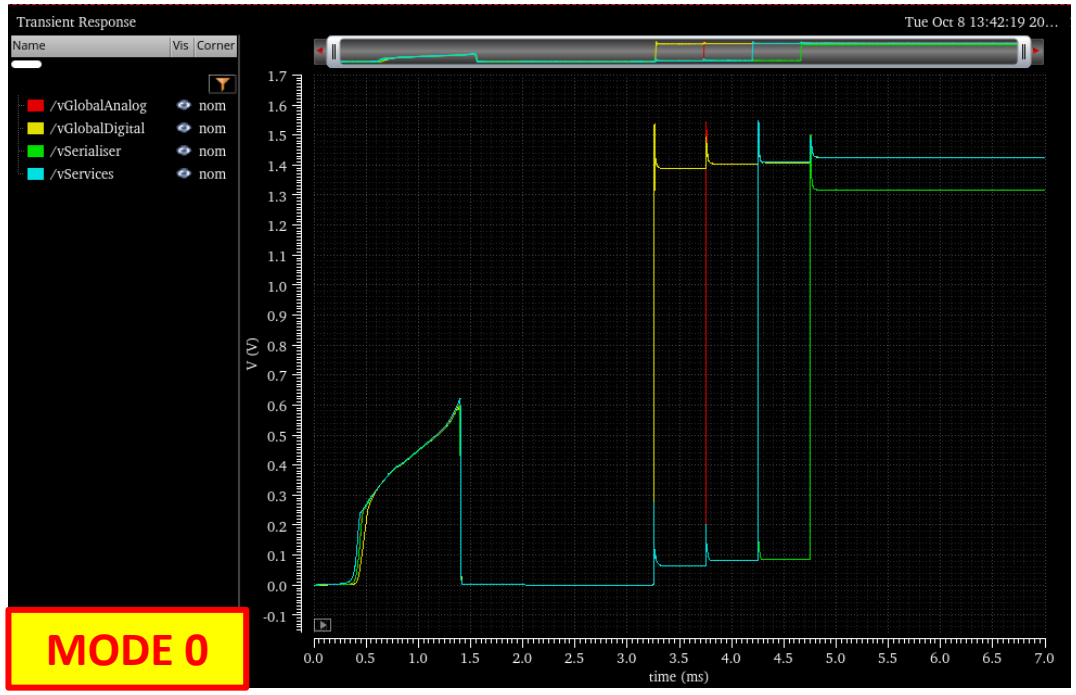
Science and Technology Facilities Council

AncASIC Performance

Boundary Conditions

- 3 Conditions
  - 6 RSU LAS – Expected
  - 6 RSU LAS – Max
  - MOSAIX (12 RSU) – Expected
- 2 Modes
  - MODE 0: SLDOs disabled at startup and turned on individually
  - MODE 1: SLDOs enabled at start-up
- +10% shunt overhead based on https://cds.cern.ch/record/2292628/files/CR2017_385.pdf





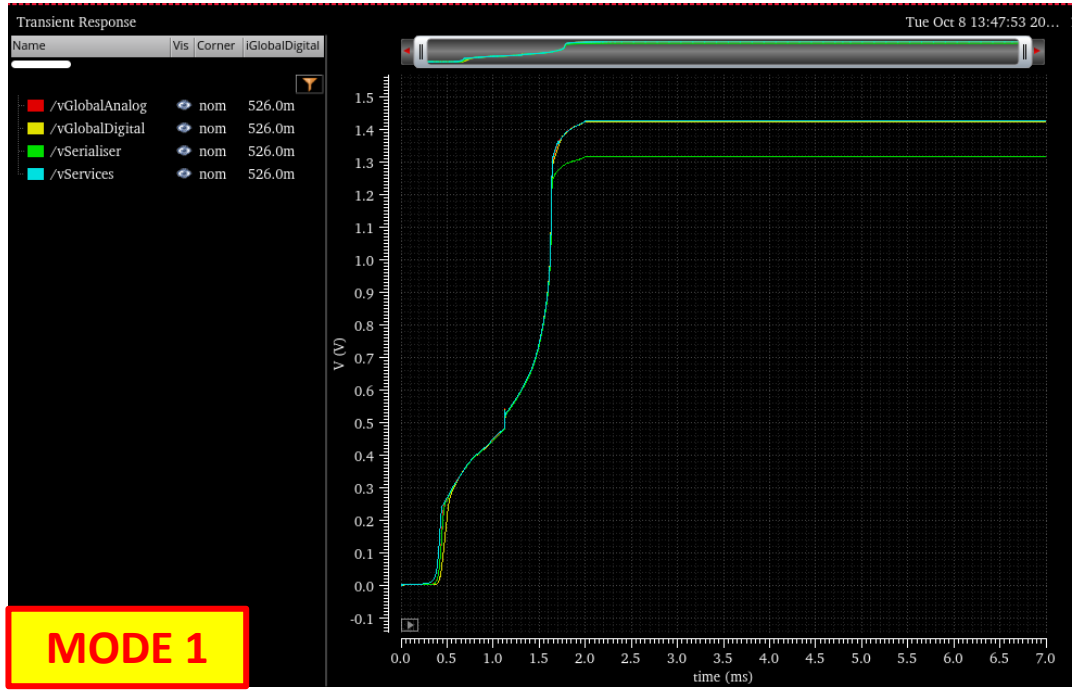
Science and Technology Facilities Council

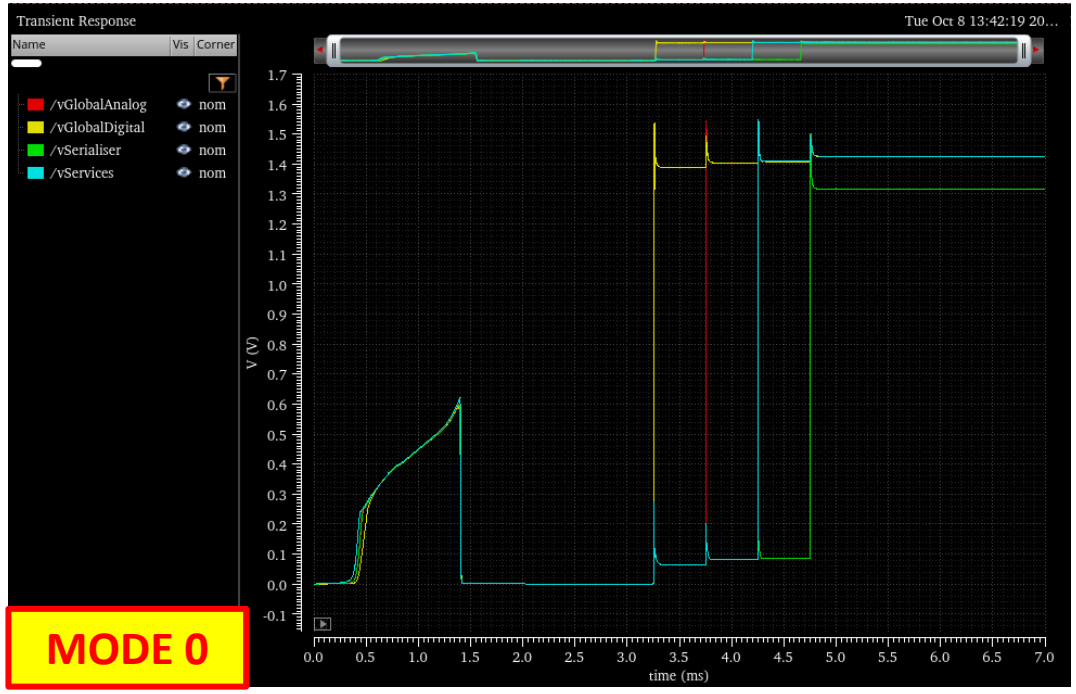
AncASIC Performance

Corners

- MOS
  - tm,wp,ws,wo,wz
- RES
  - tm,wp,ws
- CAP
  - tm,wp,ws
- BJT
  - tm,wp,ws
- TEMP
  - -20, 30, 60, 105

- 540 corners / 2 Modes / 3 Conditions
  - 3240 combinations





Science and Technology Facilities Council

AncASIC Performance

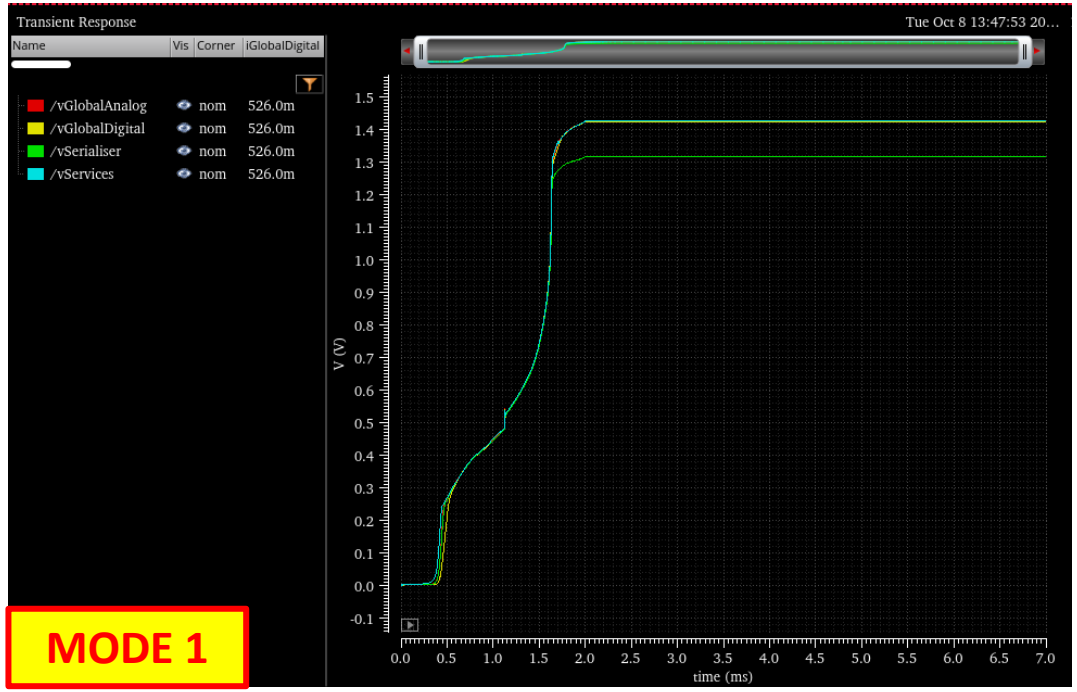
Simulation Specifications

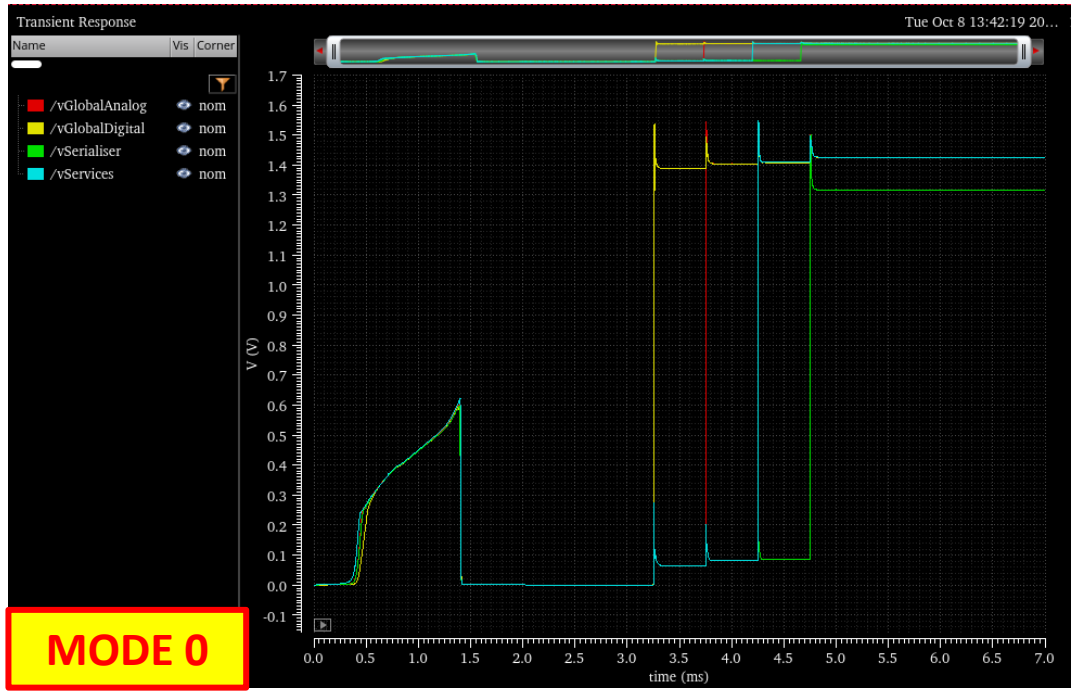
- Voltages
  - vGlobalAnalog – 1.28-1.37
  - vGlobalDigital – 1.28-1.37
  - vServices – 1.28-1.37
  - vSerialiser – 1.15 – 1.25

- Shunt Percentage
  - vGlobalAnalog – 5-15%
  - vGlobalDigital – 5-15%
  - vServices – 20-25% (min 10mA)
  - vSerialiser – 5-15%

- Dropout Voltage
  - vGlobalAnalog – 0.175 – 0.25V
  - vGlobalDigital – 0.175 – 0.25V
  - vServices – 0.175 – 0.25V
  - vSerialiser – 0.3 – 0.35V

- Shunt Power <35% of Load Power





Science and Technology Facilities Council

AncASIC Performance

Device Checks

Name	1V8_ALL
Owner	EIC_SHUNT_LDO_XT011.tb_ANC_ASIC:constraint
Enabled	true
Notes	
Model	*lvt*
Cond	v(d,s)>1.8 || v(g,s) >1.8 || v(g,d) >1.8 || v(g,b) >1.8 || v(s,b) >1.8
Duration	5e-09
Sample	start
Sort	no
Time Window	tstart,tstop
Error Limit	10000
Inst	
Xinst	
Subckt	
Xsubckt	
Depth	8

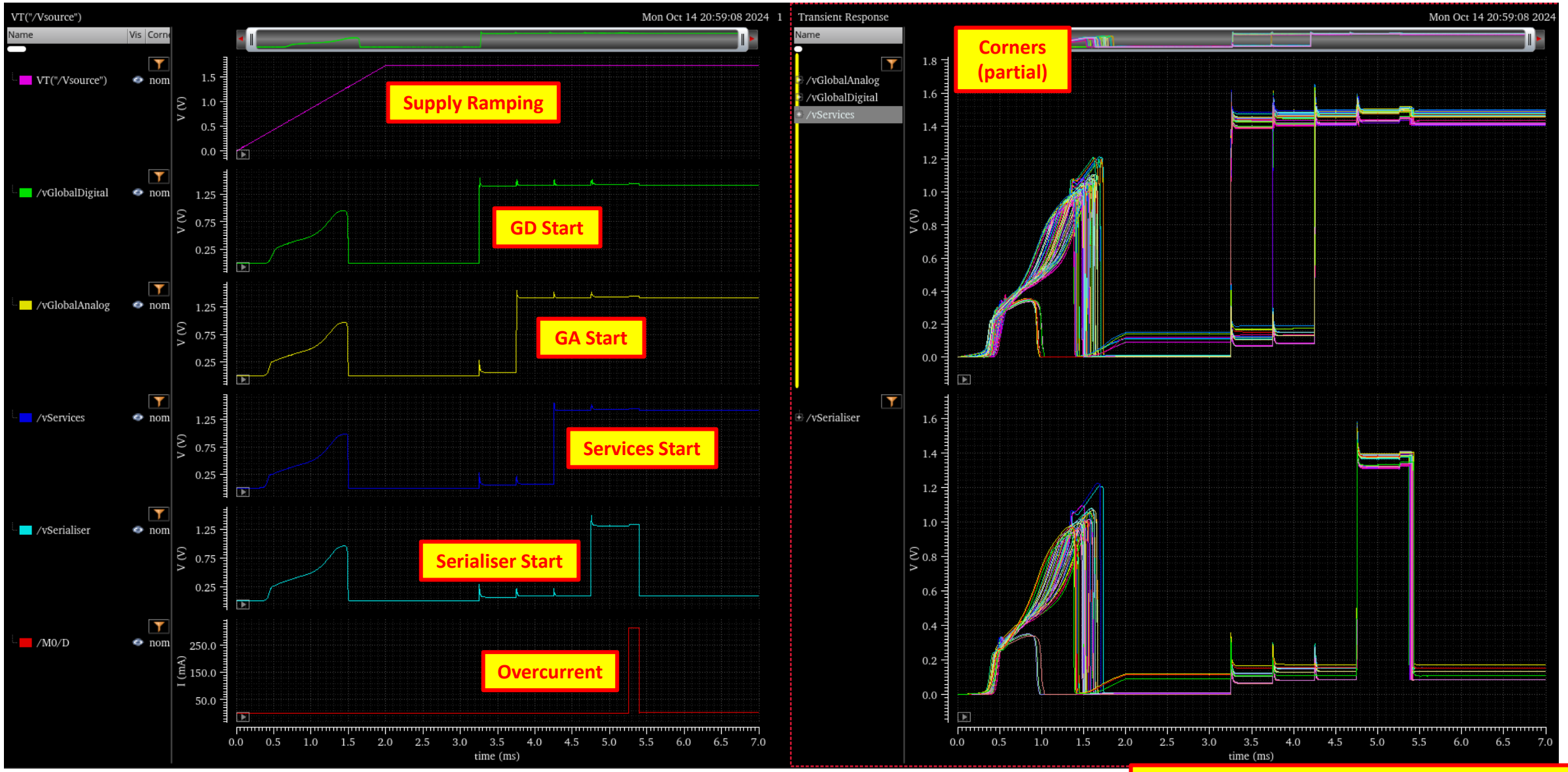
Name	1V5_POST_STARTUP
Owner	EIC_SHUNT_LDO_XT011.tb_ANC_ASIC:constraint
Enabled	true
Notes	
Model	*lvt*
Cond	v(d,s)>1.5 || v(g,s) >1.5 || v(g,d) >1.5 || v(g,b) >1.5 || v(s,b) >1.5
Duration	5e-09
Sample	start
Sort	no
Time Window	5m,1
Error Limit	10000
Inst	
Xinst	
Subckt	
Xsubckt	
Depth	8

Name	1V6_POST_STARTUP
Owner	EIC_SHUNT_LDO_XT011.tb_ANC_ASIC:constraint
Enabled	true
Notes	
Model	*lvt*
Cond	v(d,s)>1.6 || v(g,s) >1.6 || v(g,d) >1.6 || v(g,b) >1.6 || v(s,b) >1.6
Duration	5e-09
Sample	start
Sort	no
Time Window	5m,1
Error Limit	10000
Inst	
Xinst	
Subckt	
Xsubckt	
Depth	8

Name	1V7_POST_STARTUP
Owner	EIC_SHUNT_LDO_XT011.tb_ANC_ASIC:constraint
Enabled	true
Notes	
Model	*lvt*
Cond	v(d,s)>1.7 || v(g,s) >1.7 || v(g,d) >1.7 || v(g,b) >1.7 || v(s,b) >1.7
Duration	5e-09
Sample	start
Sort	no
Time Window	5m,1
Error Limit	10000
Inst	
Xinst	
Subckt	
Xsubckt	
Depth	8

Science and Technology Facilities Council

AncASIC Performance



MODE 0 – overcurrent on serialiser

AncASIC Performance

Mode 0 - Typical

Output	Nominal	Spec	Weight	Pass/Fail	Min	Max
Filter	Filter	Filter	Filter	Filter	Filter	Filter
, iGlobalAnalog=168m, R3_GlobalAnalog=16K, R3_GlobalDigital=5K, R3_Services=58K, R3_Serialiser=13K, iSerialiser=200m, iServices=40m, vChain=1.74}						
Count 'All Checks/Asserts'	4				0	4
VOUT_GlobalDigital	1.326 V	range 1.28 1.37		pass	1.306 V	1.359 V
VOUT_GlobalAnalog	1.326 V	range 1.28 1.37		pass	1.306 V	1.361 V
VOUT_Services	1.326 V	range 1.28 1.37		pass	1.307 V	1.363 V
VOUT_Serialiser	1.214 V	range 1.15 1.25		near	1.195 V	1.267 V
Shunt_Fraction_Services	25.73 %	range 20 30		fail	21.98 %	40.31 %
Shunt_Fraction_GA	11.36 %	range 5 15		near	8.685 %	15.97 %
Shunt_Fraction_GD	10.56 %	range 5 15		fail	3.514 %	12.65 %
Shunt_Fraction_Serialiser	13.22 %	range 5 15		fail	10.72 %	18.67 %
Dropout_Voltage_GD	210.6 mV	range 0.175 0.25		pass	179.1 mV	231.6 mV
Dropout_Voltage_GA	210.5 mV	range 0.175 0.25		pass	176.8 mV	231.6 mV
Dropout_Voltage_Services	210.3 mV	range 0.175 0.25		near	174.4 mV	231.5 mV
Dropout_Voltage_Serialiser	322.8 mV	range 0.3 0.35		fail	269.5 mV	342.8 mV
PWR_TOT	1.871 W				1.825 W	1.896 W
PWR_TOT_Load	1.223 W				1.187 W	1.294 W
PWR_TOT_Shunt	428.2 mW				329 mW	460.6 mW
PWR_Additional_TOT	52.95 %				41.74 %	57.18 %
PWR_Additional_SHUNT	35 %	< 35		fail	25.47 %	38.8 %
Chain_Current	1.075 A				1.049 A	1.09 A
Drop - Trace Upper	101.7 mV				99.22 mV	103.1 mV
Drop - Trace Lower	101.7 mV				99.22 mV	103.1 mV
BW Drop - GlobalDigital	20.38 mV				20.07 mV	20.9 mV
BW Drop - GlobalAnalog	15.2 mV				14.96 mV	15.62 mV
BW Drop - Serialiser	18.21 mV				17.93 mV	19.04 mV
BW Drop - Services	10.89 mV				10.72 mV	11.22 mV

Output	Nominal	Min	Max
Filter	Filter	Filter	Filter
PWR_GD_In<0>	910.4 mW	867 mW	922 mW
PWR_GD_Load<0>	700.6 mW	680.1 mW	736.2 mW
PWR_GD_Shunt<0>	209.8 mW	130.8 mW	238.3 mW
PWR_GA_In<0>	295 mW	288.5 mW	307.9 mW
PWR_GA_Load<0>	223.8 mW	217.2 mW	235.8 mW
PWR_GA_Shunt<0>	71.16 mW	60.73 mW	83.03 mW
PWR_SERV_In<0>	85.53 mW	81.8 mW	98.41 mW
PWR_SERV_Load<0>	53.3 mW	51.73 mW	56.28 mW
PWR_SERV_Shunt<0>	32.23 mW	27.78 mW	43.59 mW
PWR_Serialiser_In<0>	360.5 mW	295.3 mW	377.4 mW
PWR_Serialiser_Load<0>	245.6 mW	238 mW	267.6 mW
PWR_Serialiser_Shunt<0>	115 mW	47.18 mW	127.9 mW
GlobalDigital_Pass<0>	591 mA	561.6 mA	599.2 mA
GlobalDigital_Shunt<0>	62.39 mA	19.73 mA	75.42 mA
GlobalAnalog_Pass<0>	190.7 mA	185.9 mA	198.6 mA
GlobalAnalog_Shunt<0>	21.67 mA	16.21 mA	31.66 mA
Services_Pass<0>	54.47 mA	52.17 mA	62.53 mA
Services_Shunt<0>	14.02 mA	11.47 mA	24.61 mA
Serialiser_Pass<0>	233.4 mA	222.8 mA	244.5 mA
Serialiser_Shunt<0>	30.85 mA	24.47 mA	41.6 mA

Science and Technology Facilities Council

Also for Mode 0 Max and Mode 1 Typ and Max (see back up slides)

AncASIC Performance

Overall Power Consumption

EIC-LAS, AncASIC and Total Power (mW)	MODE 0										
	Typ				Max				Total		
	EIC-LAS	AncASIC			EIC-LAS	AncASIC			Min	Nom	Max
		Min	Nom	Max		Min	Nom	Max			
Global Digital	701	131	210	238	1088	193	341	394	832	911	1482
Global Analog	224	61	71	83	360	88	111	147	285	295	507
Services	53	28	32	44	80	18	41	66	81	85	146
Serialiser	246	47	115	128	369	37	172	246	293	361	615
Total	1224	267	428	493	1897	336	665	853	1491	1652	2750
AncASIC Power Fraction		21.81%	34.97%	40.28%		17.71%	35.06%	44.97%			

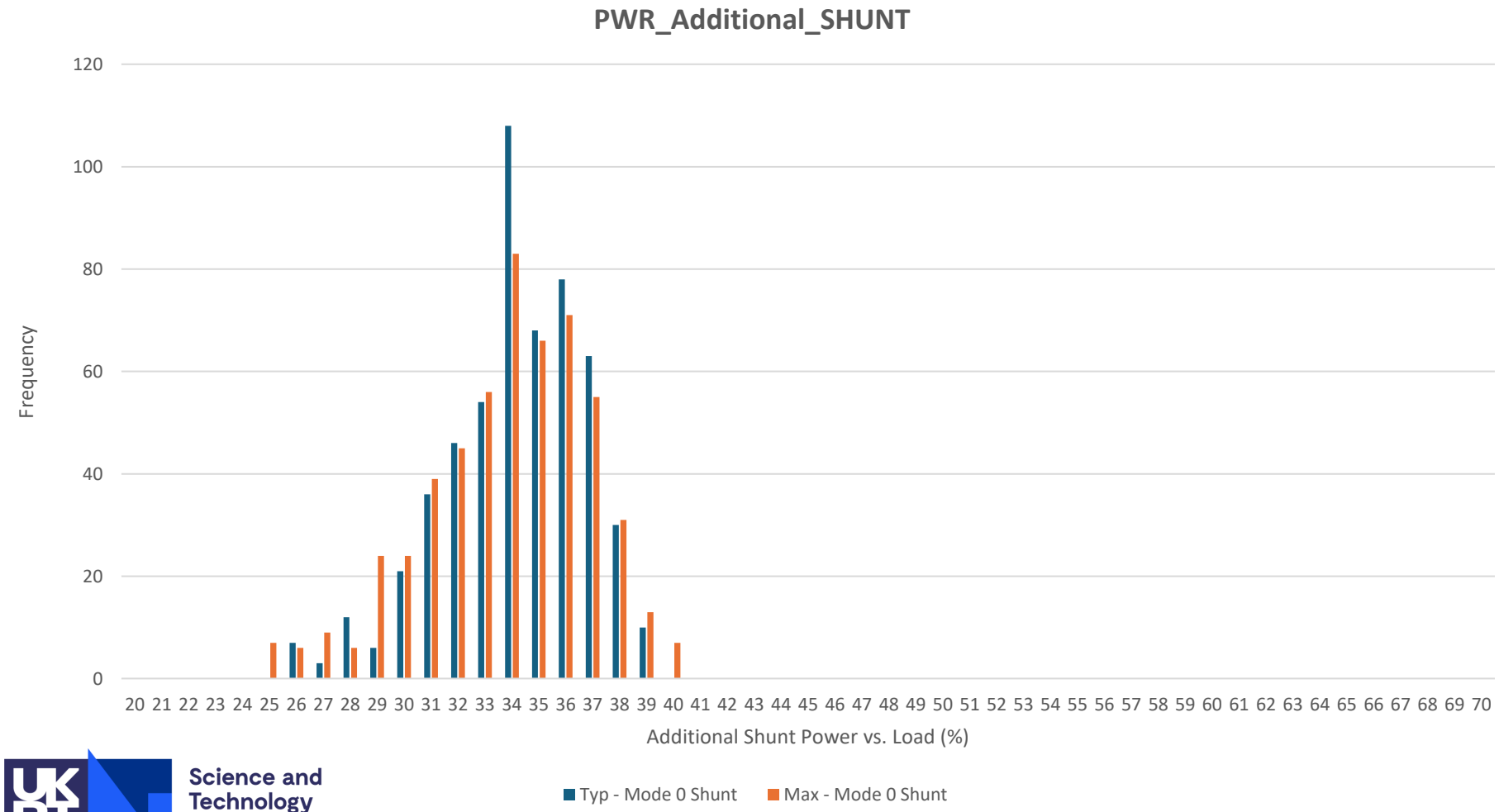
N.B. FPC traces add another 200mW

Prev values: 1702 2581

Science and Technology Facilities Council

AncASIC Performance

AncASIC Power Variation in Corners



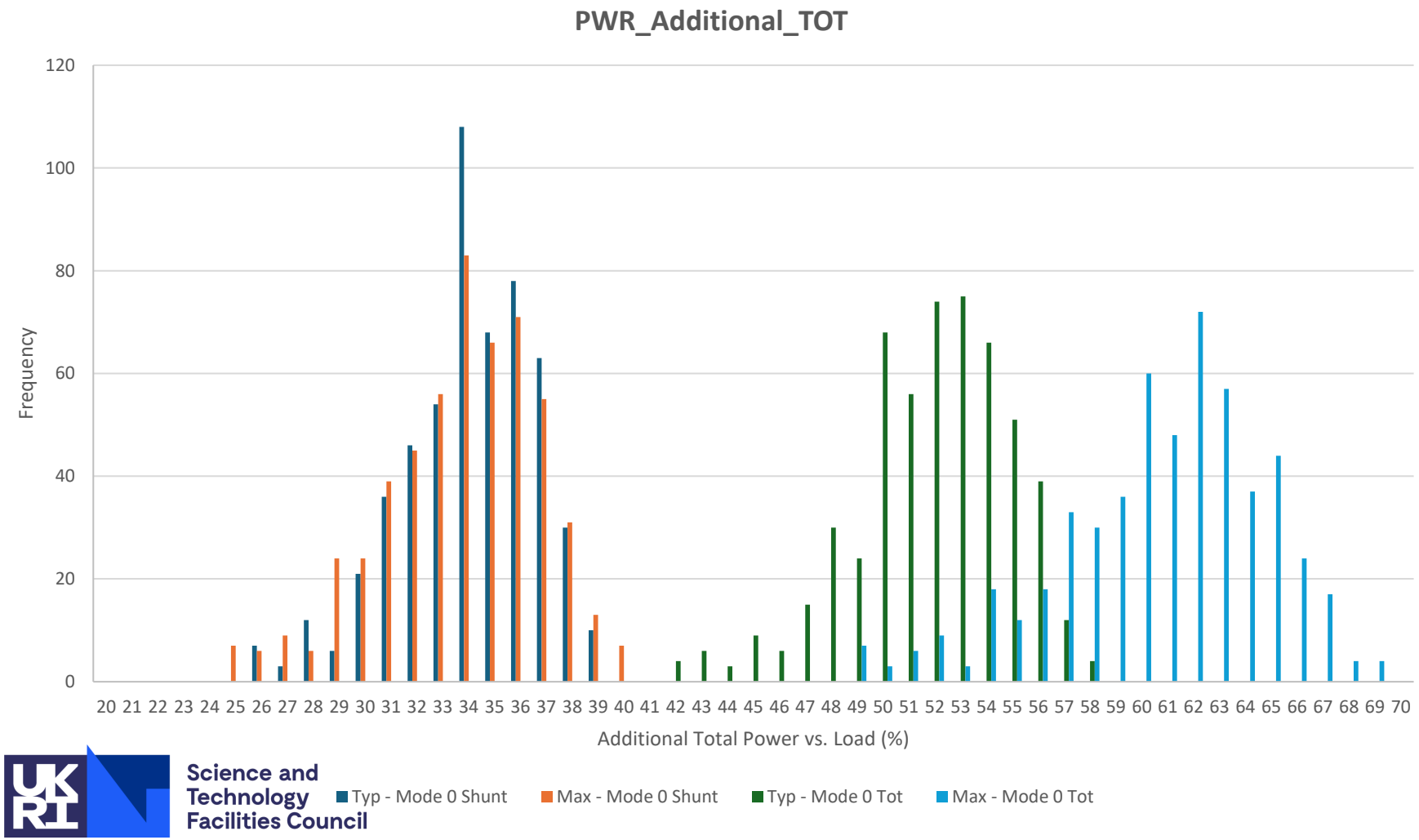
Science and Technology Facilities Council

AncASIC Power Fraction

- Graph shows power consumed by the AncASIC as a fraction of LAS power over the corners
- Typ and Max cases for LAS shown
- No major variation since presented as a percentage

AncASIC Performance

Total Power Variation in Corners



Science and Technology Facilities Council

FPC Consumption

- FPC traces consume considerable power
- Increase from ~35% to 50-60% of LAS
- Due to >1A through 200mohm
- Varies with Typ and Max corner due to current increase
- Cooling problem or not? To be included in model?

Power Caveats…

Caveats to the numbers

- Best estimate from MOSAIX. Not a warranty.
- Possibility that LEC value will rise (additional functions)
- For GAVDD, it is likely that EIC-LAS will be in the Max case, since we want the fastest frontend speed
- We may be able to reduce TXVDD consumption if we don't need all the transmitters (or can run slower)
- Need to add consumption of non-SLDO AncASIC
- Mis-match in GAVDD, GDVDD consumption may require different input voltages (waste of power in serial powering chain)
- Irradiation

Future Updates

- May be future releases from MOSAIX
- ~~AncASIC will need to be updated once porting to XT011 is completed~~
- Test results from ER2

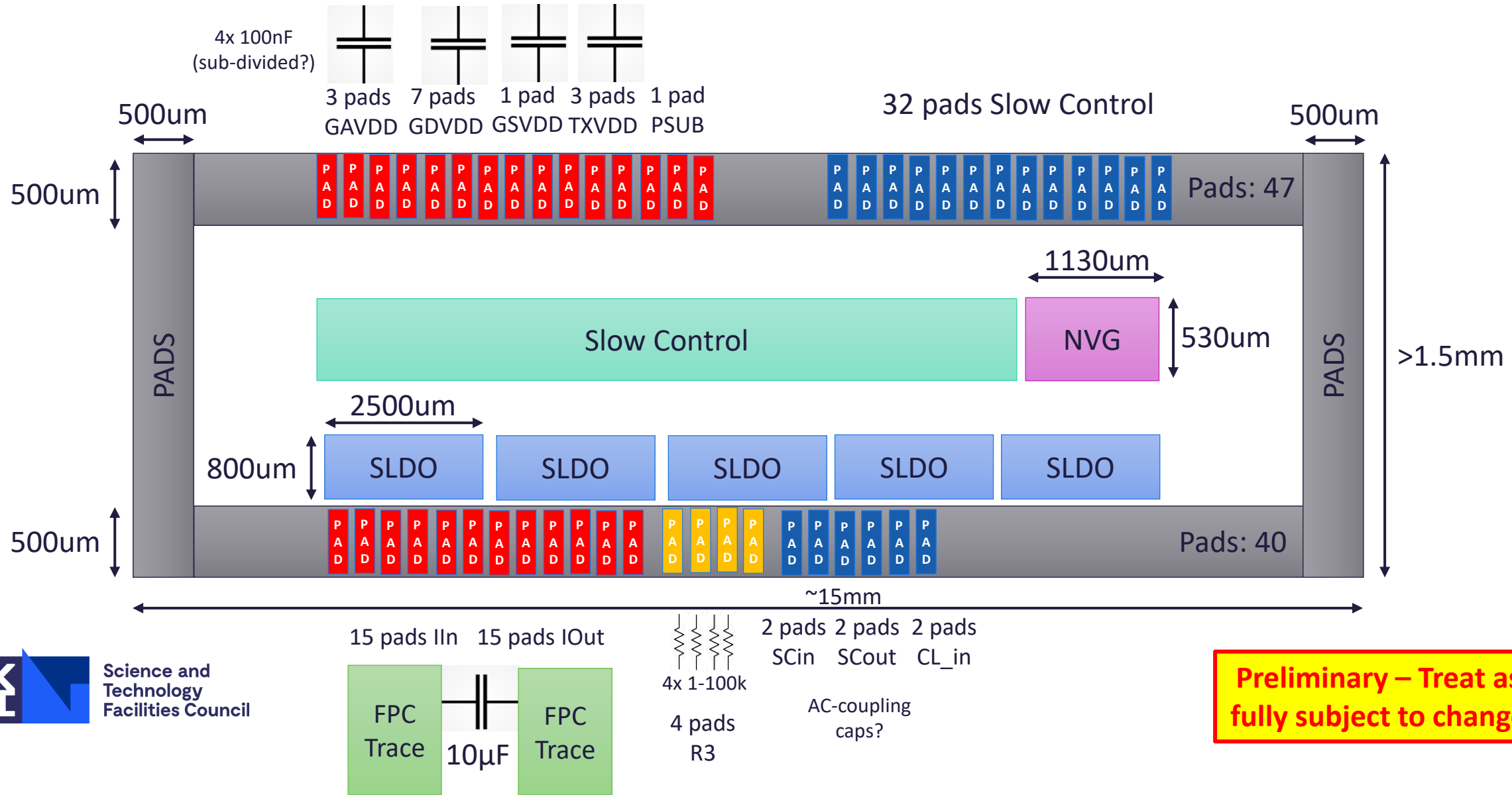
Science and Technology Facilities Council

Science and Technology Facilities Council

AncASIC Sizing

Science and Technology Facilities Council

AncASIC Size and Pads



Science and Technology Facilities Council

Preliminary – Treat as fully subject to change

Size Caveats

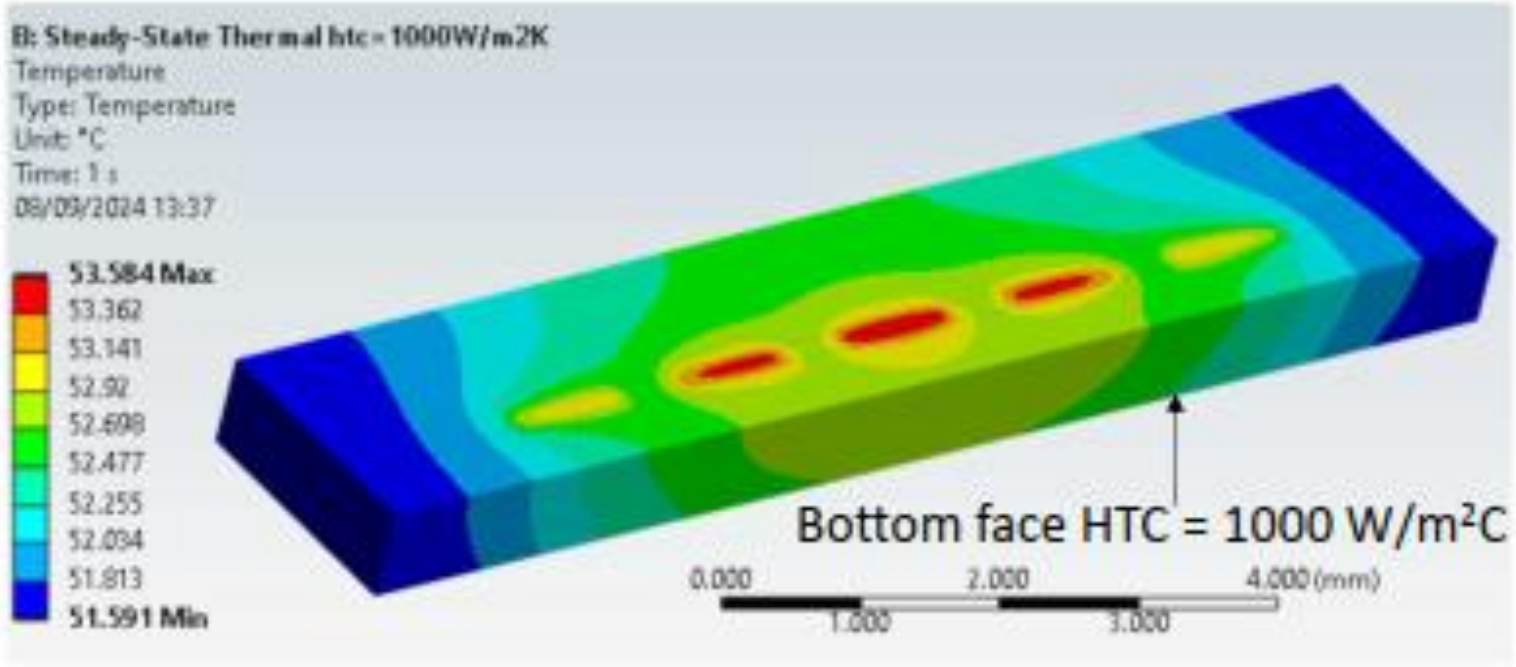
Very preliminary

- Only producing at this stage to assist with requests for stave design
- **Not discussed with other designers yet**
- Chip has 3 components:
  - Negative Voltage Generator
    - **Size unknown**
  - Slow Control Multiplexing
    - **Size unknown**
  - SLDO
    - **Size unknown**, but will probably dominate
    - Size dominated by a few transistors, so some guess at chip size can be made
    - However:
      - **Design at early stage**
      - **Sizes taken from 65nm design (not 110nm)**
- Of course, this also means we can be open to comments
- ~~**Need someone to do thermal FEA – now that size and power are known**~~

Science and Technology Facilities Council

Preliminary – Treat as fully subject to change

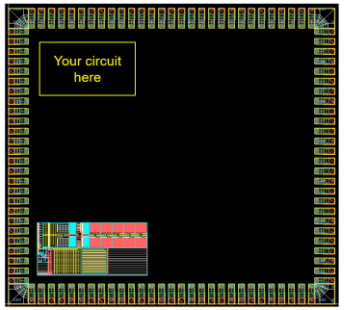
Thermal Studies



All Stephanie's work. See later! ☺

Science and Technology Facilities Council

AncASIC Progress



Progress

- A lot of work in simulation and estimation to allow mechanical/thermal design to proceed
- Target schedule of submissions towards AncASIC

Tape-in date	Expected from Foundry	Circuit Details			
		NVG	Slow Control	SLDO	Irradiation Test Structures
~~02/09/24~~	~~24/03/25~~	~~Basic NVG~~	~~Daisy Chain and I2C~~	~~Sub-regulators~~	~~LVT Transistors~~ ~~MOSVCTI Capacitors~~ ~~BJT~~
25/11/24	16/06/25	NVG with (partial?) monitoring ADC	TBD - Alternative powering? Daisy Chain and I2C	Full SLDO	LVT Transistors MOSVCTI Capacitors BJT
March 2025	Oct 2025	AncASIC V1 (inc. Full NVG and AncASIC)			
May 2025	Dec 2025	AncASIC V2 (production?)			

- NVG: Simulated and layout well underway. Virtually complete for November run
- SLDO: Verification sims still ongoing. Layout started. Targeting November but very resource challenged.
- Slow Control: Conceptual. BNL plan to have funding next FY to start design on FPGA
- In general, many legal and procedural hurdles at the moment.