Update on Flexible Printed Circuits (FPCs)

19/11/2024

M.Borri on behalf of WP3 Electrical Interfaces

Science and Technology Facilities Council

Outline

- Low TRL OB prototypes: recap.
- Status of assembly.
- Test plan.
- Conclusion and future work.

Spoiler:
No results yet!

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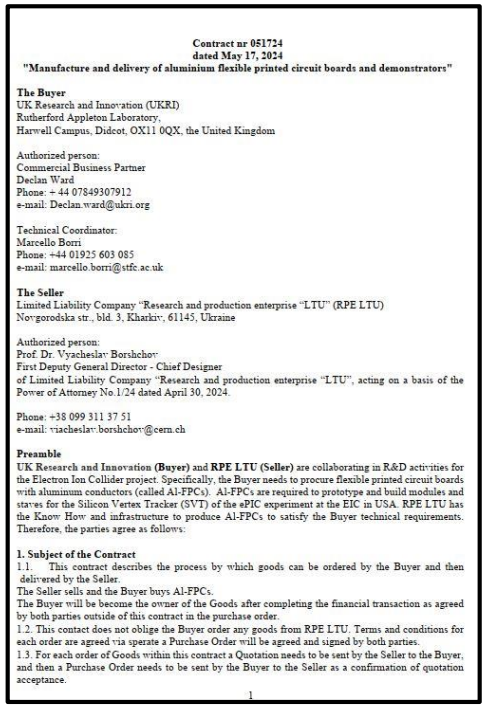
Low TRL OB prototypes: time-line

- Defined requirements:
  - 18/03/2024
- Design review:
  - 16/05/2024
- Prototypes delivery:
  - 08/10/2024
- Testing:
  - To assemble to interface cards;
  - To distribute and test;

- Issue so far:
  - RPE LTU customer contract ☑

Administrative issue



Contract nr 051724
dated May 17, 2024
"Manufacture and delivery of aluminium flexible printed circuit boards and demonstrators"

The Buyer
UK Research and Innovation (UKRI)
Rutherford Appleton Laboratory,
Harwell Campus, Didcot, OX11 0QX, the United Kingdom

Authorized person:
Commercial Business Partner
Declan Ward
Phone: + 44 07849307912
e-mail: Declan.ward@ukri.org

Technical Coordinator:
Marcello Borri
Phone: +44 01925 603 085
e-mail: marcello.borri@stfc.ac.uk

The Seller
Limited Liability Company "Research and production enterprise "LTU" (RPE LTU)
Novgorodska str., bld. 3, Kharkiv, 61145, Ukraine

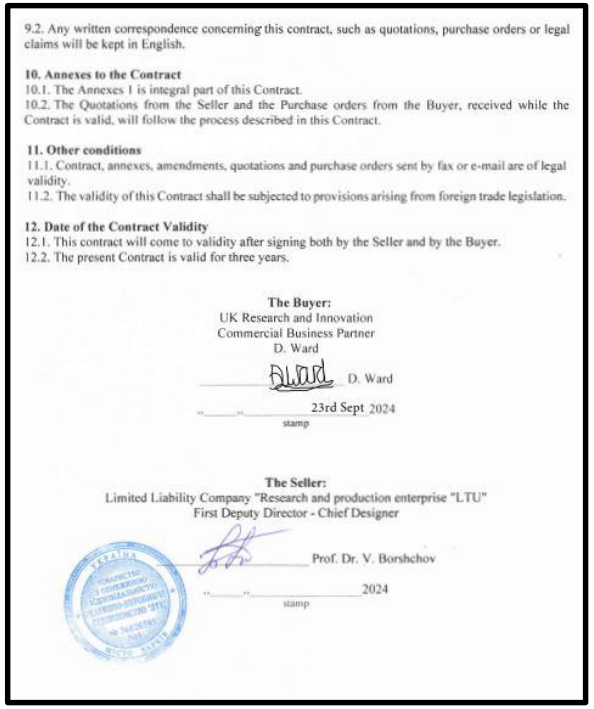
Authorized person:
Prof. Dr. Vyacheslav Borshchov
First Deputy General Director - Chief Designer
of Limited Liability Company "Research and production enterprise "LTU", acting on a basis of the Power of Attorney No.1/24 dated April 30, 2024.

Phone: +38 099 311 37 51
e-mail: viacheslav.borshchov@cern.ch

Preamble
UK Research and Innovation (Buyer) and **RPE LTU (Seller)** are collaborating in R&D activities for the Electron Ion Collider project. Specifically, the Buyer needs to procure flexible printed circuit boards with aluminium conductors (called Al-FPCs). Al-FPCs are required to prototype and build modules and staves for the Silicon Vertex Tracker (SVT) of the ePIC experiment at the EIC in USA. RPE LTU has the Know How and infrastructure to produce Al-FPCs to satisfy the Buyer technical requirements. Therefore, the parties agree as follows:

1. Subject of the Contract
1.1. This contract describes the process by which goods can be ordered by the Buyer and then delivered by the Seller.
The Seller sells and the Buyer buys Al-FPCs.
The Buyer will be become the owner of the Goods after completing the financial transaction as agreed by both parties outside of this contract in the purchase order.
1.2. This contact does not oblige the Buyer order any goods from RPE LTU. Terms and conditions for each order are agreed via sperate a Purchase Order will be agreed and signed by both parties.
1.3. For each order of Goods within this contract a Quotation needs to be sent by the Seller to the Buyer, and then a Purchase Order needs to be sent by the Buyer to the Seller as a confirmation of quotation acceptance.

1



9.2. Any written correspondence concerning this contract, such as quotations, purchase orders or legal claims will be kept in English.

10. Annexes to the Contract
10.1. The Annexes 1 is integral part of this Contract.
10.2. The Quotations from the Seller and the Purchase orders from the Buyer, received while the Contract is valid, will follow the process described in this Contract.

11. Other conditions
11.1. Contract, annexes, amendments, quotations and purchase orders sent by fax or e-mail are of legal validity.
11.2. The validity of this Contract shall be subjected to provisions arising from foreign trade legislation.

12. Date of the Contract Validity
12.1. This contract will come to validity after signing both by the Seller and by the Buyer.
12.2. The present Contract is valid for three years.

The Buyer:
UK Research and Innovation
Commercial Business Partner
D. Ward
D. Ward
23rd Sept 2024
stamp

The Seller:
Limited Liability Company "Research and production enterprise "LTU"
First Deputy Director - Chief Designer
Prof. Dr. V. Borshchov
2024
stamp

Issued on 17/05/2024
Signed on 23/09/2024

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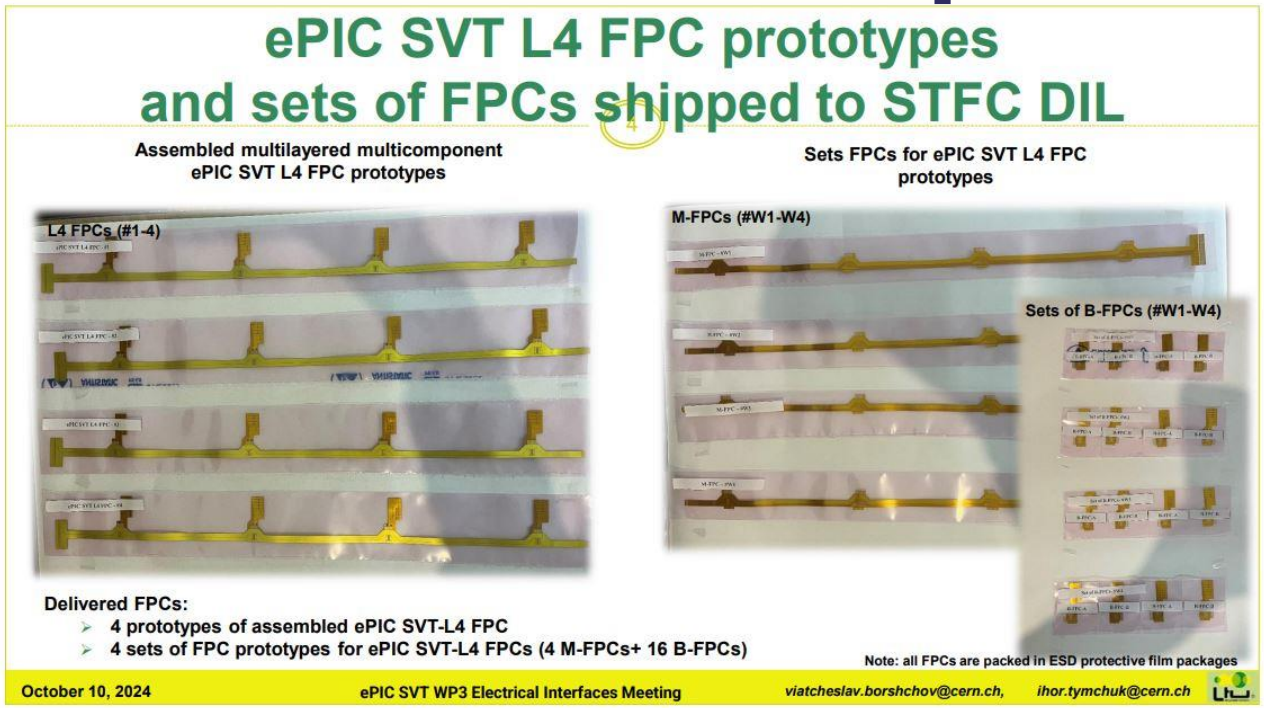
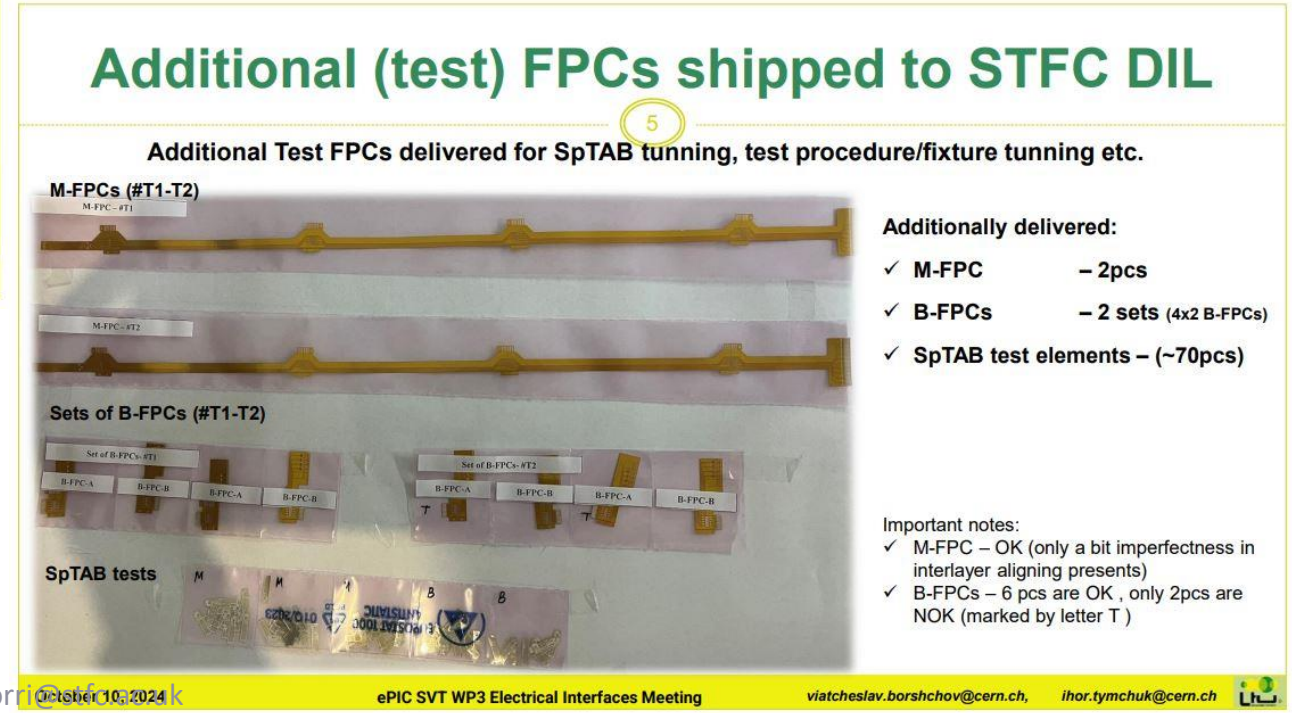
marcello.borri@stfc.ac.uk

Low TRL OB prototypes: delivery



A lot of details in the design…

I.Tymchuk:
30 masks in total were required for M-FPC + B-FPC-A + B-FPC-B;
i.e. 10 photomasks for each FPC were required;
(usually a 2 layer FPC requires up to 6 masks)



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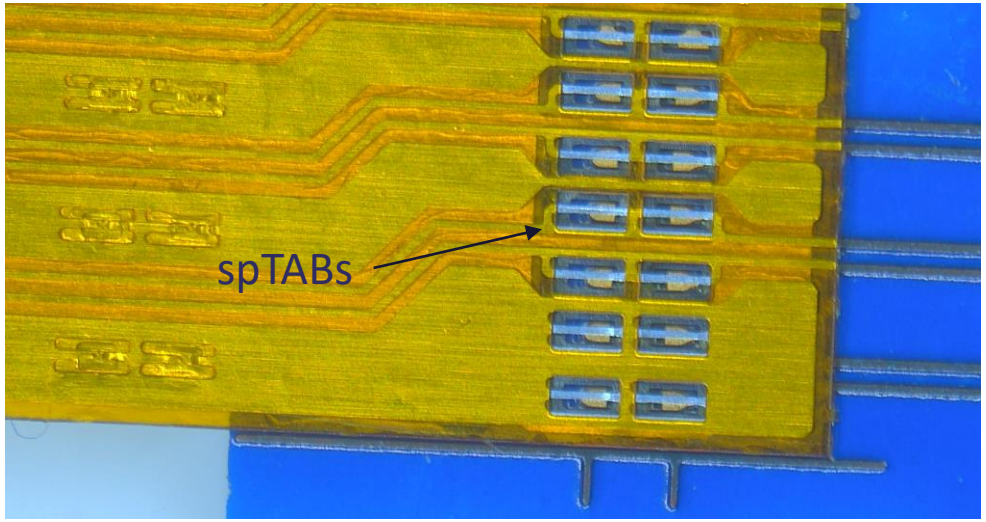
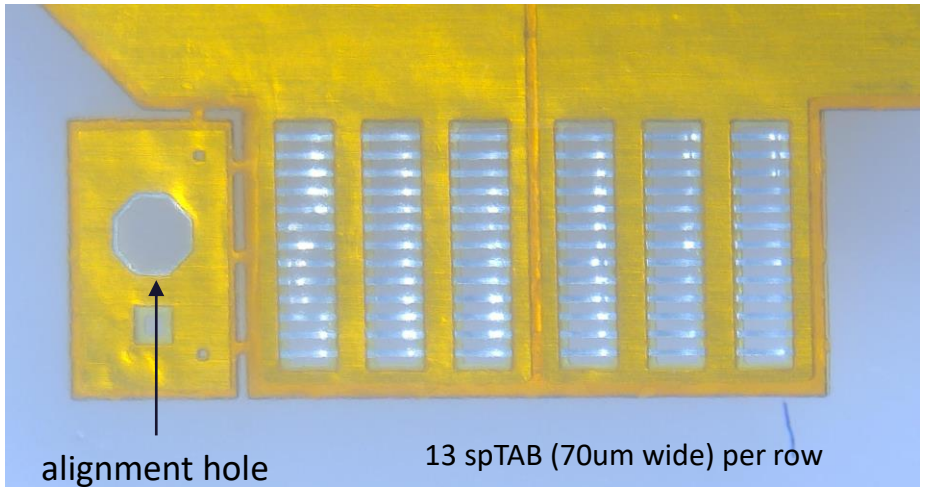
Low TRL OB prototypes: visual inspection at DL

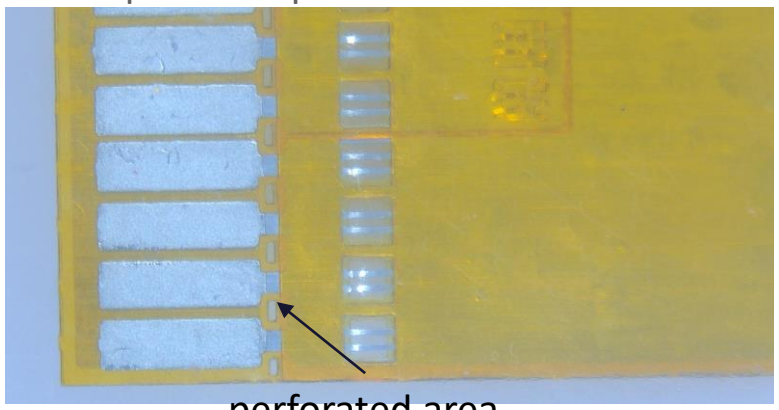
Alignment of FPC to interface PCB



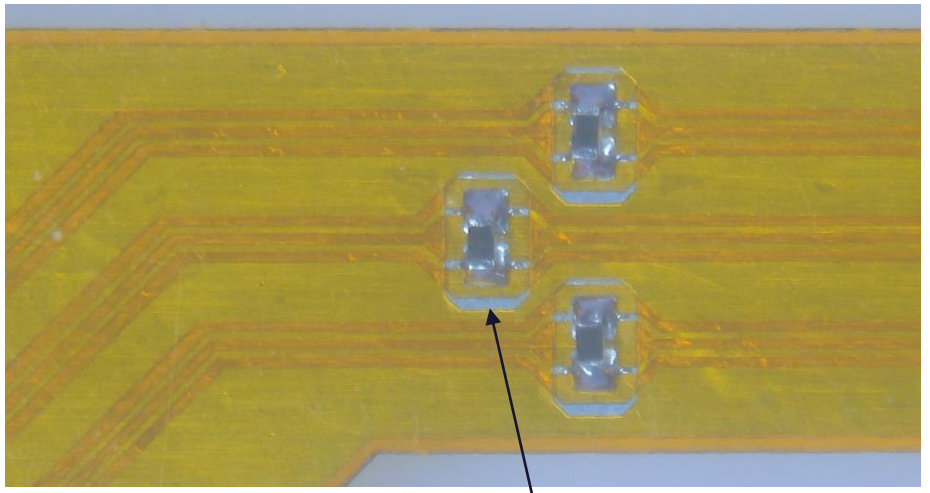
Current in/out spTABs at joint with bridge FPC



Probe pads and perforated area



0201 components



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Low TRL OB prototypes: visual inspection at DL

Schematic cross-section of M-FPC and B-FPC

Total = ~115um

Difference ~3.6um

Measured 111.4um

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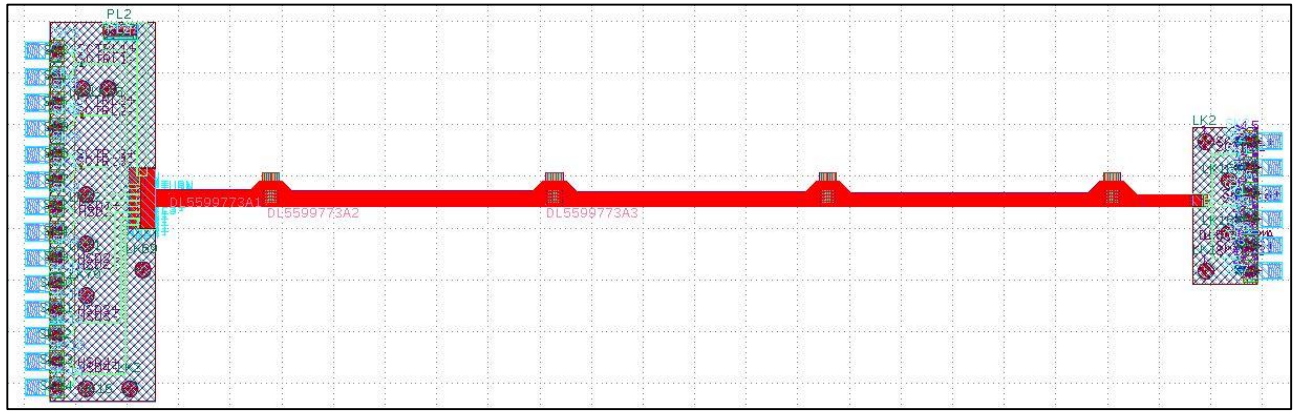
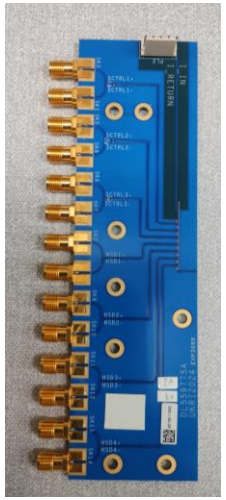
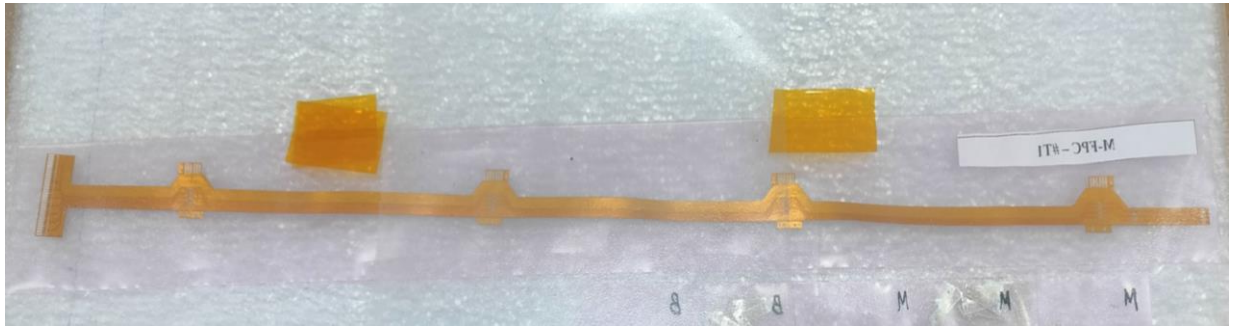
Low TRL OB prototypes: interconnection

- Interconnection required in order to enable electrical testing;
- The FPCs are interconnected to interface cards;
  - This improves signal transmission to/from the FPC;
- We start simple:
  - M-FPC to interface cards;

Sketch of the main FPC (M-FPC) to interconnected to interface cards







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Low TRL OB prototypes: interconnection

- Selection of interconnection site, options:
  - RAL
  - Oxford
  - L'pool (only briefly)
  - B'ham ☑
- From July 2024:
  - Discussed details of the job;
  - Visited sites;
  - … but because we could not estimate a delivery date, nothing tangible happened. (Pressure from other jobs/projects)
  - Converged on the selection of the interconnection site later than expected.

Wedge required to spTAB prototypes to interface PCBs

Ordered by J.Glover, estimated delivery ~11/12/2024.

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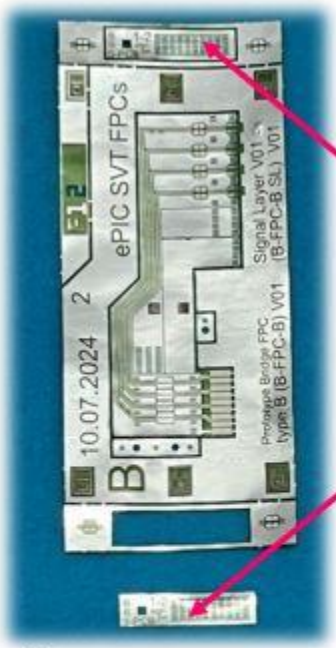
SpTAB test elements for investigating/checking bond parameters

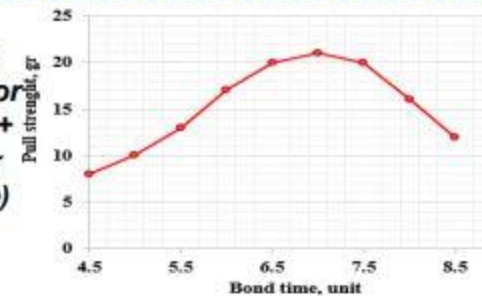
- ***For SpTAB need to be done investigating and verifying bonding parameters***
- ***For this purpose special bond test elements are using*** *(same trace width as in bond area)*
- ***Bond test elements are made of same material as object for bonding*** *(top and bottom layers of multilayered flex)*
- ***Bond parameters need to be investigated/verified for each/different bonder***

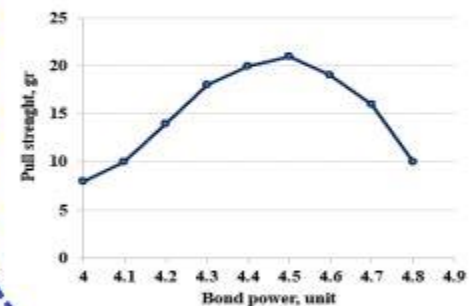


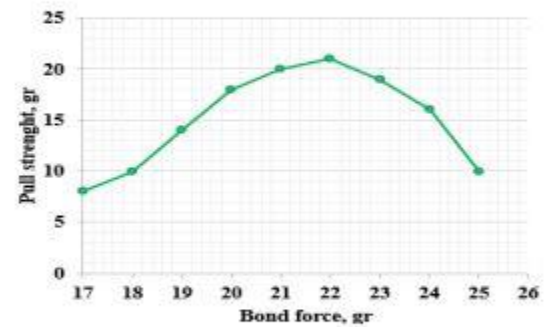
SpTAB test element

@B'ham
Would you have in mind
a substrate for these tests?

Examples of dependencies of pull strength on bonding parameters for SpTAB bonds of FPC (LTU-15-10) + MAPS chip, trace width 120um (for semi- automated bonder UZSM-type)

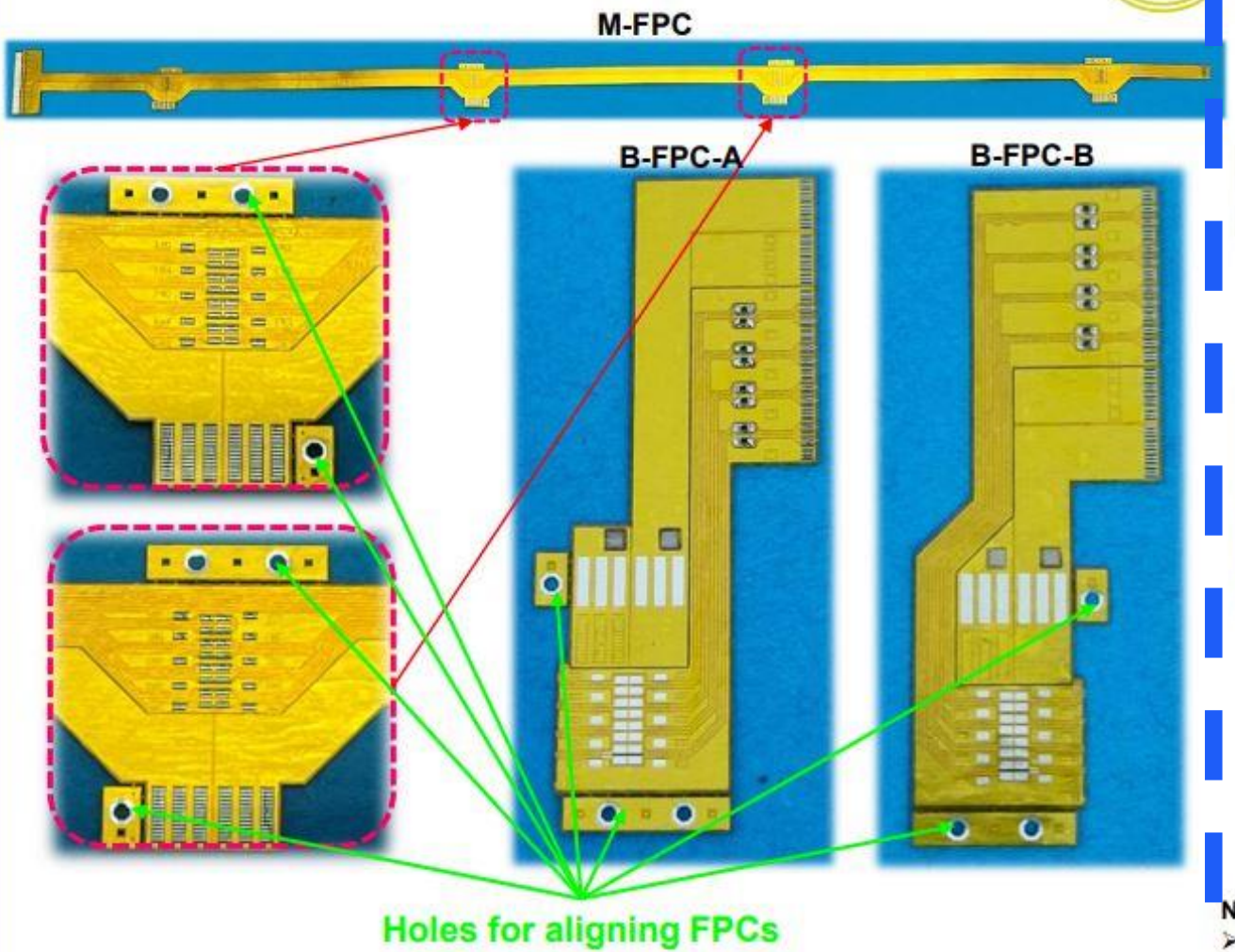






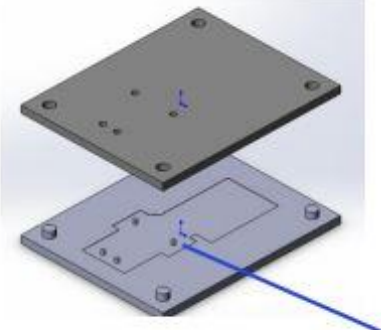
Note:
typically SpTAB test elements are delivering together with FPCs

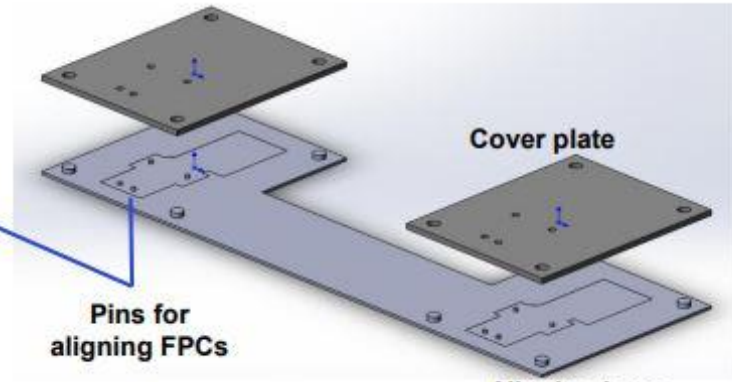
Possible approach to aligning FPCs and 3-D printed jig for assembling ePIC SVT FPC

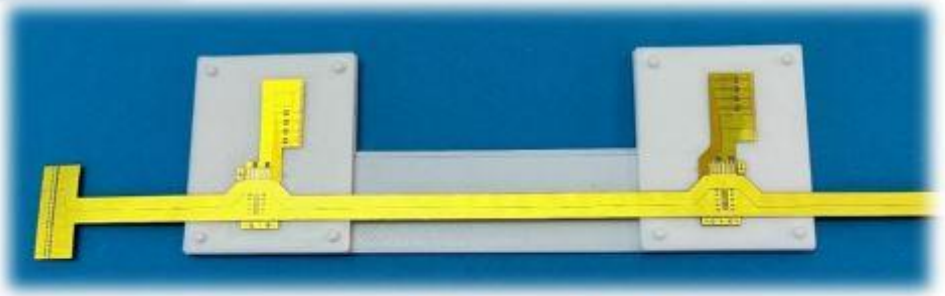


Single B-FPC approach

To replicate @ B'ham
Inc. interface cards for B-FPCs





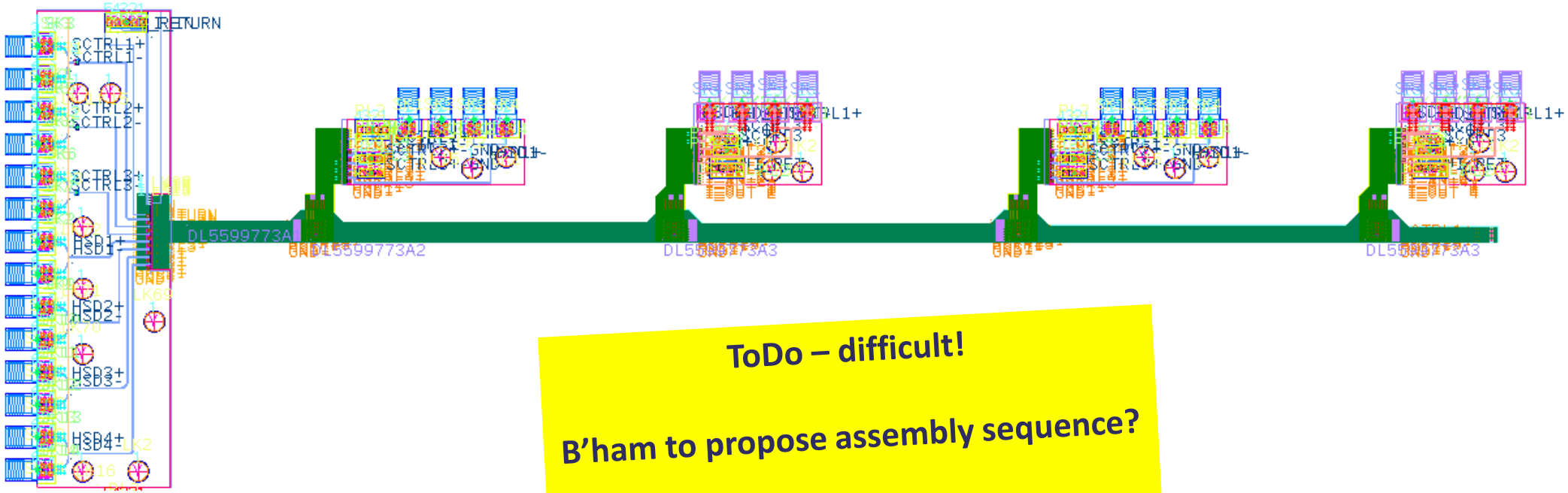


Notes:
- *Single-B-FPC jig is intended for aligning both B-FPC-A and B-FPC-B*
- *Base approach is verified (set of jig 3-D printed out, few iterations)*

Further down the line to try in-house spTAB bonding of B-FPCs to M-FPCs

viatcheslav.borshchov@cern.ch, ihor.tymchuk@cern.ch

Low TRL OB prototypes: interconnection further steps



ToDo – difficult!

B'ham to propose assembly sequence?

Example
1- B-FPC to B-int'face-PCB
2- B-FPC to M-FPC
3- M-FPC to M-int'face-PCB

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What do we test for: signal and pwr integrity

- Signal integrity.
  - The ability to propagate signals without distortions

- Factors that contribute to signal integrity degradation:
  - Reflections
    - Impedance discontinuities
  - Cross talk
    - Mutual parasitic capacitance & inductance
  - Skew
    - Propagation delays
  - Jitter
    - Non-uniform impedance, crosstalk, interference, and power supply noise
  - Signal attenuation
    - Losses caused by conductive and dielectric energy dissipation.

- Power integrity
  - Reduced Noise pick up
    - Decoupling capacitors (Equivalent Series Resistor)
    - Coherent grounding strategy over the Power Distribution Network
  - Acceptable IR drop (and related FPC power consumption)

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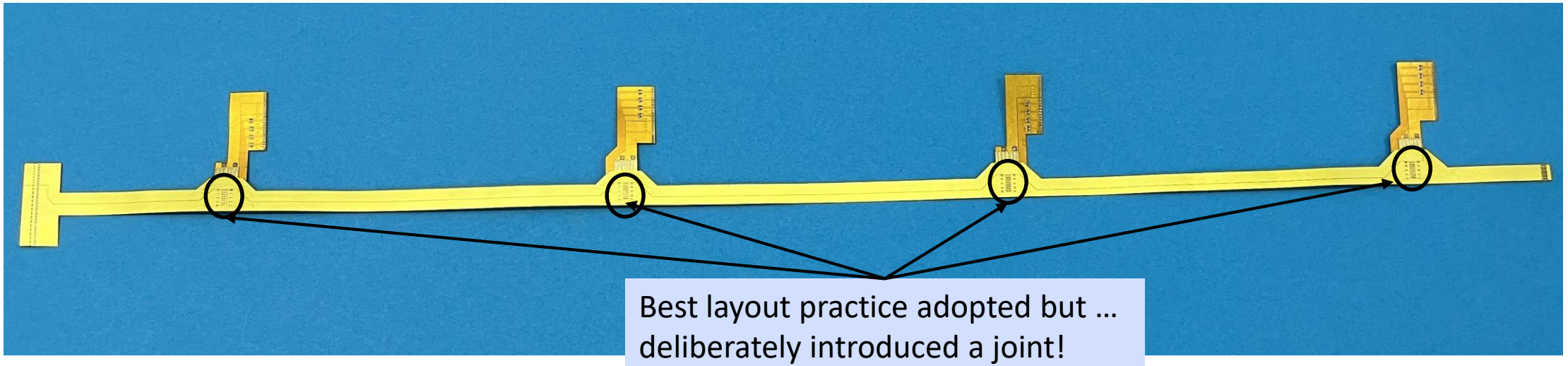
Signal integrity: layout dependent



The most important cause of signal integrity issues in a PCB is faster signal rise times.

Signal name	Type	Comment	Coupling	Standard	lpGBT eLink	Rate
slow ctrl clk (down)	AC	from lpGBT to AncASIC	Capacitive	CERN Low Powering Signal (CLPS)	clock-eLink	80 Mb/s
slow ctrl write (down)	AC	from lpGBT to AncASIC	Capacitive	CERN Low Powering Signal (CLPS)	output-eLink	80 Mb/s
slow ctrl read (up)	AC	from AncAsic to lpGBT	Capacitive	CERN Low Powering Signal (CLPS)	input-eLink	160 Mb/s
data	AC	from AncAsic to VTRX+ (1 diff line/AncASIC)	Capacitive	CERN Low Powering Signal (CLPS)	N/A	5.12 Gb/s (or 10Gb/s)
voltage supply	DC	Max: (2.5V/AncASIC) * (4 AncASIC)	Direct	10% Vdrop for 2.5V/LAS, is it OK?	N/A	N/A
current	DC	2.5 A (total per AnASIC)	Direct		N/A	N/A

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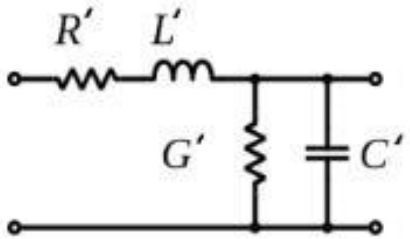
https://www.microwaves101.com/encyclopedias/transmission-line-loss

Transmission lines – signal attenuation



Infinitesimal portion of transmission line

KCL + KVL

$$\frac{\partial v(z,t)}{\partial z} = -Ri(z,t) - L\frac{\partial i(z,t)}{\partial t}$$
$$\frac{\partial i(z,t)}{\partial z} = -Gv(z,t) - C\frac{\partial v(z,t)}{\partial t}$$

$$V(z) = V_0^+ e^{-\gamma z} + V_0^- e^{\gamma z}$$

$$I(z) = I_0^+ e^{-\gamma z} + I_0^- e^{\gamma z}$$

Schematic cross-section of M-FPC and B-FPC

Let γ = α + jβ or α + j(2π/λ)

γ = complex propagation constant
α = attenuation constant (nepers/unit length)
β = phase constant (radians/unit length)
λ = wavelength
ω = angular frequency (radians/second)

$\alpha = \alpha_C + \alpha_D + \alpha_G + \alpha_R$

α_C = loss due to metal conductivity

α_D = loss due to dielectric loss tangent

α_G = loss due to conductivity of dielectric

α_R = loss due to radiation

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Testing – first tests to do at DL

Main FPC only, slow control

Inject Data or Clock and data into SCTL1…3 from KCU105 via SMA cables

Remove termination from Main FPC

View SCTL1..3 with Scope

- Connect via SMA cable
  - 50 Ω terminated to GND at scope
  - Remove termination on test card
- Or connect via Hi (active) scope probe
  - With termination on test card.
- Also consider test in reverse direction.
- Additionally test these lines at > 1 Gbits/s using iBert bitstreams and MGT.

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Equipment

EK-U1-KCU105-G	https://www.digikey.co.uk/en/products/detail/amd/EK-U1-KCU105-G/5080514	KCU105
CCSMA-MM-SS402-24	https://www.digikey.co.uk/en/products/detail/crystek-corporation/CCSMA-MM-SS402-24/2137809	24 inch cable.
CCSMA-MM-SS402-36	https://www.digikey.co.uk/en/products/detail/crystek-corporation/CCSMA-MM-SS402-36/2137810	36 inch cable.
ADP-SMAF-BNCM	https://www.digikey.co.uk/en/products/detail/linx-technologies-inc/ADP-SMAF-BNCM/9826665	BNC to SMA adapter

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High speed data & first tests

VTRx+ TX input Eye mask

Specification	Value
X1 @ UI=97.66ps	10.7 ps
X2	30.3 ps
Y1	95 mV
Y2	350 mV

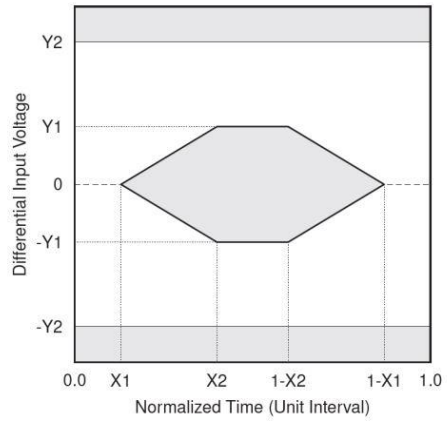

Figure 6: Electrical Eye Mask for 4.2.5 Tx Input & 4.4.5 Rx Output

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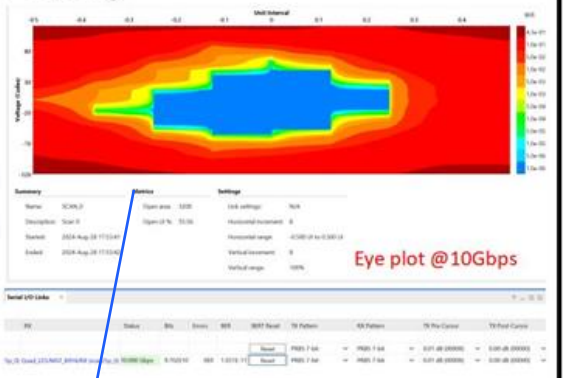
LBNL results w prototypes from Omni Circuits (dielectric is ArlonEmd)

BERKELEY LAB

Updates for Today

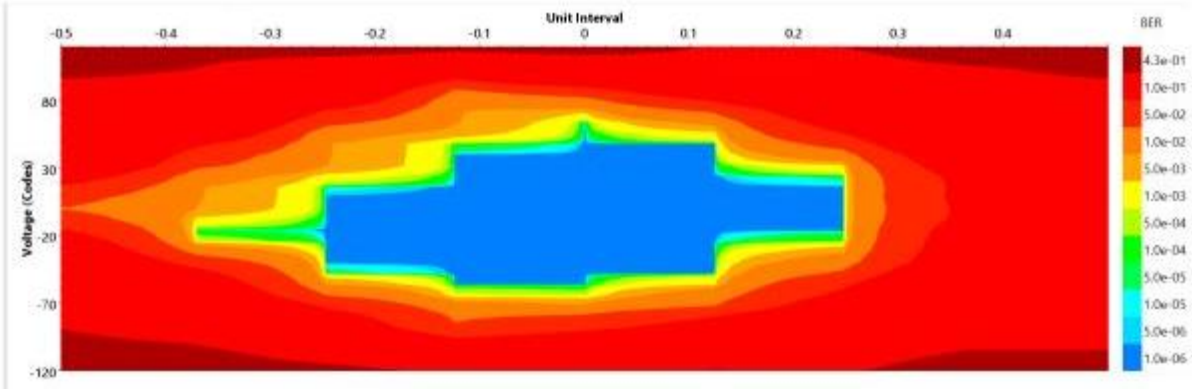
- Received a 2nd set of Al-based FPC prototypes from OMNI.
  - Double metal layer with 25 cm long differential lines for high-speed data transmission
- Improvements compared to the previous set
  - Soldering and vias facilitated by selective Cu plating
  - Improved high frequency signal transmission property based on S21 measured up to 4 GHz
  - IBERT test done with FPGA suggests that these FPC support GTY communication @10Gbps
- Questions to follow up:
  - Check the mechanical properties of the FPC
  - 2 out of 36 connector pads detached from the FPC when disconnecting the cable
  - Total material budget of the FPC is 0.136% X_0 (TBC), with dominant contribution from dielectrics. Can this be reduced
- Plan:
  - Manufacture FPC based on LTU/STFC design but modified to be consistent with vendor's design rules if there is no objection.



Eye plot @10Gbps

Promising result

September 12, 2024 Zhengwei Xue 2



… conversion to Volt and time possible.

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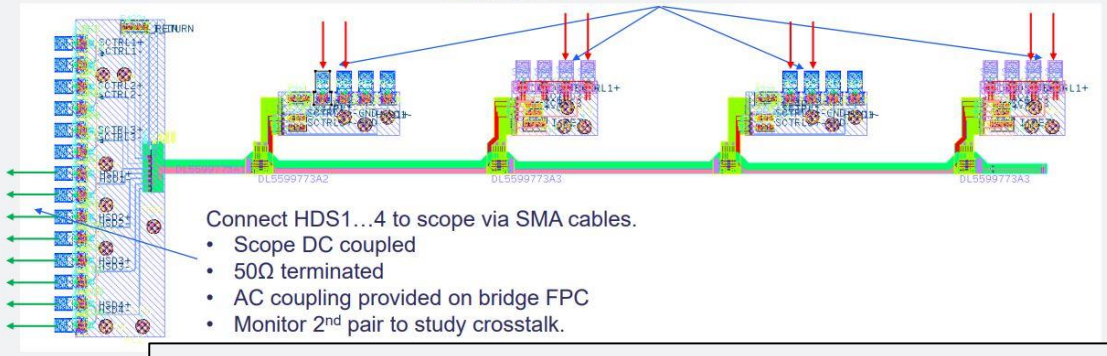
Further testing

High speed signals

Inject Data into HSD1..4 from KCU105 via SMA cables.



Connect HDS1…4 to scope via SMA cables.

- Scope DC coupled
- 50Ω terminated
- AC coupling provided on bridge FPC
- Monitor 2nd pair to study crosstalk.

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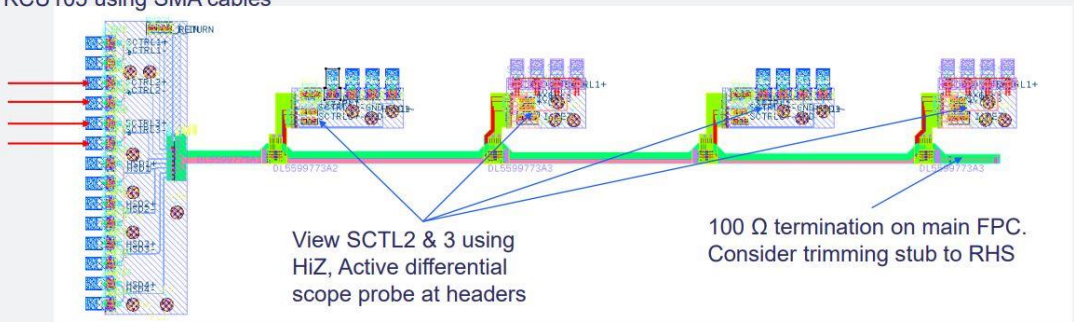
Slow Control Clock and TX data SCTL2 & 3

Inject Data or Clock and data into SCTL2…3 from KCU105 using SMA cables



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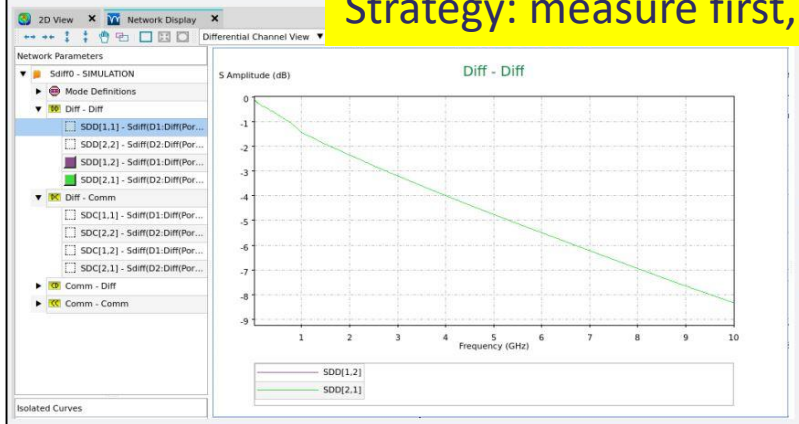
Clarity3d layout simulations of 100 mm pair

Strategy: measure first, simulate after



- -0.076 dB at 10 MHz
- = 0.99 transmission
- expect 0.97 at DC
- -8.4 dB @ 10 GHz
- Predicted -4.23
- Explained by different values of Df.
- Clarity material: Df= 0.035 @ 10 GHz

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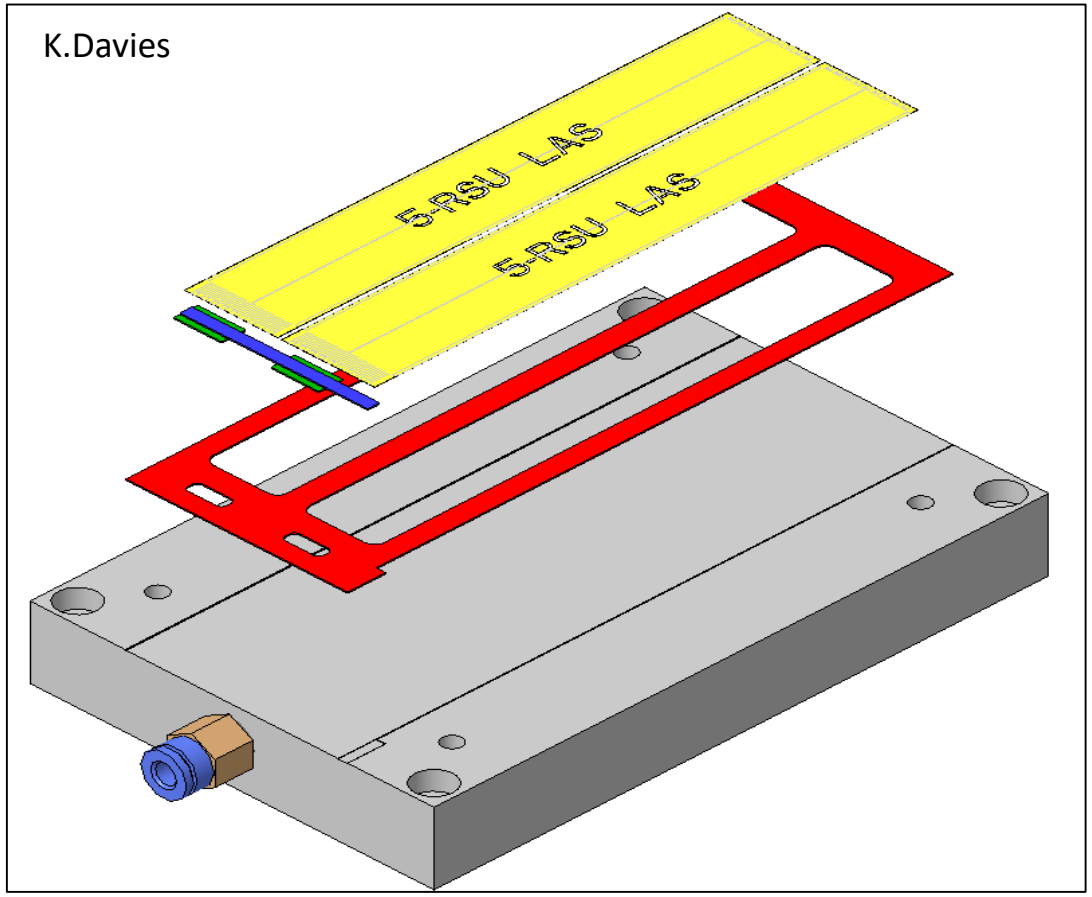
- To rent higher spec equipment:
  - Lecroy WaveMaster8330HD 33GHz scope (33 GHz, 12 bits, 160 GS/s, 200 Mpts)
  - Lecroy WavePulser40iX 40GHz TDR instrument
- Discussed first month free of charge with supplier.

Conclusion

- Characterization of FPCs will start in the new year.
- Valuable learning from the design and procurement stage.
- Currently learning on how to spTAB the FPCs to their interface cards.
- Starting to work on the definition stage of the next FPC iteration (module)



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