# Vertex Detector at CLIC

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# Outline

- Requirements
- Simulation layouts
- Performance optimisation
- Integration, assembly and cooling
- Sensor- and readout-technology R&D

Occupancies and radiation exposure:
→ André Sailer's presentation on backgrounds

# Requirements

- Integral part of tracking systems (in particular for low $p_T$)
- Efficient tagging of heavy quarks + tau leptons through precise determination of displaced vertices:

$$\sigma(d_0) = \sqrt{a^2 + b^2 \cdot \mathrm{GeV}^2/(p^2 \sin^3\theta)}$$

$$a \approx 5\mu m \quad b \approx 15\mu m$$

→ Good single point resolution: $\sigma_{SP}$~3 µm

→ Low material budget: X $\lesssim$ 0.2% $X_0$ / layer (incl. cooling)

- Full coverage down to low polar angles $\theta_{min}$~7°
- Few % occupancy despite large background rates
- Time stamping with 5-10 ns accuracy, to reject background

- To date: no technology option available fulfilling all requirements

→ Simulation studies: impact of layout on performance

→ Integration/Assembly + cooling

→ Discuss ongoing and future R&D on sensors & readout

# Simulation layout CLIC_ILD

Fig. 4.1a

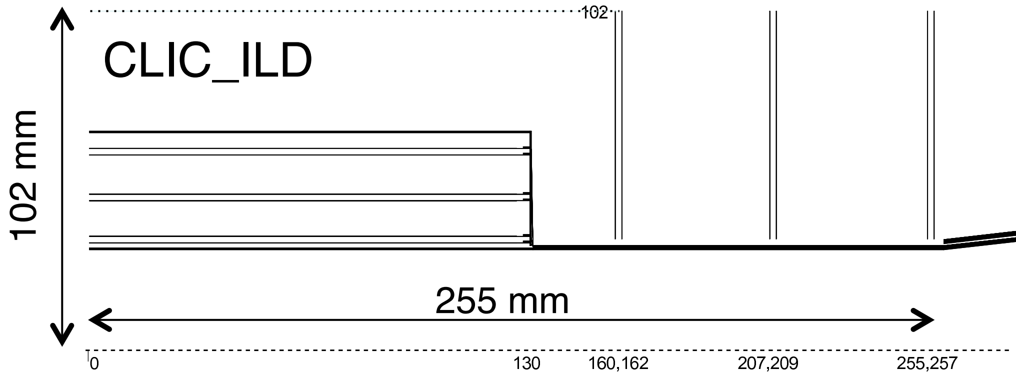
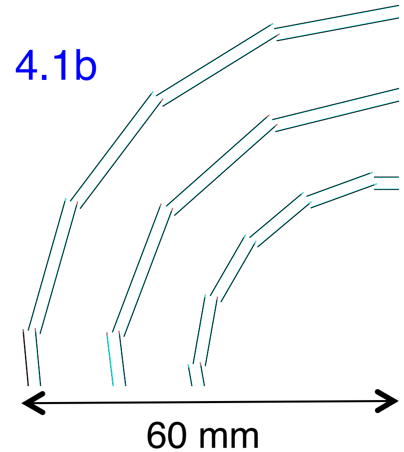



Fig. 4.1b




Tab. 4.1

| | CLIC_ILD | CLIC_SiD |
|---|---|---|
| Central beam pipe | Beryllium | |
| | $R_i = 29.4$ mm<br>$d = 0.6$ mm | $R_i = 24.5$ mm<br>$d = 0.5$ mm |
| Barrel region | 3 double layers<br>$\|z\| < 130$ mm<br>$R_i = 31,\ 44,\ 58$ mm | 5 single layers<br>$\|z\| < 98.5$ mm<br>$R_i = 27,\ 38,\ 51,\ 64,\ 77$ mm |
| Forward region | 3 double layers<br>$z = 160, 207, 255$ mm | 7 single layers<br>$z = 120, 160, 200, 240,$<br>$280, 500, 830$ mm |
| Sensors | 20 µm × 20 µm, $\sigma_{sp} \approx 3$ µm | |
| | $X/X_0 = 0.18\%$<br>per double layer | $X/X_0 = 0.11\%$<br>per single layer |
| Surface area | 0.736 $m^2$ | 1.103 $m^2$ |
| Number of channels | $1.84 \times 10^9$ | $2.76 \times 10^9$ |

# Simulation layout CLIC_SiD

Fig. 4.2a

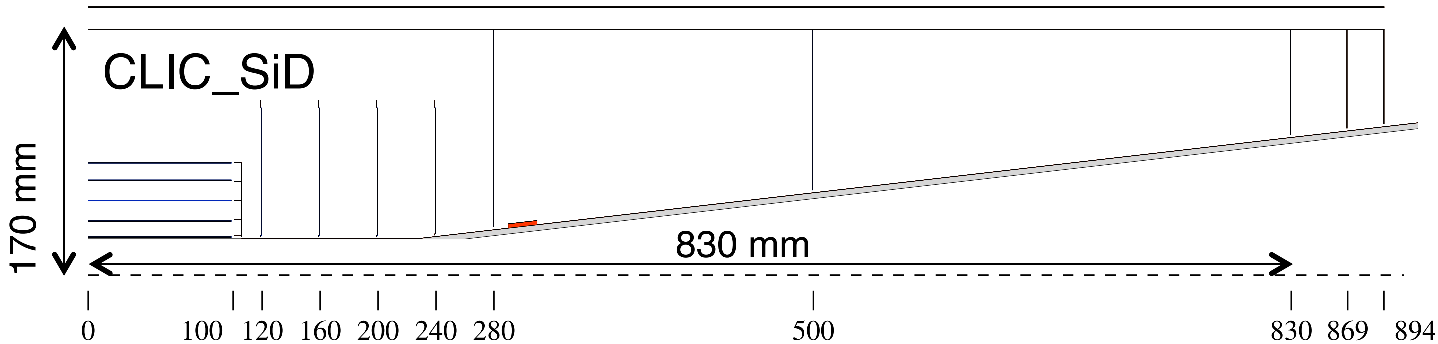
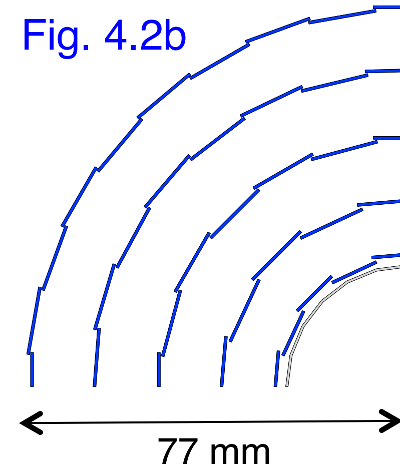



Fig. 4.2b

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# Material budget vertex region

Fig. 4.3a

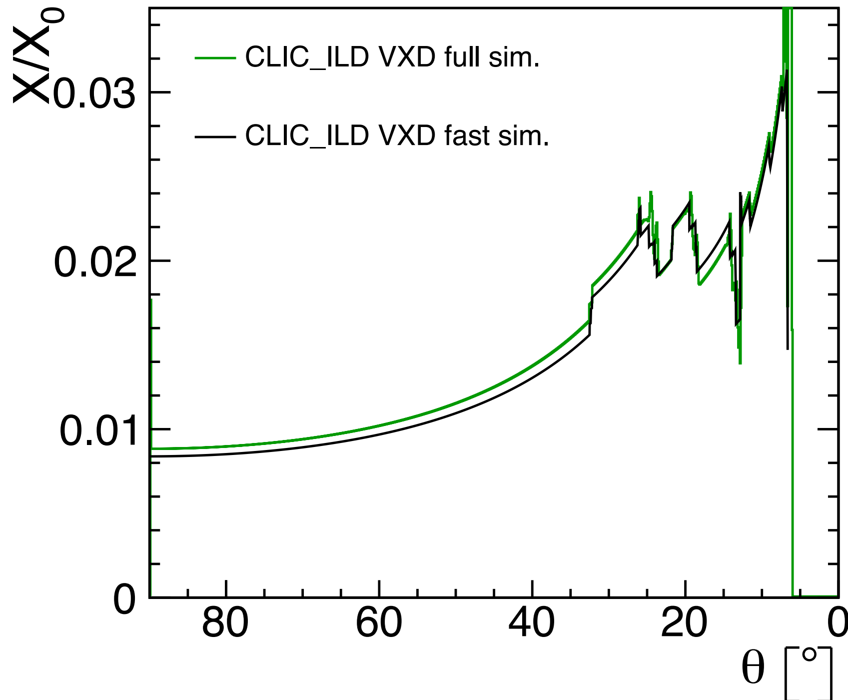
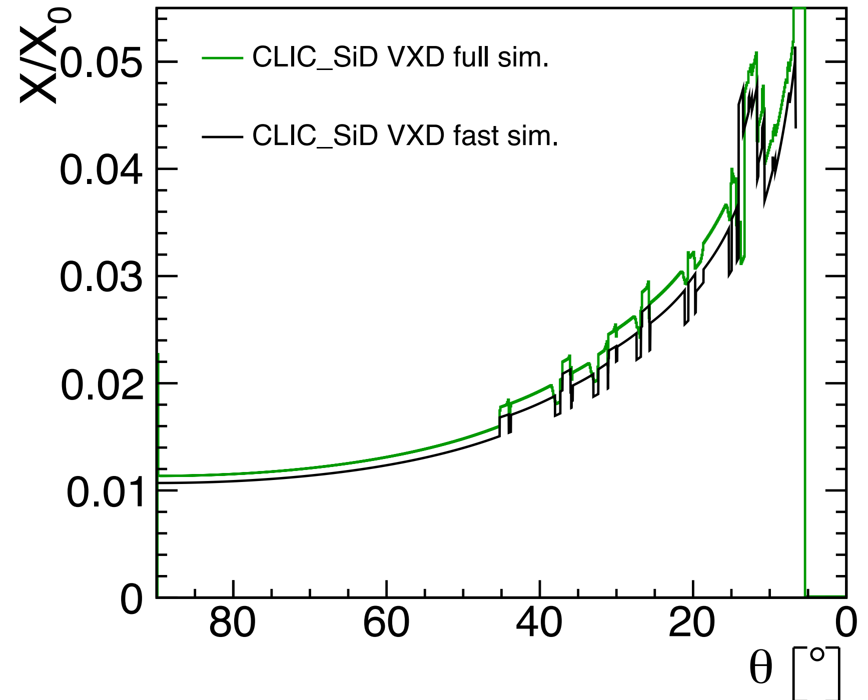



Fig. 4.3b




- Integrated amount of material seen by particles originating from the IP:
  $X/X_0 \sim 1\%$ (at $\theta=90^o$, averaged over $\phi$)
- Good agreement full / fast simulation
  (fast simulation has only ideal cylinders and disks, no module overlaps)

# Transverse impact-parameter resolution

$d_0$: distance of closest approach to interaction point in R-phi plane
→ main benchmark parameter for vertex detector performance

Fast simulation: LiC detector toy tool, used for design optimisation

Full simulation: Geant4-based ILD/SiD frameworks, used for physics studies

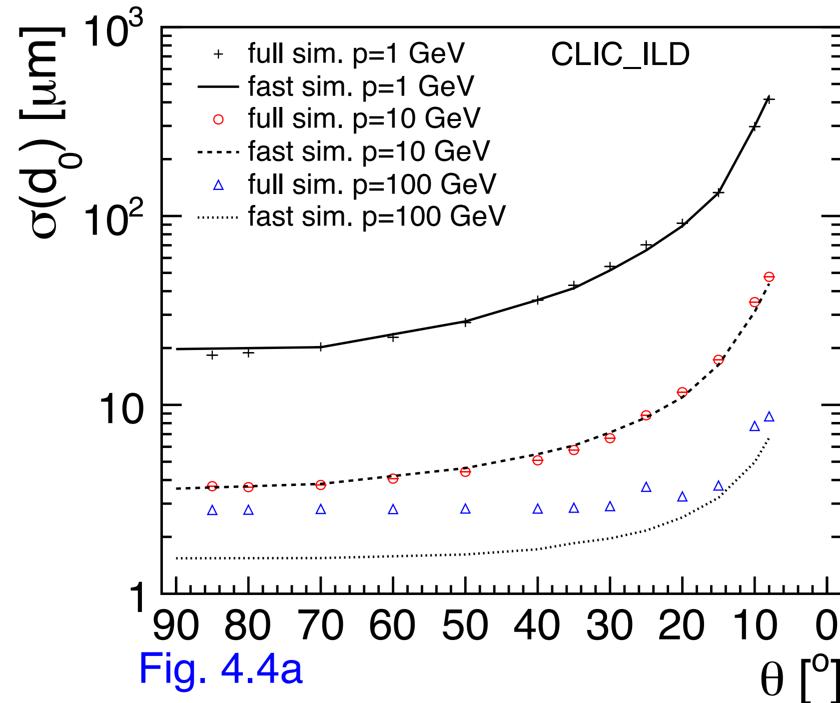


Fig. 4.4a

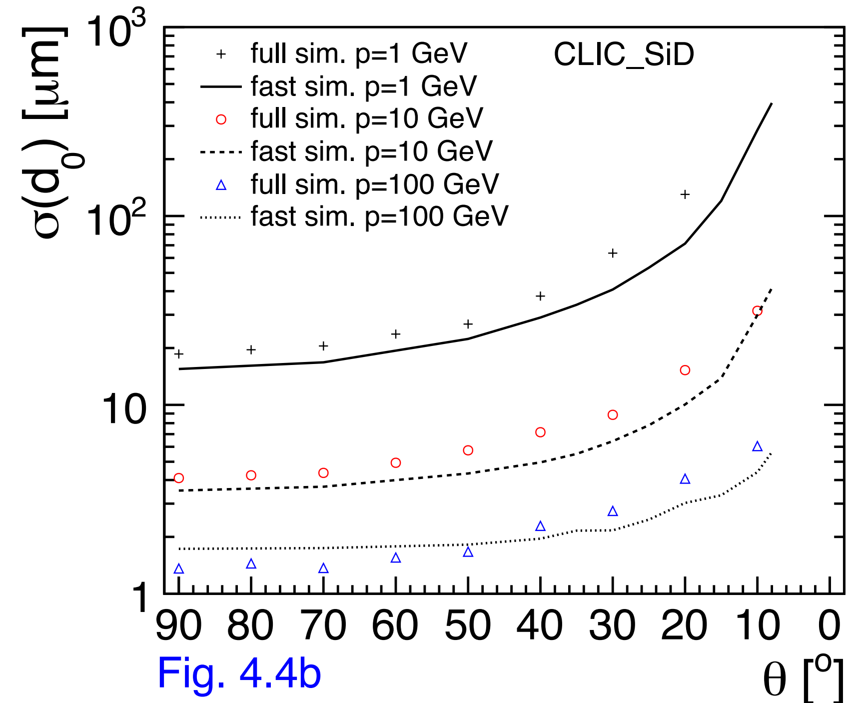


Fig. 4.4b

**CLIC_ILD:**

- Both full and fast simulation perform simple Gaussian hit smearing
- Full simulation without TPC information
  → Worse resolution for high momenta

**CLIC_SiD:**

- Full simulation models clustering according to parametrisation of KPiX readout chip
  → added realism leads to worse resolution in full simulation, as expected

# Dependence on single-point resolution

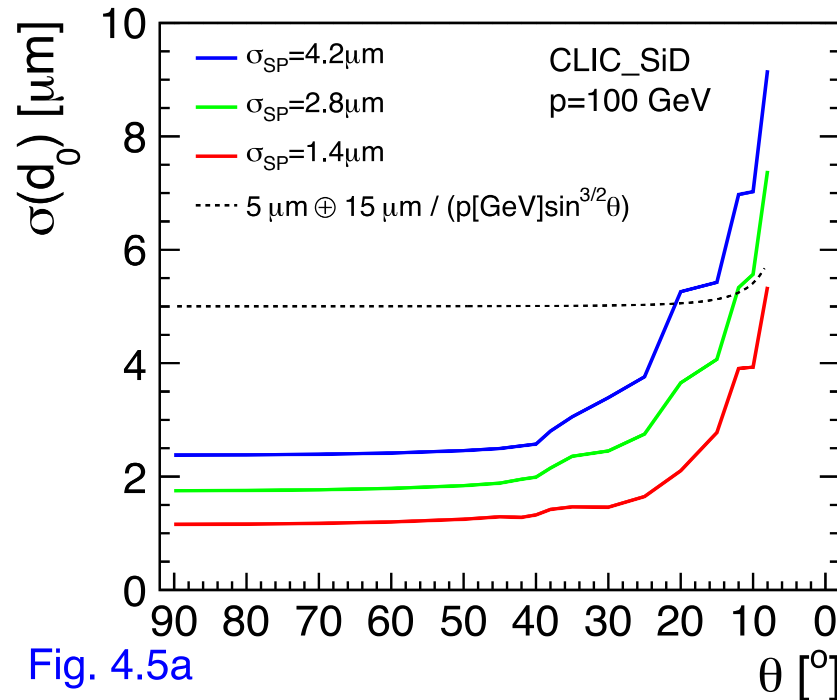



Fig. 4.5a

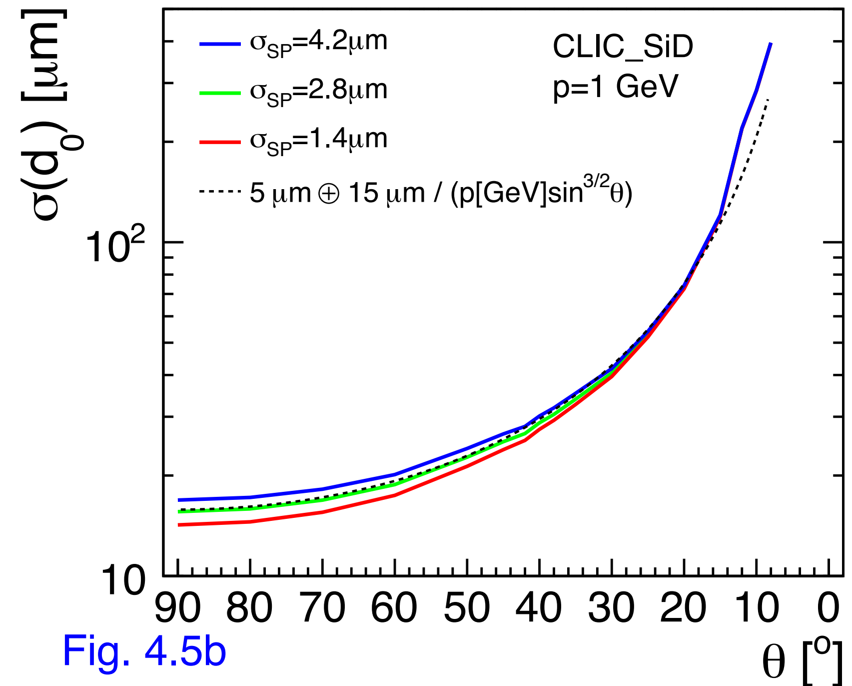
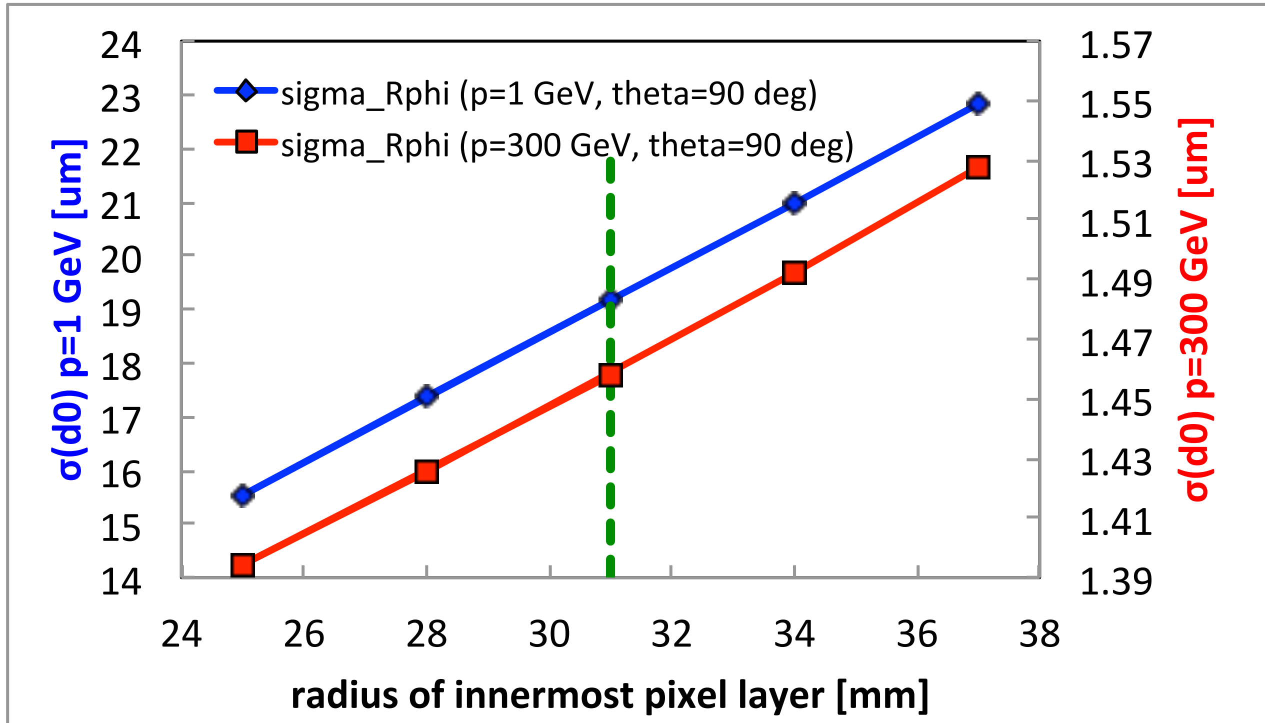



Fig. 4.5b

- Varied single-point resolution by +- 50% (~ pixel sizes 10x10, 20x20, 30x30 $\mu m^2$)
- Observed change in $d_0$-resolution:
  - +- 40% for p = 100 GeV
  - +- 15% for p = 1 GeV
- Resolution close to or better than target values for all cases
- Pixel size is also constrained by:
  - Expected background occupancy
  - Ability to separate adjacent tracks in dense jets

# Dependence on distance to IP

Fig. 4.6




- Varied distance to interaction point, by changing radii of beam pipe and barrel vertex layers in CLIC_ILD model
- Observed change in $d_0$-resolution:
  - 3.2% / mm for high momenta (parameter ‘a’)
  - 0.8% / mm for low momenta (parameter ‘b’)
- Distance to interaction point is constrained by direct hits from incoherent pairs (see André Sailer’s presentation on backgrounds)

# Dependence on material

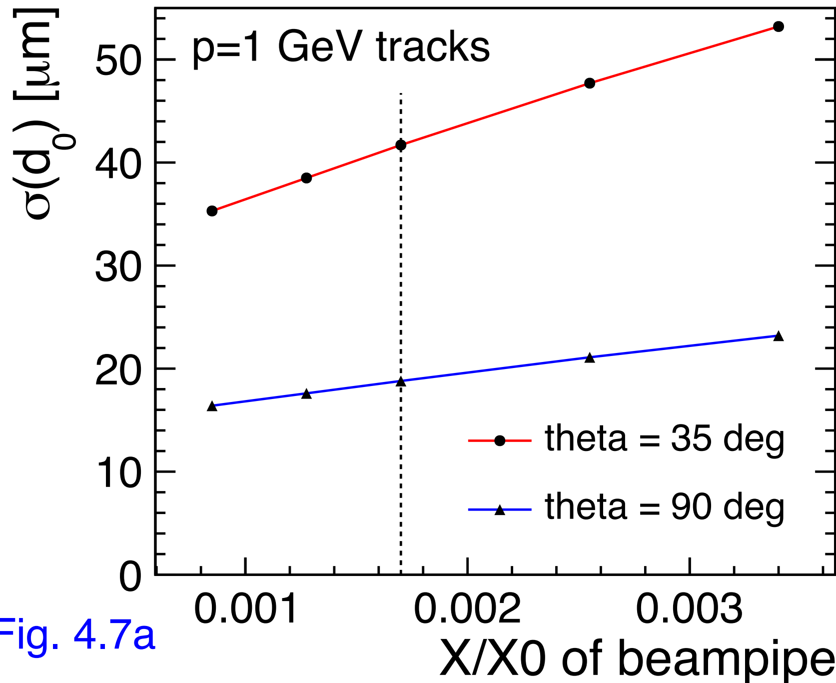


Fig. 4.7a

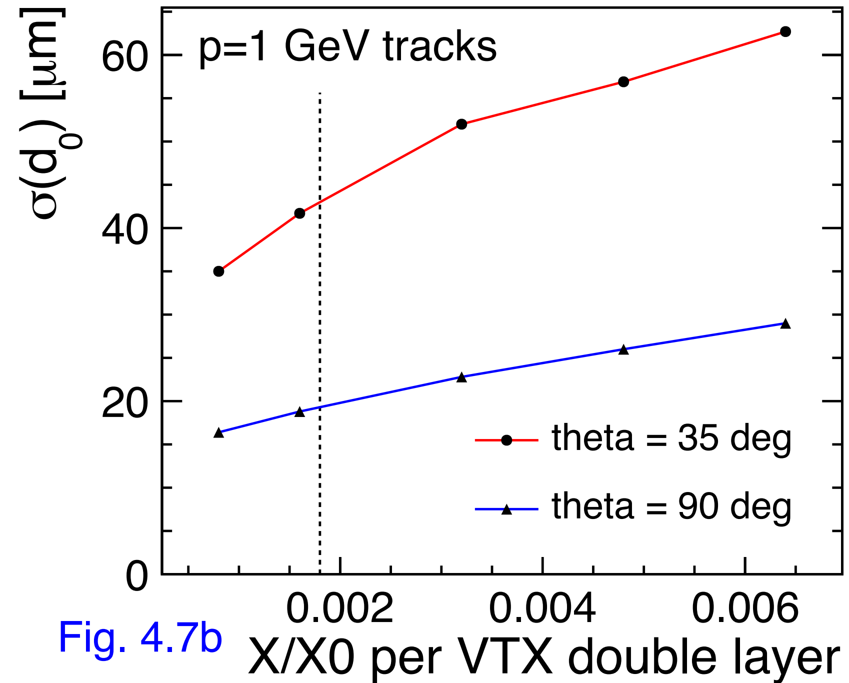


Fig. 4.7b

- Very small amount of material in baseline designs
- Realistic models for supports, cabling, cooling not available yet
- Studied sensitivity of $d_0$ resolution for low momenta on material in beampipe and silicon pixel layers of CLIC_ILD
- Doubling beam-pipe thickness → ~20% worse resolution at 90°
- Doubling material in silicon layers → ~20% worse resolution at 90°
- Steeper slope in forward region

# Beam pipe

Requirements for beam pipe:

- Provide good vacuum → leak tightness
- Minimise multiple scattering → small amount of material in central part
- Allow for placement of Si layers close to IP → small radius
- Stay outside region of high background occupancy → lower limit on radius
- Shield against back scatters from forward region → thick conical part outside VTX acceptance

Implementation in simulations:

- Central Beryllium part:
  - CLIC_ILD: d=0.6 mm, R=29.4 mm (B=4 T)
  - CLIC_SiD: d=0.5 mm, R=24.5 mm (B=5 T)
  - Safe w.r.t. backgrounds, vacuum collapse, leak tightness (D0, CDF experience in run II)
  - Unlike ILC: no extra shielding, due to low expected levels of incoh. synchrotron radiation (t.b.c.)
- Forward conical part:
  - 4 mm iron, to shield against back scatters from forward region
  - Pointing to interaction point → no extra material inside tracking acceptance

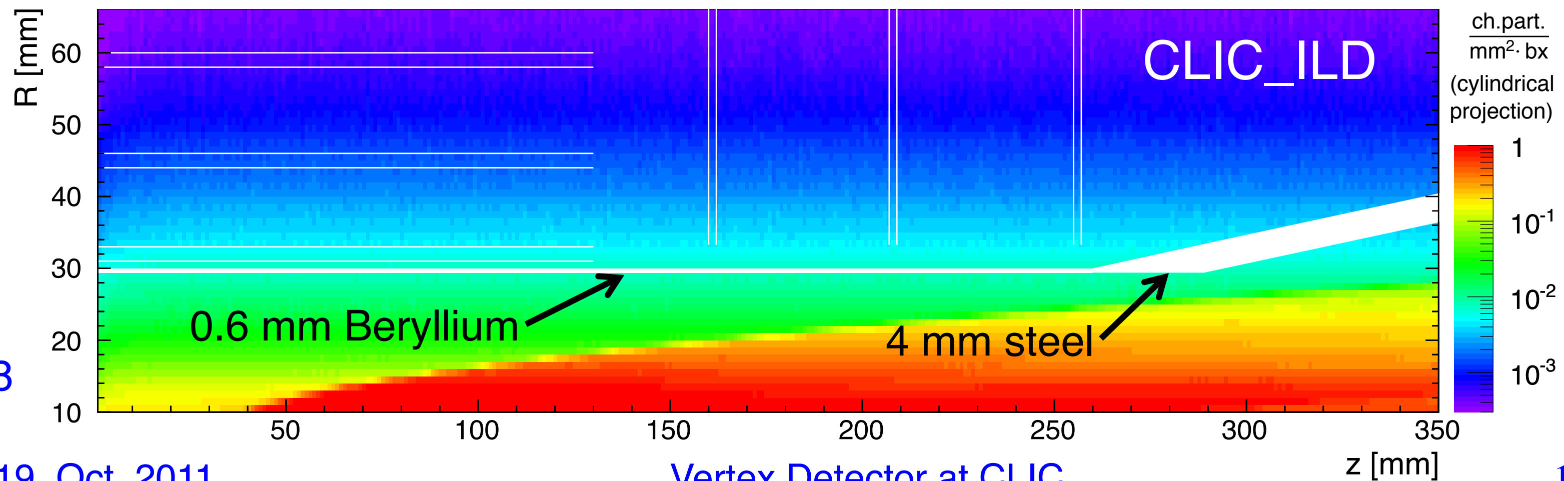



Fig. 4.8

# Assembly and Integration (CLIC_SiD)

Fig. 4.10

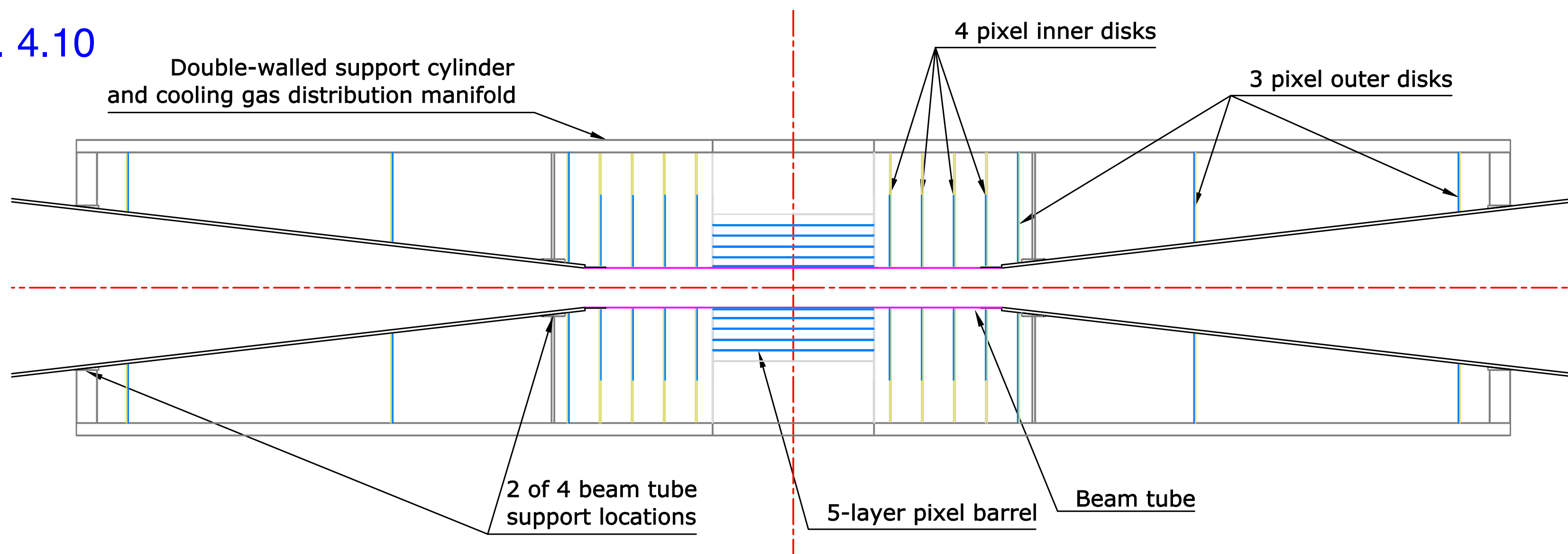
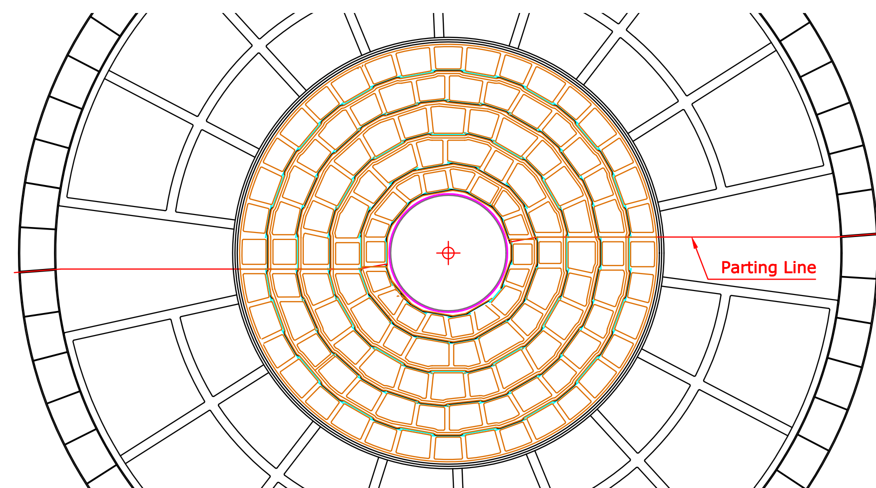



Fig. 4.11




- Assembly in two halves
  → separation from beam pipe assembly
- Double-walled carbon fibre outer support cylinder + support disks
  - supported by conical part of beam pipe
  - Keep central part of beam pipe straight
- Longitudinal passages for cooling gas
- Sensor assembly to be defined:
  - glued to each other or glued to CF support
- CF end rings to control roundness
- Spoked CF membranes to connect layers

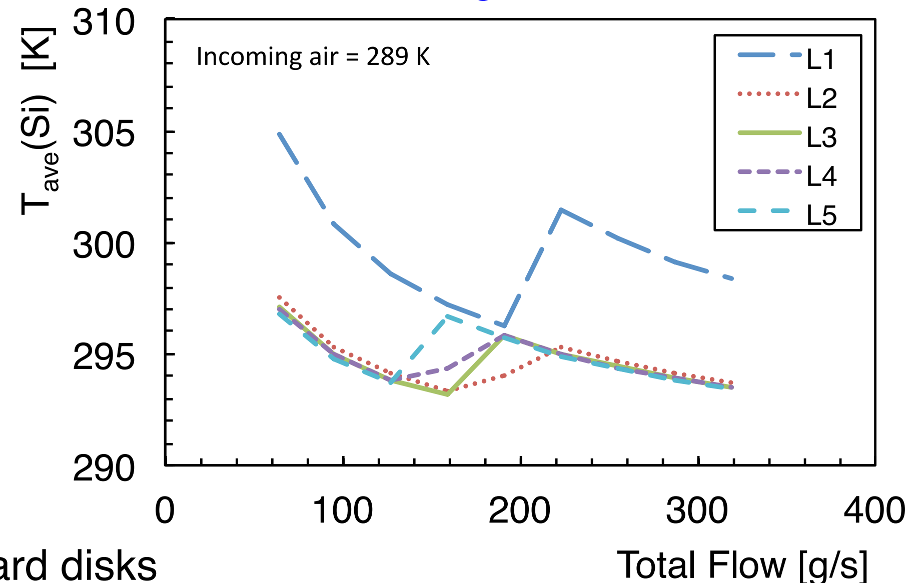
# Cooling

- P~500 W in vertex detectors (50 mW/cm$^2$)
- Need efficient cooling, meeting material budget requirements

**Forced (dry) air flow**

- baseline for barrel region
- no extra material
- CLIC_SiD calculation: $T_{in}$=16°C, $T_{ladders}$~25°C → up to **240 liter/s** flow, ~**40 km/h** flow velocity
- Innermost layer critical
- Possible improvements: lower $T_{in}$ and/or allow for higher $T_{ladders}$

Fig. 4.12




**Evaporative $CO_2$ cooling**

- Option for supplementary cooling in forward disks
- High pressure up to ~70 bar, requires rather thick tubing
- ~2.7 % $X_0$ per tube (incl. coolant)

**Water cooling**

- Option for supplementary cooling in forward disks
- Sub-atmospheric pressure
- Can use thin PEEK pipes → lower material budget than $CO_2$, ~0.4% $X_0$ per tube

**Micro-channel cooling**

- Ongoing R&D (e.g. NA62 Gigatracker upgrade)
- Integrate cooling channels in Silicon
- Connectors pose major challenge

# Pixel-detector technology options

- 20x20 μm$^2$ pixel sizes → need small feature sizes
- Time-stamping ~5-10 ns → need high-resistivity sensor
- ~0.2% material/layer → corresponds to ~200 μm silicon (incl. support + cables)
- 156 ns bunch train every 20 ms → trigger-less readout, power pulsing
- Radiation exposure <$10^{11}$ $n_{eq}$/cm$^2$/yr → radiation hardness not a major concern

**Possible technology development paths:**

1) **Hybrid or multi-tier technologies**
- Thinned high-resistivity fully depleted sensors
- Fast, low-power highly integrated readout chip
- Low mass interconnects
- Pros: factorisation of sensor + readout R&D; r/o chips profit fully from advancing industry standards
- Cons: interconnect difficult/expensive; harder to reduce material

2) **Integrated technologies**
- Sensor and readout combined in one chip or 3D integration of multiple tiers
- Charge collection in epitaxial layer (typically < 1 μm)
- Pros: allows for very low material solutions; synergy with R&D for ILC detectors
- Cons: harder to achieve good time resolution and sufficient S/N

# Examples for Hybrid Approach

- Thinned high-resistivity fully depleted sensors
  - ALICE pixel upgrade: 50 μm silicon sensors (IZM)
  - Handling is a concern, in particular for larger structures

- Fast, low-power readout ASICs in Very-Deep-Sub-Micron (VDSM) technology
  - Timepix3: 55 $\mu m^2$, 130 nm
    → CLICPix (prototypes ~2014): 20 $\mu m^2$, 65 nm
  - ALICE1LHCb r/o chip: 50x425 $\mu m^2$, 250 nm
    → upgrade (prototypes ~2012-13): 30x30 $\mu m^2$, 130-180 nm

- Low-mass interconnects and pixel connectivity
  - Through Silicon Vias (TSV):
    - fan out ASIC contacts to backside through vertical conducting channel
    - avoids dead areas from wire-bonding pads around the chips
    - Implem. example: CEA-Leti (Medipix3, prototypes 2011-12)
  - 3D interconnects
    - Interconnection of separately optimised tiers in different technologies
  - Lateral interconnectivity
    - Edgeless sensors
    - Stitching of CMOS arrays

# Examples for Integrated Approach

- Active R&D programs for integrated technologies, targeted to ILC requirements
- Attempts to reach faster signal collection and ~ns time-stamping capability, compatible with CLIC requirements:
  - MIMOSA CMOS chip family (currently 350 nm) in STAR, EUDET Telescope
    → developing high-resistivity epitaxial layers, smaller feature sizes
  - Chronopixel CMOS sensors with fully depleted epitaxial layer
  - INMAPS technology: deep p-well barrier protects n-well charge collector, improves charge collection, allows for high-resistivity epitaxial layer and full-featured CMOS MAPS technology
  - High-voltage CMOS: CMOS signal processing electronics embedded in reverse-biased deep n-well that acts as signal collecting electrode
  - Silicon-On-Insulator (SOI): ~200 nm $SiO_2$ isolation layer separates charge collection and readout functionality
  - Full 3D-integrated pixel solutions: Thinned high-resistivity sensitive tier coupled to additional tiers with advanced analog+digital functionality

- Concerns for CLIC:
  - Long-term availability of processes
  - Suitability for large-scale systems

  → prefer staged developments and synergy with industrial trends

# Future Work

- Simulation, Layout + Integration:
  - Improve realism of simulation for digitization / reconstruction (signal development, clustering, charge sharing, resolution, angular dependence, single-event effects, etc.)
  - Improve models for cabling / supports / cooling
  - Develop low-mass support structures
  - Work out assembly, integration and access scenarios
  - Strengthen link to physics requirements: heavy flavour tagging, benchmark studies involving forward physics
  - Re-optimise geometry in view of all of the above

- Sensor + Readout R&D:
  - Develop pixel detector with small pitch (~20 μm) and fast time stamping of hits (~5 ns)
    → Hybrid or multi-tier
    → Integrated CMOS technologies
  - Low-mass interconnects for vertical and lateral integration
  - Thinning of wavers to ~50 μm
  - Power delivery and power reduction techniques ($P \lesssim 50$ mW / cm$^2$)
    → Power-pulsing + air cooling in magnetic field

# Summary / Conclusions

- CLIC environment + physics requirements pose challenging demands on vertex-detector systems
- Presented initial layout proposals meeting those demands
- Studied dependence of performance on layout parameters
- Integration, Assembly and Cooling considerations
- Examples for active R&D on sensor + readout technologies, aiming to meet the CLIC requirements