CLIC electronics chapter

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presented by A. Kluge

October 19, 2011

Outline

- Aim of chapter
- Overview of detector readout channels
- Implementation options for few subdetectors
- Powering scheme
- DAQ aspects
- Summary

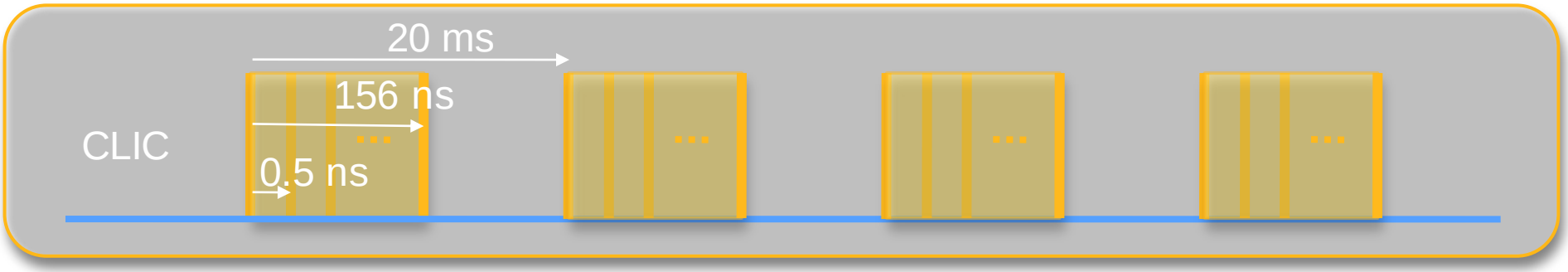
Aim of chapter

- Overview of detector readout requirements
- Verifies consistency of requirements
- Evaluates principle implementation feasibility
- Summarizes priority areas for further research and development

Introduction

- Electronics requirements resemble
  - LHC detectors for
    - pile-up and time stamping aspects with more precision
  - ILC detectors
    - for trigger-less readout
    - high channel count
    - low material budget
    - power pulsing aspects
    - Radiation similar to situation at ILC (factor 10^4 lower than LHC)

Introduction



- 0.5 ns time separation between bunch crossings
- sequence of 312 bunch crossings in train
  - → 156 ns long bunch train
- bunch train repetition each 20 ms

5 detector categories with similar readout specifications

- Silicon pixel detectors
  - Arrival time for 1 hit readout per train
  - Zero suppression
- Silicon strip detectors
  - Arrival time for >1 hits per train
  - Sampling of pulse at regular interval
  - No zero suppression due to the large occupancies
- TPC
  - Analog pad readout for 1000 voxels per channel
- Calorimeters
  - Arrival time for >1 hits per train
  - Sampling of pulse at regular interval
  - Pulse heights higher than strip detectors → time resolution
  - No zero suppression
- Muon detectors
  - Digital readout of > 1 hits per train with a multi-hit TDC
  - Zero suppression

CLIC_ILD

time stamping resolution [ns]	time sampling period [ns]	cell size [mm^2]	number of channels [10^6]	average to maximum occupancy per train [%]	number of bits per hit [bit]	data volume [Mbyte]

Safety factor 5/2 for incoherent pairs/γγ to hadrons, TPC no safety

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FTD strips							
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[b] The 3D TPC reads out 1000 voxels per channel for each bunch train.

Safety factor 5/2 for incoherent pairs/γγ to hadrons, TPC no safety

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Implementation Example: Pixel Detector

- single point resolution: ≈3 µm
- timing precision: 5-10 ns
- pixel sizes: 20 µm × 20 µm
- material budget: 0.2% X0 per layer
- power dissipation: 50 mW/cm² with power pulsing

Implementation Example: Pixel Detector

- several technologies considered
  - → example based on a hybrid pixel detector and Timepix1 ASIC
- ASIC 512 × 512 pixels with 20 µm × 20 µm
  - each pixel
    - 4 bit arrival time measurement (16 time-slices of 10 ns)
    - 4 bits Time-Over-Threshold (TOT) measurements
    - clock = time binning of 10 ns (100 MHz)
  - Zero- suppressed data readout between trains
  - Vertex Barrel:
    - Occupancy 1%, → 56 Megabytes per bunch train
  - ≤ 65 nm CMOS technology

Implementation Example: Pixel Detector

- Analog circuitry dominant power consumer
  - Expected power of 10 µW/pixel → 2.5 W/cm²
- power pulsing factor of ≈50 → 50 mW/cm²
  - analog part on during 40 µs per bunch train
  - digital part on ~ 400 µs
- Data flow
  - → 50 Mbyte/s instantaneous data transfer rate during digital power-on time
- Material budget
  - sensor thickness
    - → minimum detectable charge, preamplifier noise
  - detector integration process
  - Research targets Through-Silicon Vias (TSV)
    - for both hybrid pixel detectors and integrated CMOS detectors.

Implementation Example: TPC Pad Readout

- drift length 2.25 m →
  - maximum drift time ≈ 30 μs, depending on gas mixture
- end plates: 1.5 million readout pads of 1 × 6 mm² size
- 40 MHz read out during drift time per pad
- 10-bit pulse height data for 1000 time-voxels per pad
- TPC hit occupancies
  - max 32% of the time-voxels for inner row
  - 1% outer row
  - no safety factors

Implementation Example: TPC Pad Readout

- SAltro readout based on ASIC
  - low-noise programmable amplifier
  - high-speed 10-bit ADC
  - programmable digital filters
  - Current SAltro-16 channels used for qualification of TPC prototypes
  - Current SALTRO first system level TPC power pulsing studies
- In a next phase
  - optimised ADC with a reduced power consumption, smaller surface, more channels
  - power pulsing
  - reduced power consumption
- An alternative TPC readout scheme using 55 µm × 55 µm pixels is also under study

Implementation Example: Analog Calorimeter Readout

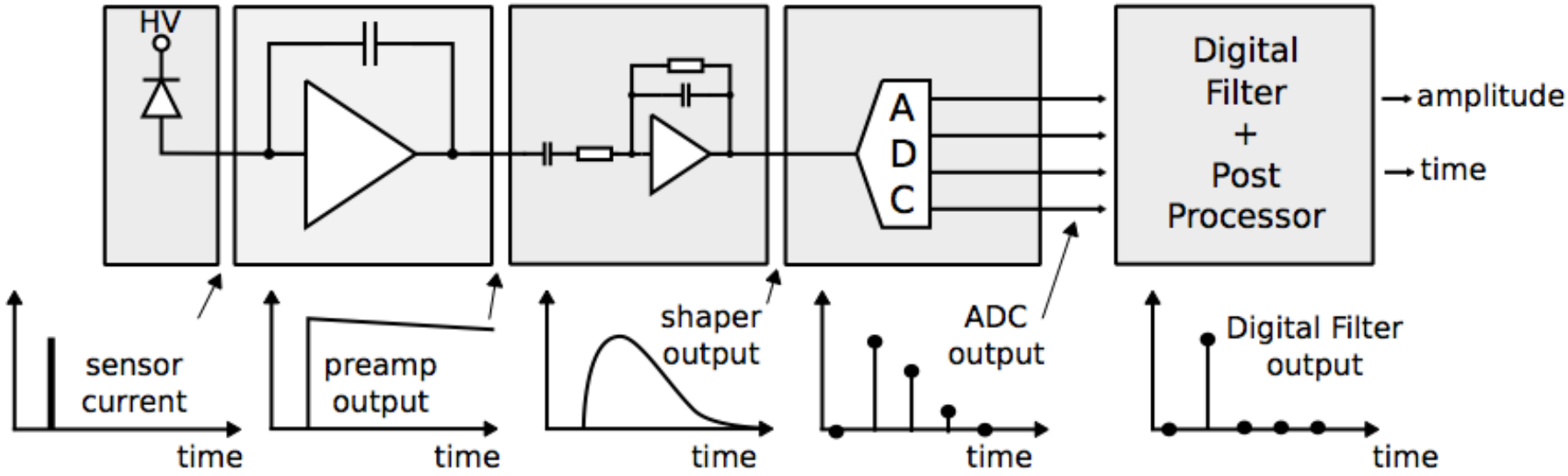
- ECAL dynamic range 12 bits
- HCAL dynamic range 14 bits
- Time resolution 1 ns (shower start)
- Occupancies high in forward regions
  - max 150% ECAL occupancy (5×5 mm^2)
  - max 5200% HCAL (3×3 cm^2)
- Accommodate up to 5 hits per train in high-occupancy regions

Implementation Example: Analog Calorimeter Readout

- timing and energy information
  - preamplifier-shaper peaking time slower than the time-stamping resolution, pulse length ~ 100 ns
  - digitation at 40 MHz with 14-16 bits

- Comparison
  - ATLAS liquid argon calorimeter electronics samples at 40 MHz
  - Overall hit time resolution <1 ns was at system level

Implementation Example: Analog Calorimeter Readout



Implementation Example: Analog Calorimeter Readout

- Alternative
  - signal stored using fast analog memory
  - digitised at low speed at end of bunch train
  - today fast analog memory option 12-13 bits
  - multi-stage amplification to cover dynamic range

Implementation Example: Analog Calorimeter Readout

- Maximum data rate
  - no suppression (no address bits)
  - 16 bits every 25 ns during bunch train of 156 ns
  - + 100 ns shower development
  - + 100 ns front-end shaping time
- Data transmission
  - 350 ns * 50/second * 120 *10^6 channels = 170 GB/s
  - comparison
    - ATLAS liquid argon calorimeter 1600 1.6 Gbit/s links

Implementation Example: Analog Calorimeter Readout

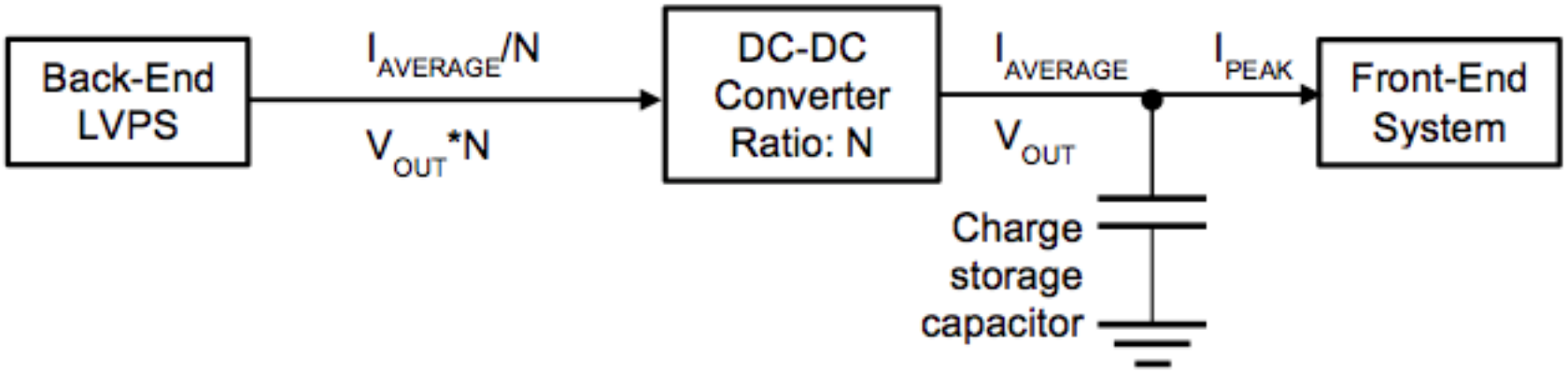
- Power consumption for 40 MHz digitisation option
  - dominated by ADC
  - existing 16-bit 40 MHz ADCs 70 mW per channel during conversion
  - → ~150 kW
- Power consumption for analog memory option
  - low speed ADCs are used → 150 µW per channel at 10 ksamples/s ~150 nW standby
  - →~1.2 kW
    - consumption doubled if a two-gain scheme is used
    - small amount of power needs to be added for the analogue memory

Power delivery & power pulsing

- Motivation
  - high number of channels
  - large masses and volumes for cooling systems and cables
- CLIC beam structure
  - bunch trains 156 ns
  - repeated every 20 ms
  - → duty cycle 7.8 · 10–6 @ 50 Hz

Power delivery & power pulsing

- DC-DC voltage step-down or low drop out (LDO) regulator and capacitor near the front-end
- Powering branch
  - back-end power supply
  - long cables
  - front-end voltage regulator
  - front-end circuits



Power delivery & power pulsing

- Power switching applied selectively to various parts of circuit
  - Analog off most of the time
  - turned on only to acquire hit signal
- Digital and data transmission active during the bunch train gap
- Turning on front-end electronics results in periodic in-rush current (several Amperes)
  - → voltage regulation circuit
- Ideally power gating feature is implemented at the ASIC level
  - Fast turn-on time of few tens of µs (typ 50 µs assumed)
  - Configuration data are permanently maintained

Power delivery & power pulsing

- Peak current delivered by a storage capacitor
  - close to the front-end system
    - voltage drop in example resulting from the charge transfer during the active time 100-200 mV with 5 mF capacitor
- Electrolytic capacitors up to 400 mF are available
  - however they are large

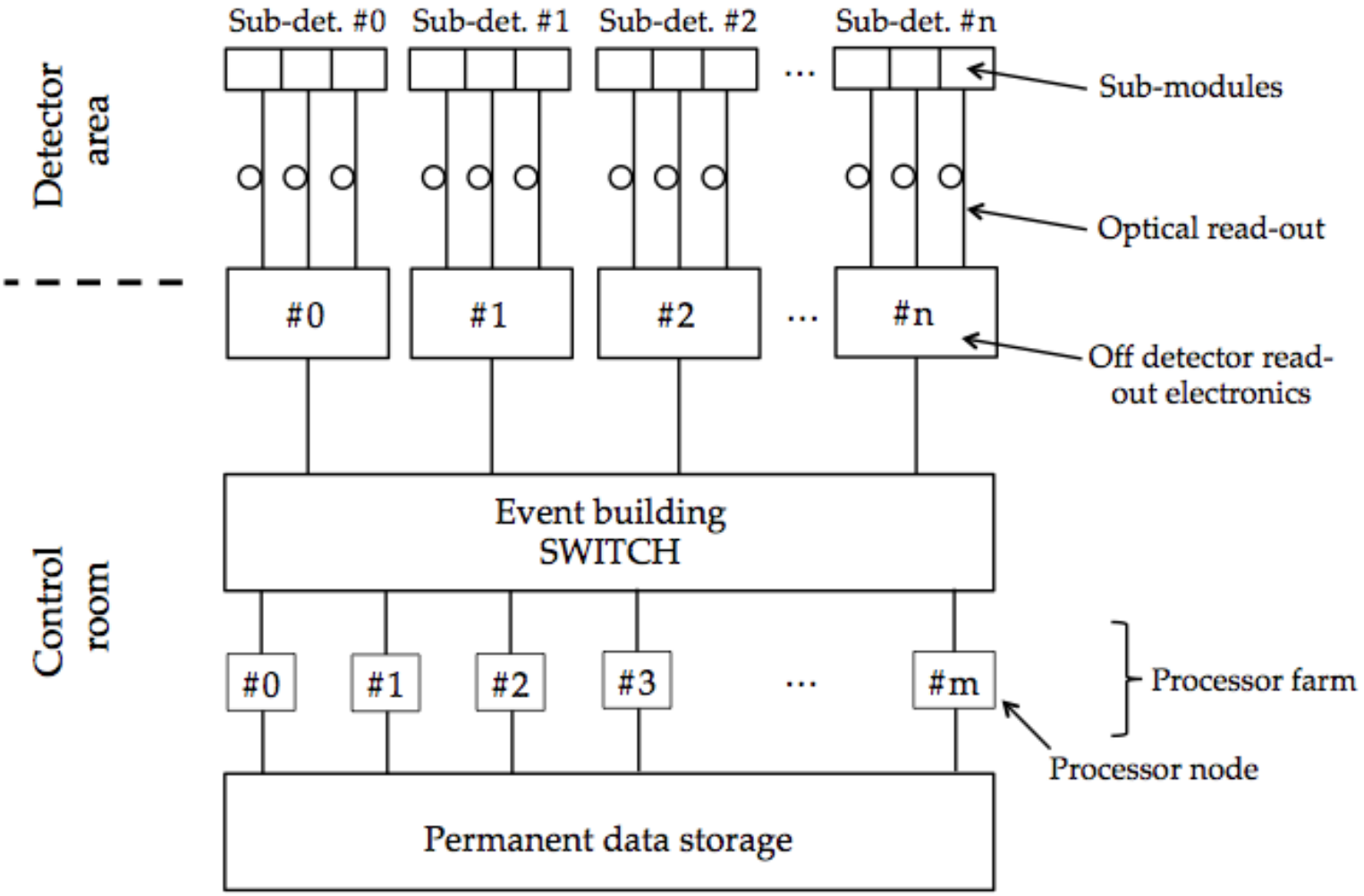
Power delivery & power pulsing

- Initial power pulsing tests applied to ILC calorimetry demonstrated validity of the concept
- Extensive R&D to demonstrate
  - feasibility for application in all subdetectors
  - particular for vertex and tracking

DAQ aspects

- Possible architecture
  - using available technologies for estimate of system dimension
- Ongoing improvement of data communication → new opportunities

DAQ aspects


Sub-det. #0
Sub-det. #1
Sub-det. #2
Sub-det. #n
Detector area
Sub-modules
Optical read-out
#0
#1
#2
#n
Off detector read-out electronics
Event building SWITCH
Control room
#0
#1
#2
#3
#m
Processor farm
Processor node
Permanent data storage

DAQ aspects

- Readout block diagram
  - front-end electronics directly connected to optical links
  - data transferred to off-detector readout system (custom electronics or commodity computers).
    - data concentrated, re-formatted and possibly zero-suppressed
  - event-building switch connected to a processor farm.
- Apart from zero suppression processor farm first place where data is filtered

DAQ aspects

- Total data volume
  - ~4 Gbyte per bunch train → 200 Gbyte/s
- Assuming data link bandwidth of 10 Gbit/s
  - number of links is 160
- Inefficiency
  - detector segmentation and limited connectivity between detector sub-modules
  - power pulsing
- Assume efficiency reduction factor of 10 →
  - effective sustained data rate of only 1 Gbit/s per link →
  - 1600 optical links
  - For comparison, CMS 80000 links

DAQ aspects

- If one off-detector readout processor has
  - 10 optical inputs
  - & 1 output to event-building switch
  - → 160 readout processors
- Switches close to this requirement already exist
  - 160 10 Gbit/s input ports and 300 output ports
  - Depending on number of processors in farm
    - each of ports connected
      - directly to a processor node
      - or via distributor node consisting of a processor and a sub-switch.

DAQ aspects

- Based on current reconstruction algorithms and required CPU time to process a bunch train
  - → estimate number of required processing nodes
- Time for bunch train reconstruction
  - 3000 seconds (Intel® Xeon® E5520 CPU 2.27 GHz 2 Gbyte RAM) →
  - 150000 seconds processing time in a second of beam operation
- Today's technology with four cores per CPU and two CPUs per node
  - ~19000 processing nodes.
  - Comparison: CMS event farm size in 2011, 7500 nodes
    - In online farm full reconstruction not be needed
    - Development of faster online algorithms
    - Improvements in available technology reduce amount of nodes

DAQ aspects

- Data suppression factor studies
  - contributions from $\gamma\gamma \rightarrow$ hadrons events can be reduced by a factor of 10 by dismissing out-of-time hits
  - Identifying hits from incoherent pairs suppress the data volume further by a factor 5 to 10
- Overall reduction of 15-20
  - sustained data rate of ~10 Gbyte/s to permanent storage.
    - Comparison ALICE 2011 5 Gbyte/s to disk.

Summary

- State of detector definition →
  - preliminary specifications for detector front- end and data acquisition systems
- Specifications are driven
  - short bunch crossing interval
  - particle arrival time stamping
  - reduction of material budget
    - silicon tracker system material budget minimisation
    - calorimeter electronics compact in physical space

Summary

- For silicon vertex detectors technologies approaches are available to pursue research to be conducted to define a full system concept
  - research on the sensor and front-end electronics level
  - field of low mass integration
  - interconnect
  - opto-electronics
  - power pulsing
  - cooling needs

Summary

- TPC
  - pad readout and pixel readout are in advanced development
  - next phase pad readout
    - profit from technology trends to achieve reduced power consumption
  - next TPC pixel readout
    - will also have more advanced functionalities on the chip

Summary

- Calorimeter
  - material reduction in active calorimeter systems
    - low power implementations
  - Further R&D for
    - detector layout
    - occupancy
    - front-end signal and shaping time especially in high occupancy regions

Summary

- Power pulsing
  - For all detectors power pulsing
  - Research effort
    - for front-end ASIC
    - power pulsing system level
    - detector specific studies to define feasibility and system requirements
    - inner tracking systems integration issues
      - control communication
      - positioning of the power pulsing

Summary

- Off-detector readout schemes and data acquisition system
  - are manageable and no further research is required at present