

Development of the greatest antimatter detector ever

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and Markus Münster

TUM / FRM II



FRM II
Forschungs-Neutronenquelle
Heinz Maier-Leibnitz

Technische
Universität
München

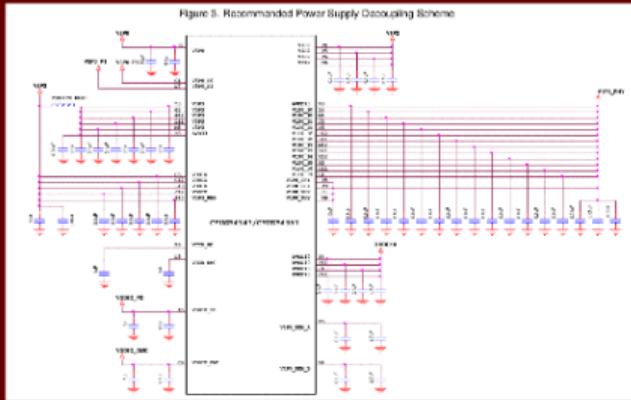
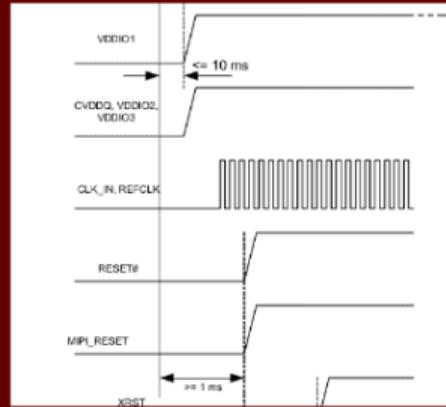
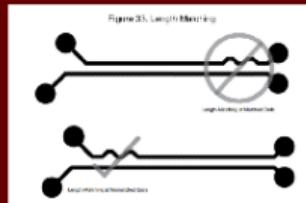


Summary

Summary

CRIME

"Legal" requirements for ICs



19.1

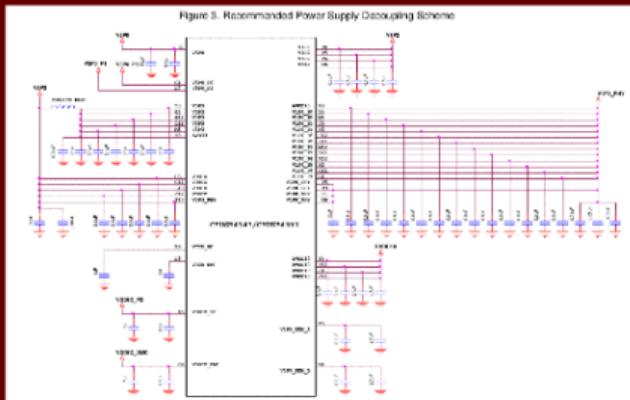
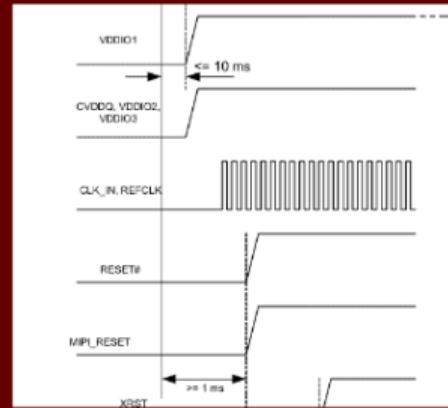
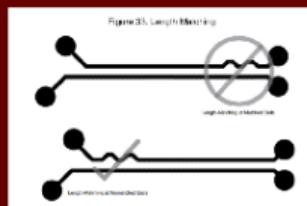
Absolute maximum ratings

Exceeding maximum ratings may shorten the useful life of the device.

Storage temperature	-65°C to +150°C
Supply voltage to ground potential V_{DD}, V_{DDQ}	1.25 V
$V_{DDIO1}, V_{DDIO2}, V_{DDIO3}$	3.6 V
$U3TX_{VDDQ}, U3RX_{VDDQ}$	1.25 V
DC input voltage to any input pin	$V_{CC} + 0.3$
DC voltage applied to outputs in high-Z state (V_{CC} is the corresponding I/O voltage)	$V_{CC} + 0.3$
Maximum latch-up current	140 mA
Maximum output short-circuit current for all I/O configurations. ($V_{OUT} = 0 \text{ V}$)	-100 mA

"Legal" requirements for ICs

But what happens if we disobey?



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"Legal" requirements for ICs

But what happens
if we disobey?

- No functionality
(optionally damage, magic smoke, other general excitement)
- Instability
- Nothing

What are actually these requirements?

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A weapon to argue legal disputes between companies...

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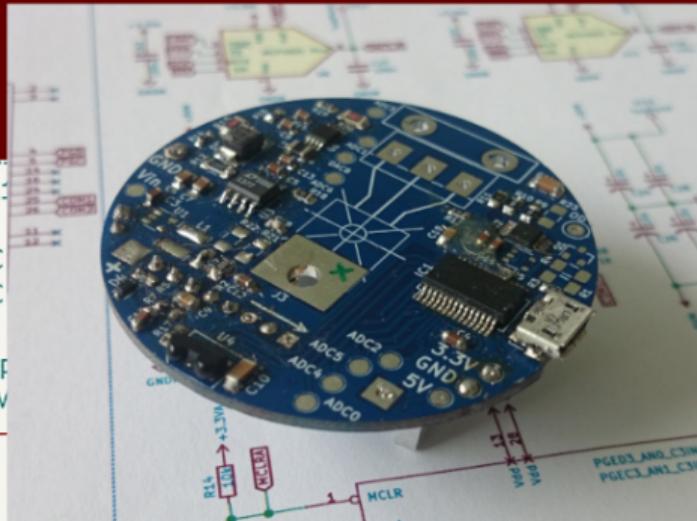
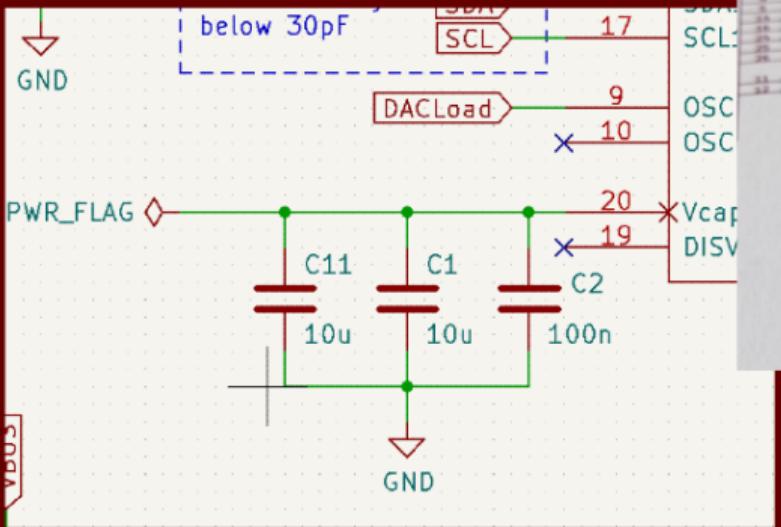
What are actually these requirements?

A weapon to argue legal disputes between companies...

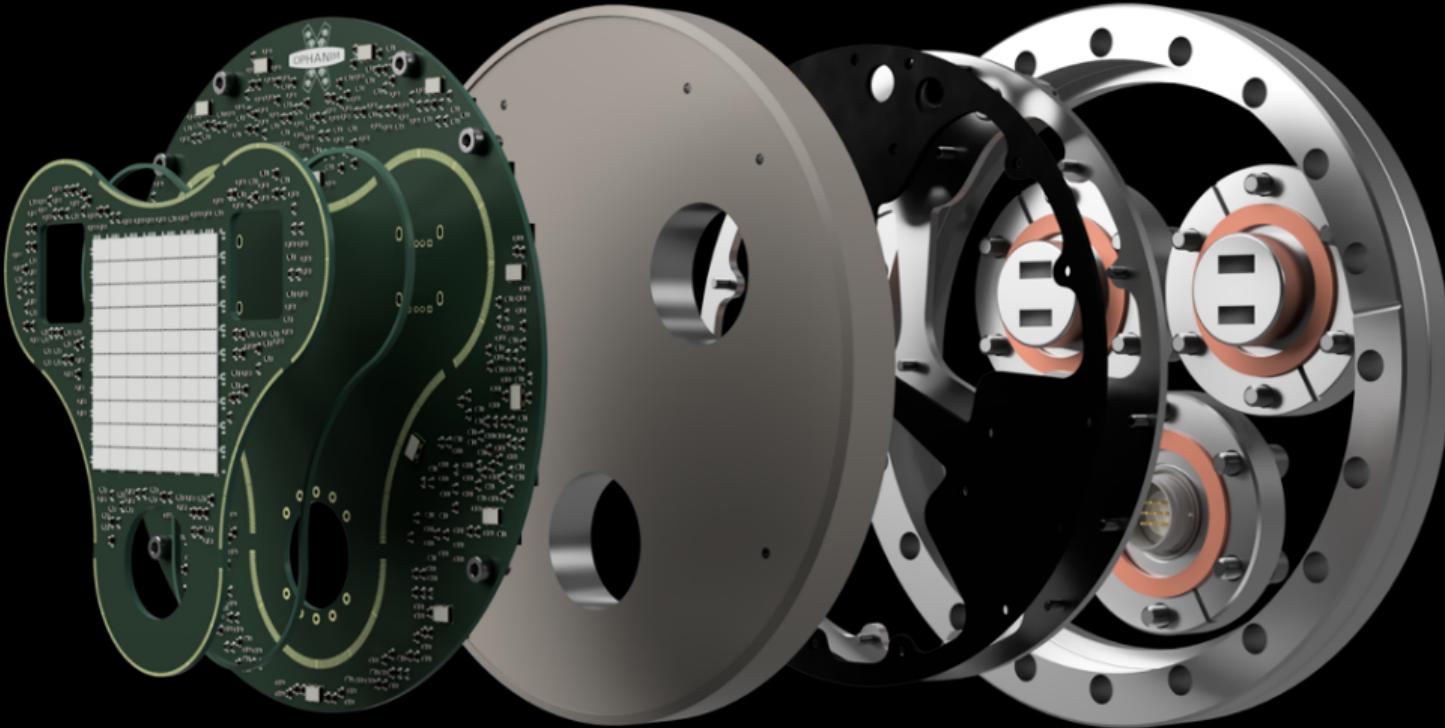


... half of the time. The other half they are actual requirements.

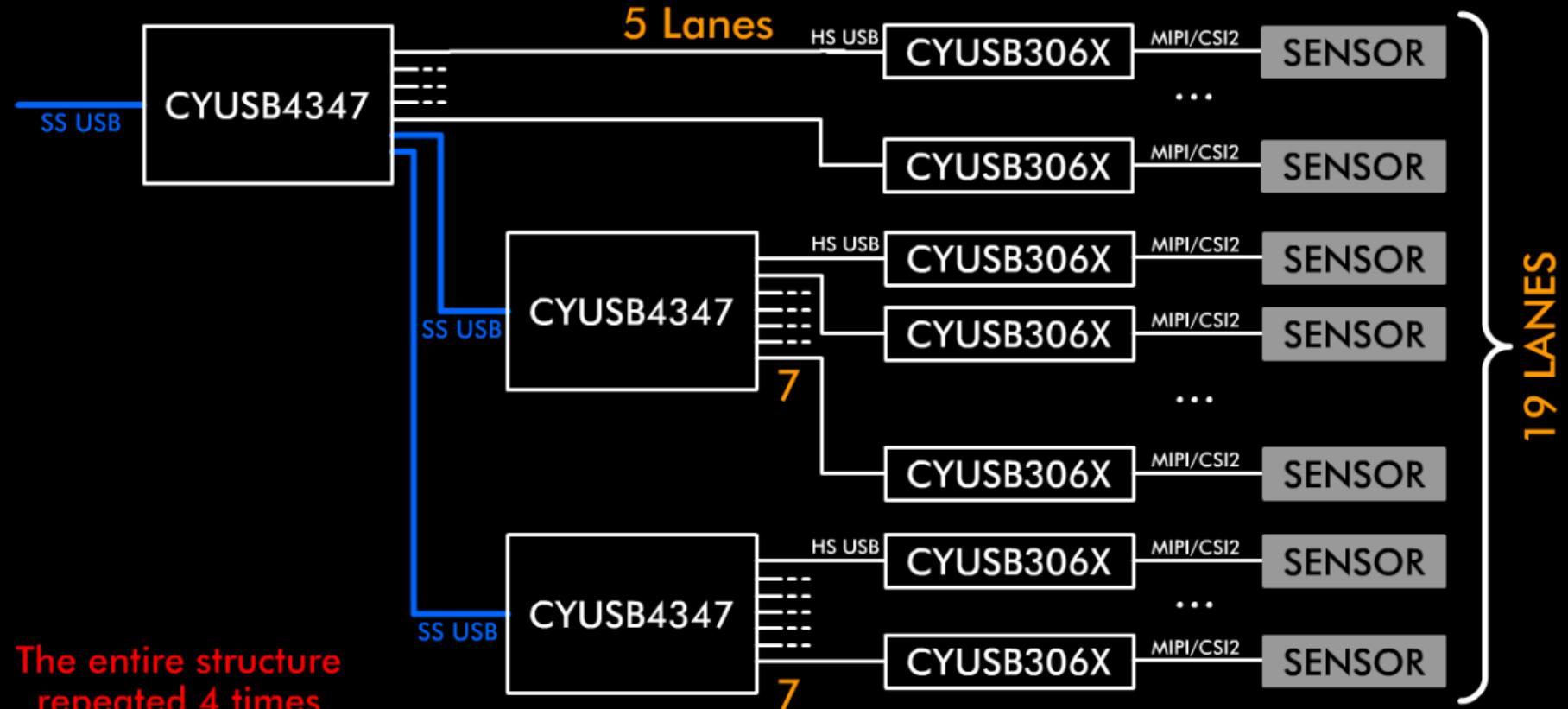
Why disobey?



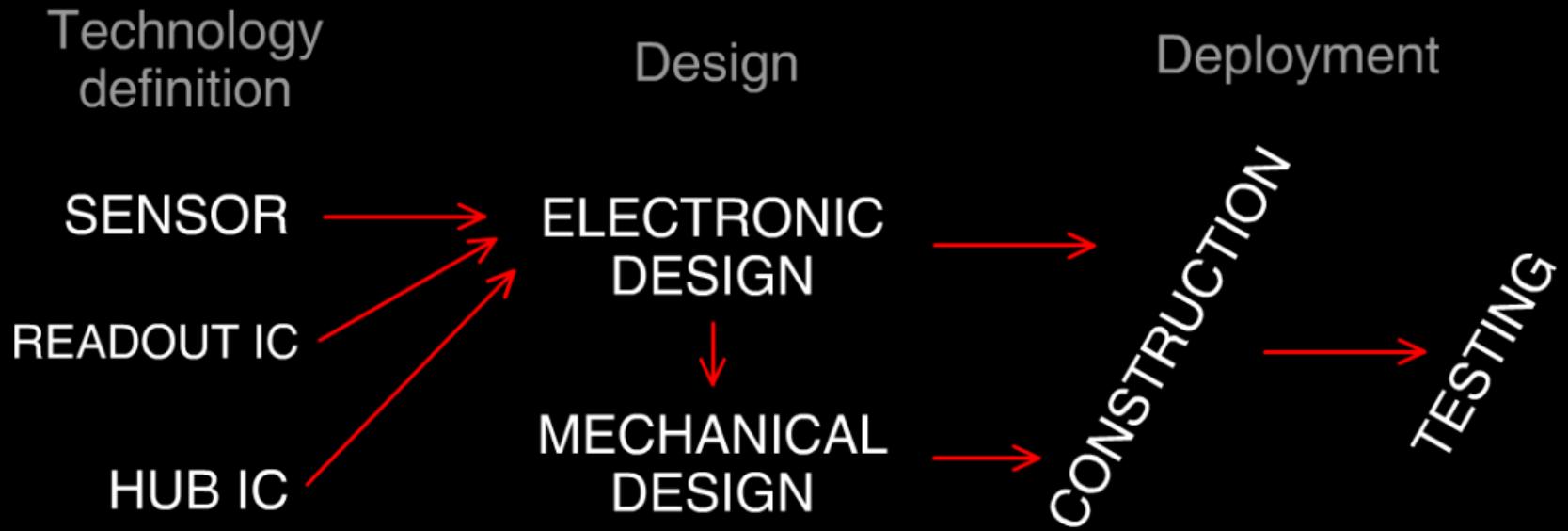
December 2023



December 2023



The big picture

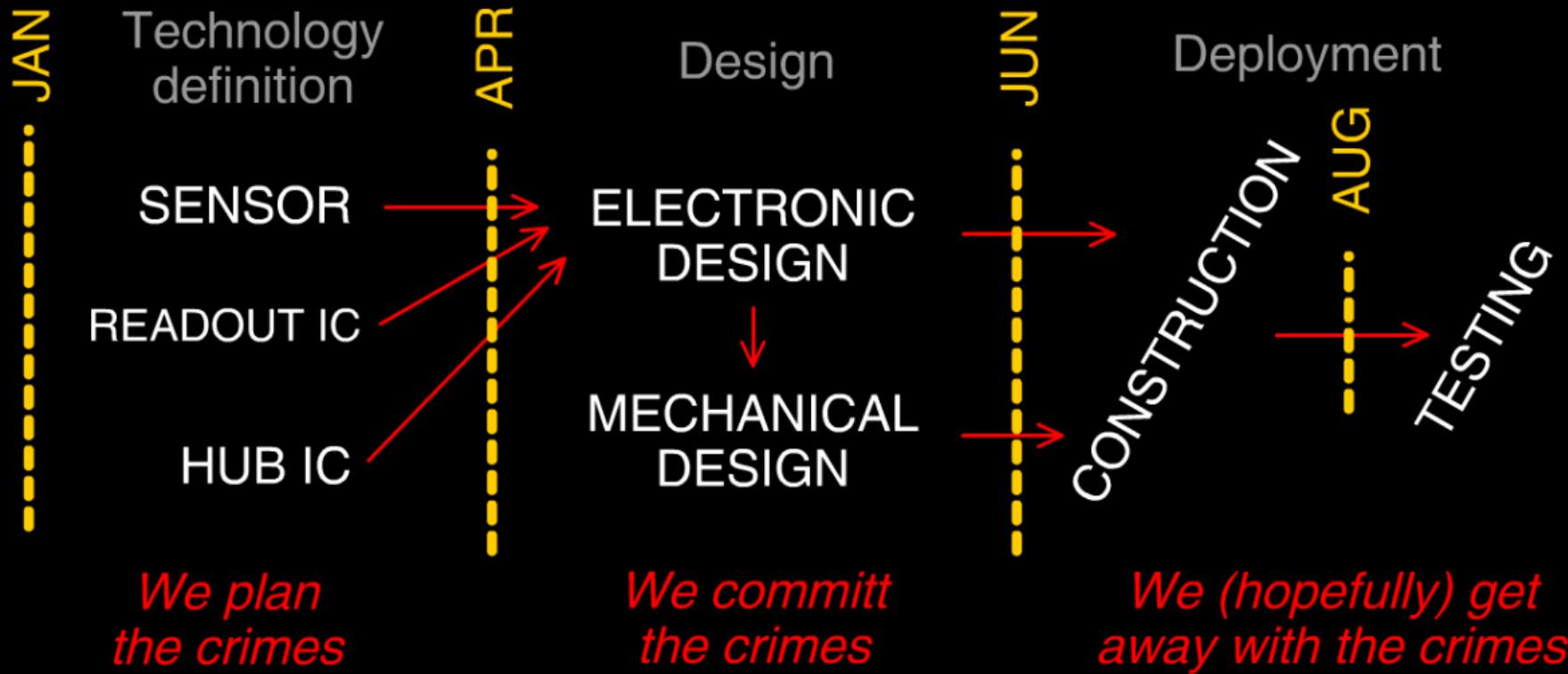


*We plan
the crimes*

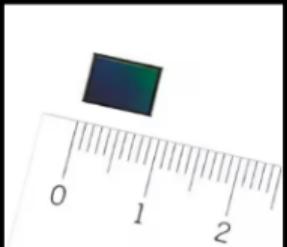
*We committ
the crimes*

*We (hopefully) get
away with the crimes*

The big picture



Which detector to use?



SONY IMX686

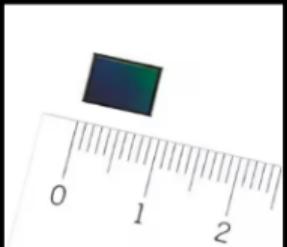
- $7.4 \times 5.5\text{mm}$ area
- $0.8\mu\text{m}$ pixels
- 56% coverage
- 64 Mpixels
- MIPI / CSI2 interface



Omnivision OV64C

- $7.4 \times 5.6\text{ mm}$ area
- $0.8\mu\text{m}$ pixels
- 65% coverage
- 64 Mpixels
- MIPI / CSI2 interface

Which detector to use?



SONY IMX686

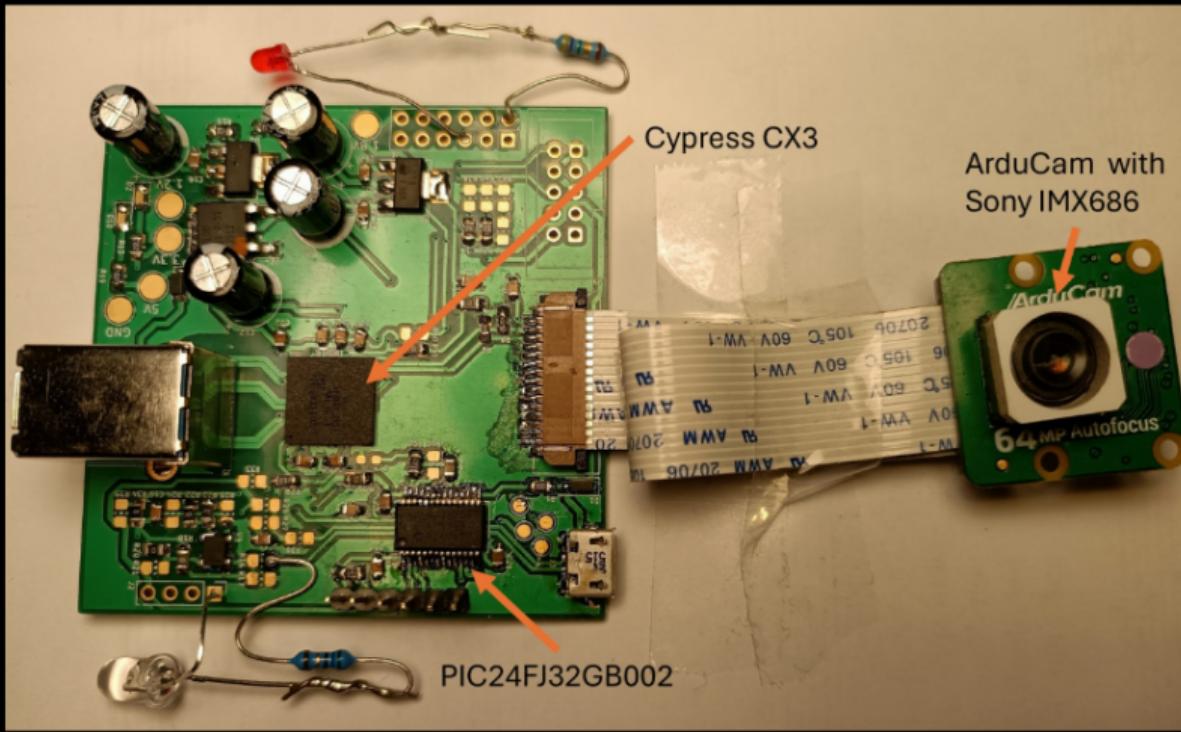
- 7.4 x 5.5mm area
 - 0.8 μ m pixels
 - 56% coverage
 - 64 Mpixels
 - MIPI / CSI2 interface
-
- SONY never answered our e-mails
 - No freely available documentation
 - Die "impossible" to buy
 - In use in consumer products



Omnivision OV64C

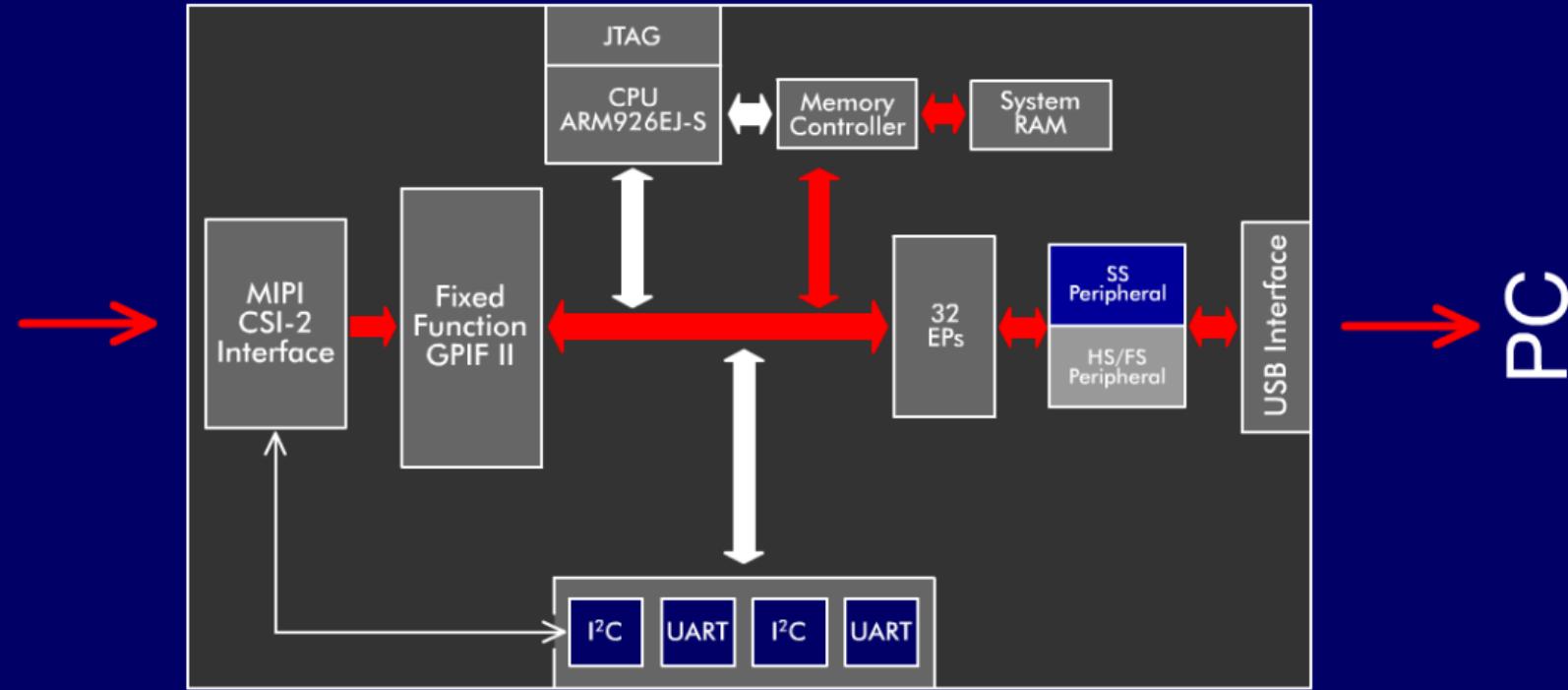
- 7.4 x 5.6 mm area
 - 0.8 μ m pixels
 - 65% coverage
 - 64 Mpixels
 - MIPI / CSI2 interface
-
- Official partnership with OV Dec - Mar
 - They ghosted us for months
 - Documentation available under NDA Apr
 - Unfindable in consumer products

Test board #1



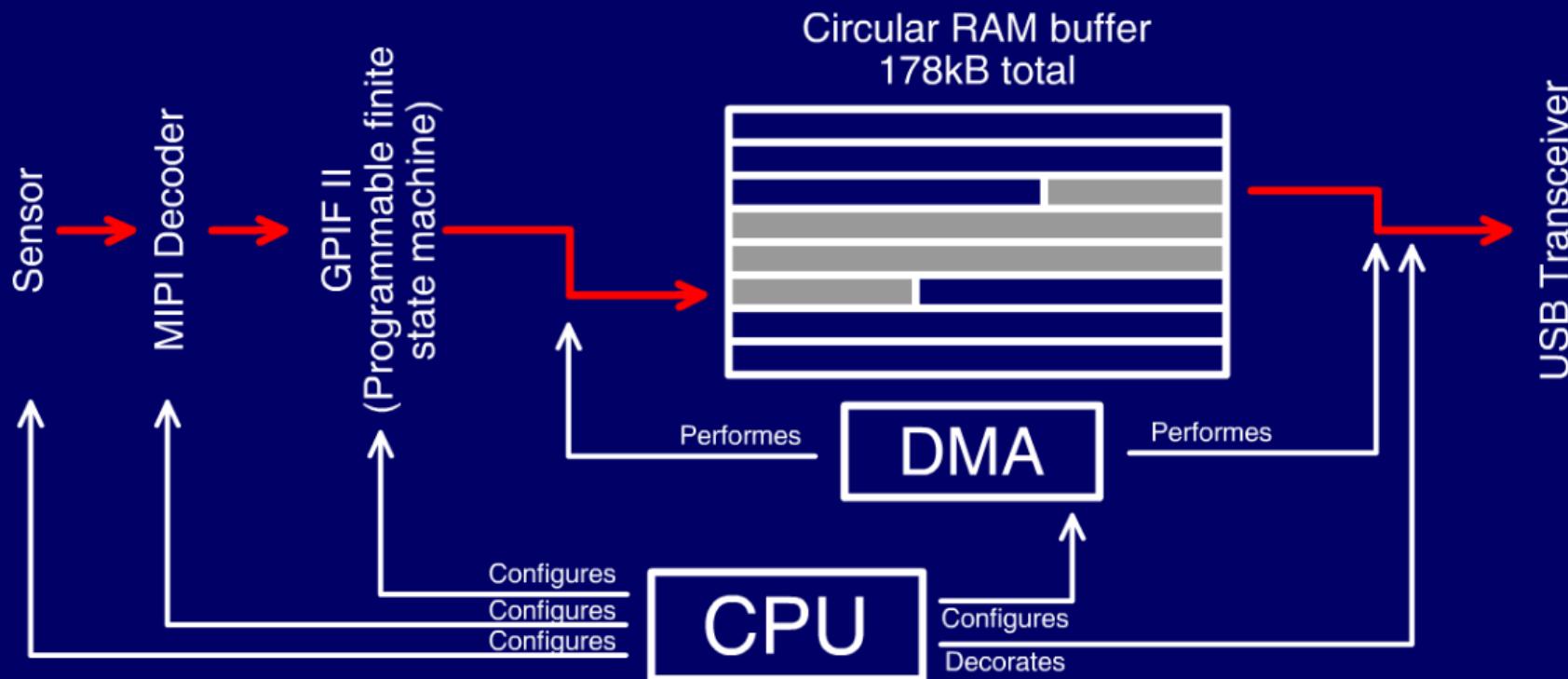
An aside: how does all this work?

SENSOR



CYUSB306X

An aside: how does all this work?



Also, about the USB speed...

USB Version			Bandwidth	DATA Transfer Speed	Logo	Connector	
Official release		Slogan					
USB4	V1.0	USB4 20Gbps USB4 40Gbps	USB4	20 or 40Gbps	2560MB/s 5120 MB/s		
USB 3.2	Gen 2x2	SuperSpeed+	USB 3.2	20Gbps	2560MB/s		
	Gen 2		USB 3.1	10Gbps	1280MB/s		
	Gen 1	SuperSpeed	USB 3.0	5Gbps	640MB/s		
USB	2.0	High-Speed	USB 2.0	480Mbps	60MB/s		
	1.1	Full Speed	USB 1.1	12Mbps	1.5MB/s		
	1.0		USB 1.0	1.5Mbps	0.192MB/s		

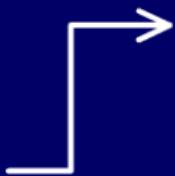


If and only if data transfer
is handled optimally

Also, about the USB speed...

A simpler example

USB Version			Bandwidth	Data Transfer Speed	Bus	Connector
Official release	Stage	Marketing name				
USB 1.0	Y1.0	Universal USB 1.0	12Mbit/s	1.5MB/s	12Mbps	
USB 2.0	Get 2.0	SuperSpeed	480 Mbit/s	480Mbps	480Mbps	
	Get 2.0	SuperSpeed	480 Mbit/s	480Mbps	480Mbps	
	Get 2.0	SuperSpeed	480 Mbit/s	480Mbps	480Mbps	
USB 3.0	Get 3.0	High Speed	4.8Gbit/s	4.8Gbps	4.8Gbps	
	Get 3.0	High Speed	4.8Gbit/s	4.8Gbps	4.8Gbps	
	Get 3.0	High Speed	4.8Gbit/s	4.8Gbps	4.8Gbps	
USB	3.0	High Speed	4.8Gbit/s	4.8Gbps	4.8Gbps	
	3.1	High Speed	10Gbit/s	10Gbps	10Gbps	
	3.2	High Speed	10Gbit/s	10Gbps	10Gbps	



→ USB 1.1 Full Speed

- Up to 1.5 MB/s

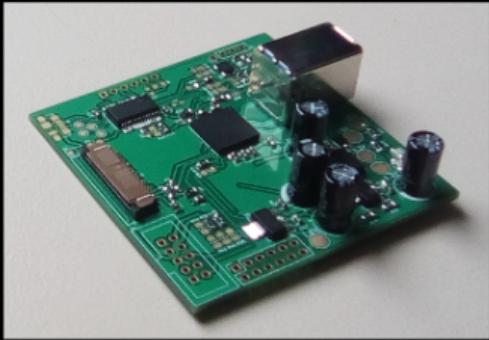
... but ...

- Max packet size: 64 Bytes
- Max 1 transaction every ms



→ Unless protocol uses transactions comprised of a multiple of 24.576 (that's 24 point...) packets, the nominal bandwidth cannot be achieved. And even then...

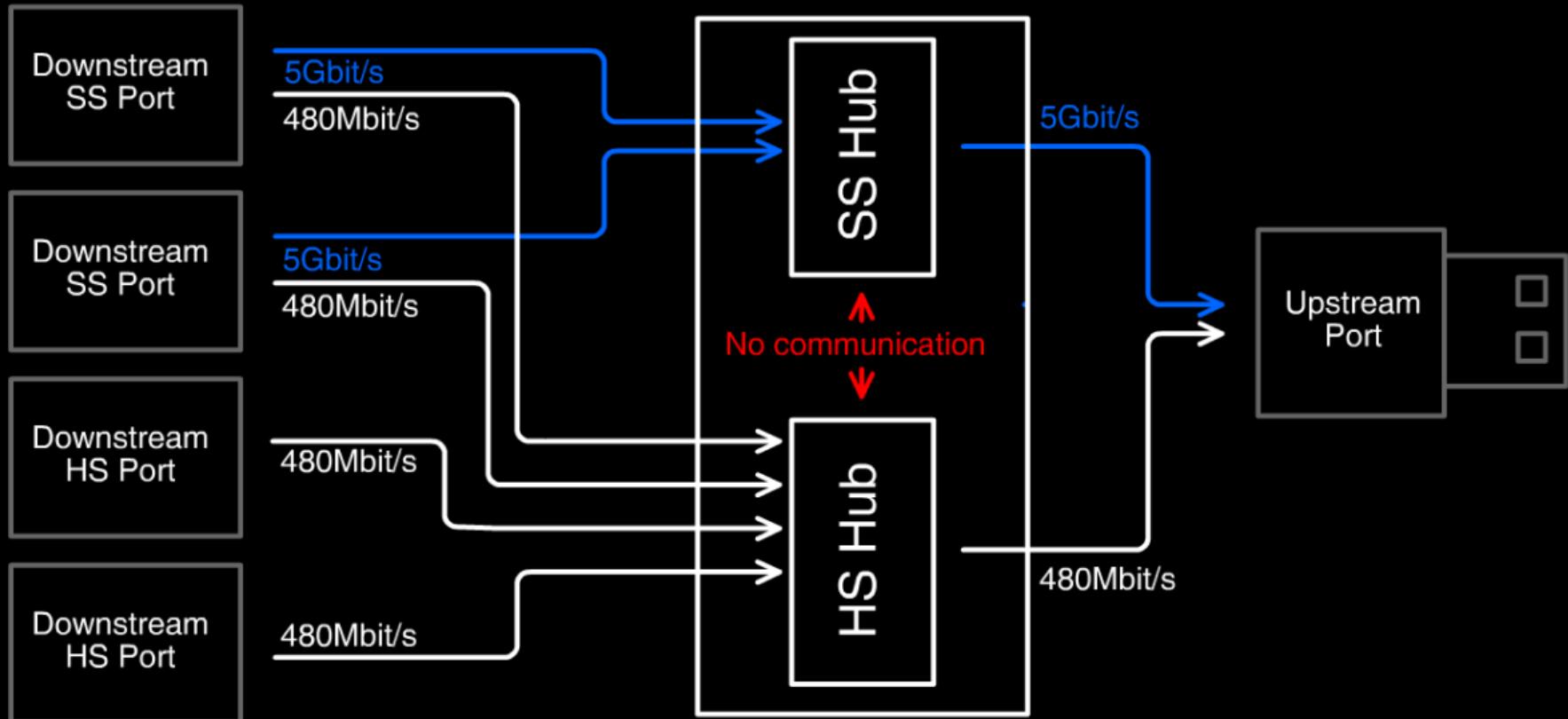
Test board #1



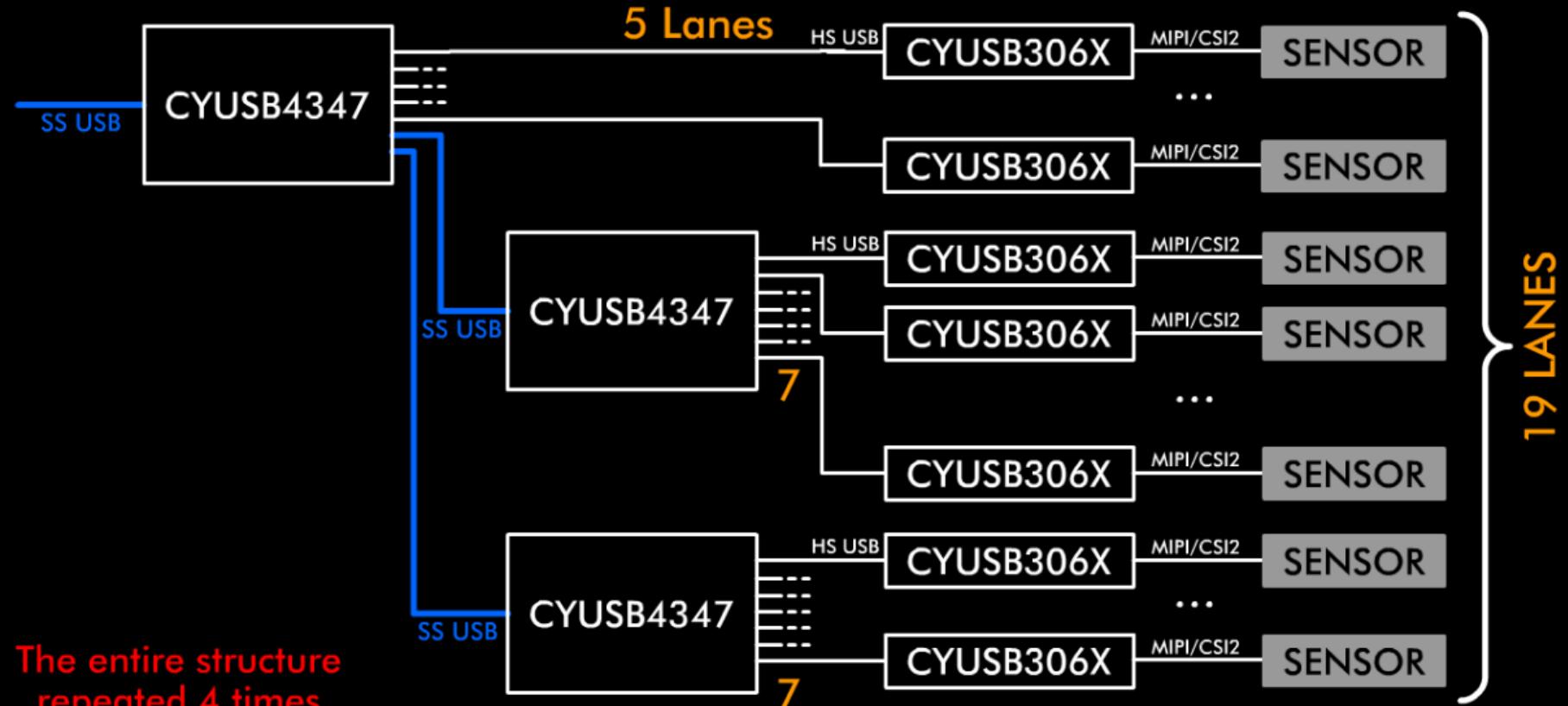
Built	Jan
Successful IMX219 Readout	May
Successful IMX686 Readout	Jun



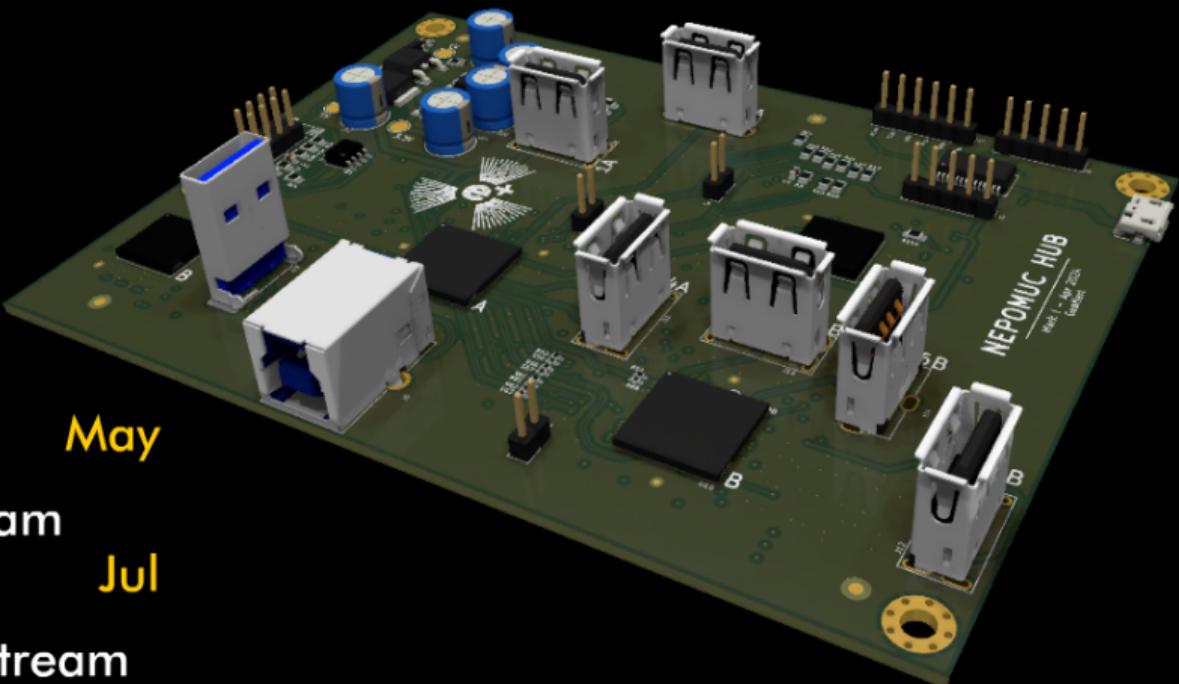
Important discovery



How does *this* look now?



Test board #2



Built

May

Successful upstream

SuperSpeed

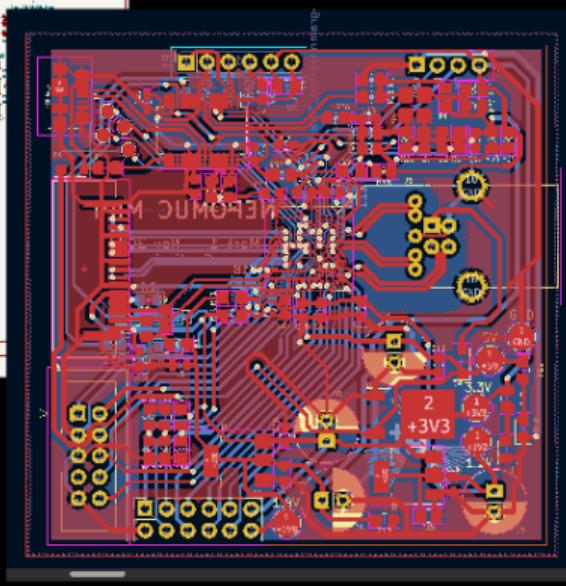
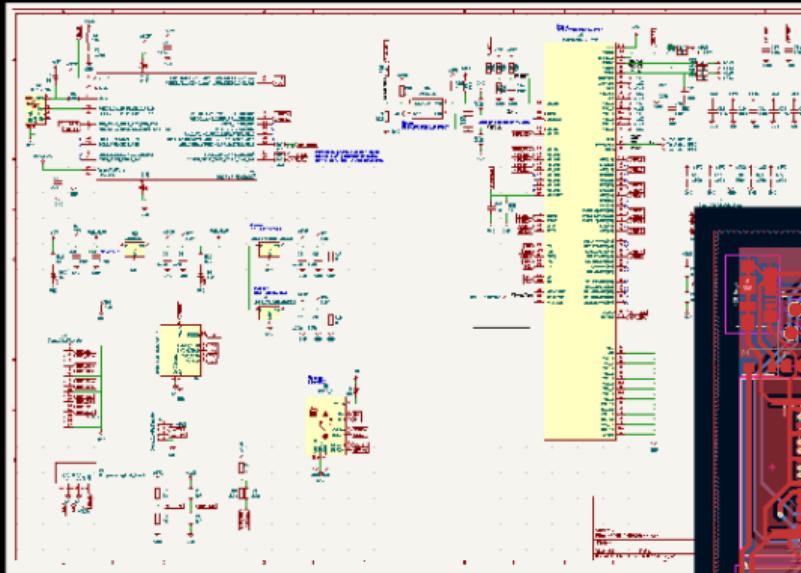
Jul

Successful downstream

SuperSpeed

Fail

Electronic design



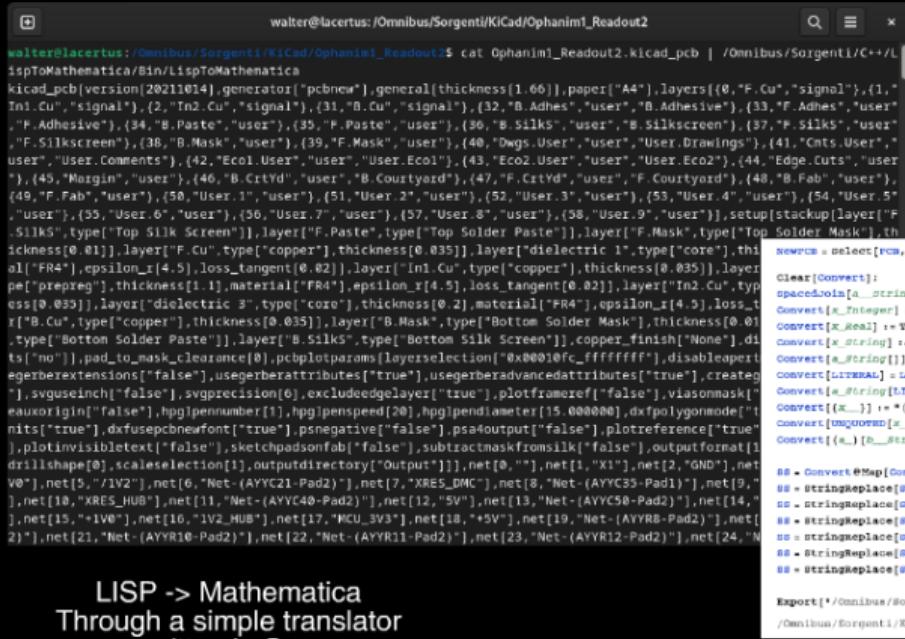
Electronic design

KiCad's native design file format: LISP

```
001 (pwr 4 0.0015 0.0015 0.0015 0.0015 0.0015 0.0015 0.0015 0.0015 0.0015 0.0015 0.0015 0.0015 0.0015 0.0015 0.0015)
002 (net 0 "GND") (pin-type "passive") (tstamp 00000000 0000 4ecf 0000 000000000000)
003 (model "%KICAD08_JDWELL_01R/Capacitor_0M.Ddshape/c_8422_1005Metall.wrl")
004 (affine (xyz 0 0 0))
005 (scale (xyz 1 1 1))
006 (rotate (xyz 0 0 0))
007 )
008 )
009 )
010 )
011 )
012 )
013 (footprint "Gummifert_C_3063_100st" (layer "F.Cu")
014 (idRef 0 0 0 0) [(tstamp 92b2c2b4-0012-0031-beb8-56fb06513b23]
015 (at 30 712581 25 0.000999)
016 (desc "Capacitor C_3063 100st (layer Metall), square (rectangular) end terminal, APC_3531 nominal with elongated pad for hand soldering. (Body size source: IPC-SM-002 page 10, component reference table, note 7.2a, amendment 1 and > pdf), generated with Kicad footprint generator")
017 (legs "Capacitor_handsolder")
018 (property "Diameter1#1" "Opposite_Railout0_Kicad.wrl")
019 (property "Diameter2#1" "")
020 (path "7a0a0331 4286 4544 a32f 8fe773db1075a")
021 (label std)
022 (fp_text reference "C35" (at 8.837495 1.45) (layer "F.Silkscreen"))
023 (effects (font (size 1 1) (thickness 1 1)))
024 (tstamp 327ac4e8 d050 4d73 36cd 6a7821c07bdc)
025 )
026 (fp_text value "100n" (at 0 1.45) (layer "F.Pb"))
027 (effects (font (size 1 1) (thickness 1 1)))
028 (tstamp 65d5d1849 ed77 4e62 9048 ab576871a0a0)
029 )
030 (fp_text user "$!$!$!$!$!$!" (at 0 0) (layer "F.Pb")
031 (effects (font (size 8 4 8 4) (thickness 8 8 8)))
032 (tstamp 61784855 8fdc 4e04 a144 1f78rrr0000)
033 )
034 (fp_line (start -0.15 0.125) (end 0 0.175) (layer "F.Silkscreen") (width 0.12) (tstamp 11c94318 a538 4542 8790 f5258aef77f25)
035 (fp_line (start 0 -0.125) (end 0 0.125) (layer "F.Silkscreen") (width 0.12) (tstamp 2ae0db2e-127e-4f97-b013-42e7d2d29e0))
036 (fp_line (start 0 0.2) (end 0.15 0.35) (layer "F.Silkscreen") (width 0.12) (tstamp 454b7e1a a9d0 4fc0 0b10 75779444936d))
037 (fp_line (start 0 +0.2) (end 0.15 -0.35) (layer "F.Silkscreen") (width 0.12) (tstamp 72f7be5a-bc63-1177-e718-8449ed436871))
038 (fp_line (start 0.15 0.125) (end 0.15 0.425) (layer "F.Silkscreen") (width 0.12) (tstamp 70b52884 6b01 487c e54c 7070fd438327))
039 (fp_line (start -0.15 0.425) (end 0.15 0.425) (layer "F.Silkscreen") (width 0.12) (tstamp 0b9430b5-577b-1fbc-bb6f-a12e73a72cd))
040 (fp_line (start 0 0.35) (end 0 0.2) (layer "F.Silkscreen") (width 0.12) (tstamp b0152a0f0 1d96 41f5 e5c0 a734a0825a27))
041 (fp_line (start 0.15 0.225) (end 0.15 0.125) (layer "F.Silkscreen") (width 0.12) (tstamp 077a4299-0f1e-429e-8119-cc9e880d79e27))
042 (fp_line (start 0 0.875) (end 0.15 0.125) (layer "F.Silkscreen") (width 0.12) (tstamp hd500d41 108f 4ecf 889046d18c9e))
043 (fp_line (start 0.15 0.725) (end 0.15 0.725) (layer "F.Ctrld") (width 0.85) (tstamp 2020e908-c95-16b2-9eb5-13ce9eab6b91)
044 (fp_line (start 1.65 0.75) (end 1.65 0.75) (layer "F.Ctrld") (width 0.85) (tstamp 2080960d 0f93 40f1 0d81 a4e54a671240))
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047 (fp_line (start 0.6 -0.8) (end 0.6 0.8) (layer "F.Pb") (width 0.1) (tstamp eb5120e0-9559-4dd3-923c-a5ea982330c651))
048 (fp_line (start 0.6 0.4) (end 0.6 0.4) (layer "F.Pb") (width 0.1) (tstamp 4bd774nn 4fn5 4232 9457 d702dcbab7d))
049 (fp_line (start 0.6 -0.9) (end 0.6 0.9) (layer "F.Pb") (width 0.1) (tstamp 89e2e61-e0b5-b4b8-bced-b5c77f9189b))
```

Electronic design

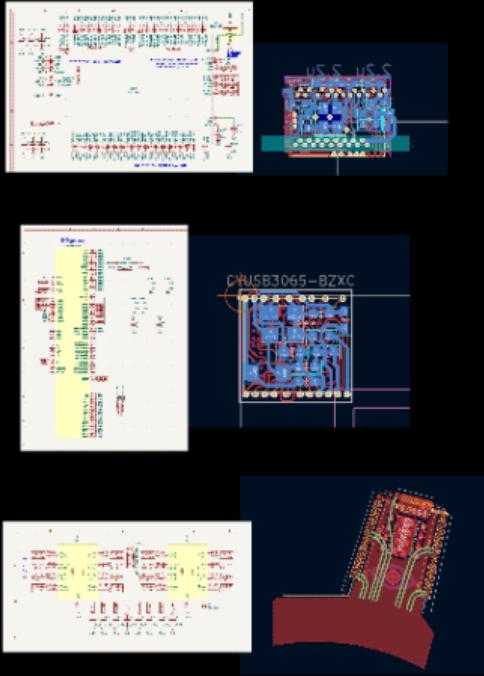
Maps very naturally in Wolfram Mathematica.



```
walter@lacertus:~/Omnibus/Sorgenti/KiCad/Ophanim1_Readout$ cat Ophanim1_Readout2.kicad_pcb | /Omnibus/Sorgenti/C++/LispToMathematica
Mathematica -> LISP
Almost native, this is the entire conversion code
NewPCB = Select[PCB, #[[0]] =!= Segment] & ~Join ~ (KiCadToMathematica@#) ~ Select[cases[PCB, _segment], inverted@#]& ~ Join
Clear[Convert];
spacedJoin[a__String]:=StringJoin@Table[If[i==1, "", " "]\[LessThanEqual]>>{a}[[i]], {i, 1, Length@a}]];
Convert[_Integer]:=ToString[#, CFForm];
Convert[_Real]:=ToString[#, CFForm];
Convert[_String]:=StringReplace[#, {"\r"\[LessThanEqual]>>"\n", "\n"\[LessThanEqual]>>"\r"}]\[LessThanEqual]>>" ";
Convert[_String]:=StringReplace[#, {"\r"\[LessThanEqual]>>"\n", "\n"\[LessThanEqual]>>"\r"}]\[LessThanEqual]>>" ";
Convert[_List]:=LITERAL;
Convert[_String|LITERAL]:=#;
Convert[{x_,y_}]:=>(* <> SpacedJoin[x,y]*);
Convert[imgName@_String]:=StringReplace[#, "\r"\[LessThanEqual]>>"\n"];
Convert[{a_,b_}~_String]:=>(* <> ToString@a <> " " <> SpacedJoin[b]<> " ");
88=Convert@Map[Convert, NewPCB, Infinity];
88=StringReplace[88, {"(segment "~~")\n(segment "~~")"}];
88=StringReplace[88, {"(gruNNErSCoNLINE "~~")\n(gruNNErSCoNLINE "~~")"}];
88=StringReplace[88, {"(footprint "~~")\n(footprint "~~")"}];
88=StringReplace[88, {"via "~~")\n(via "~~")"}];
88=StringReplace[88, {"(net "~~")\n(net "~~")"}];
88=StringReplace[88, {"(UNDERSCORE "~~")"}];

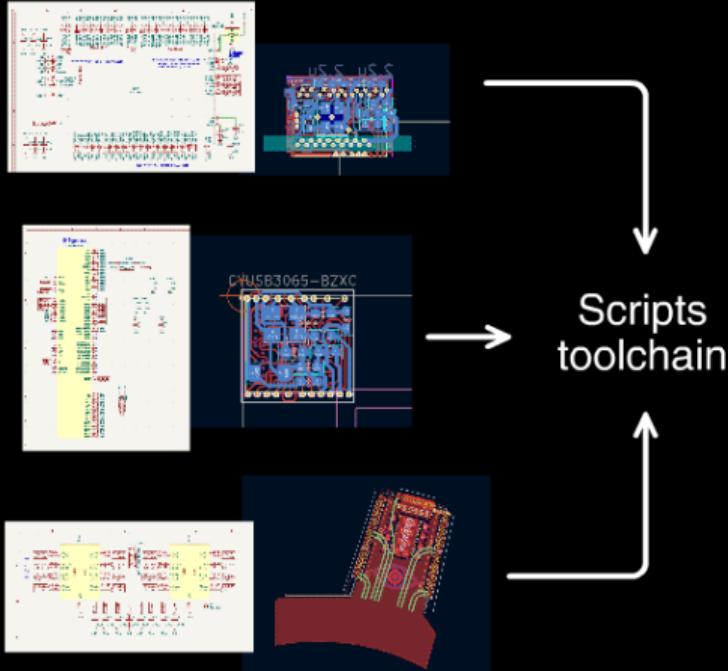
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```

Electronic design



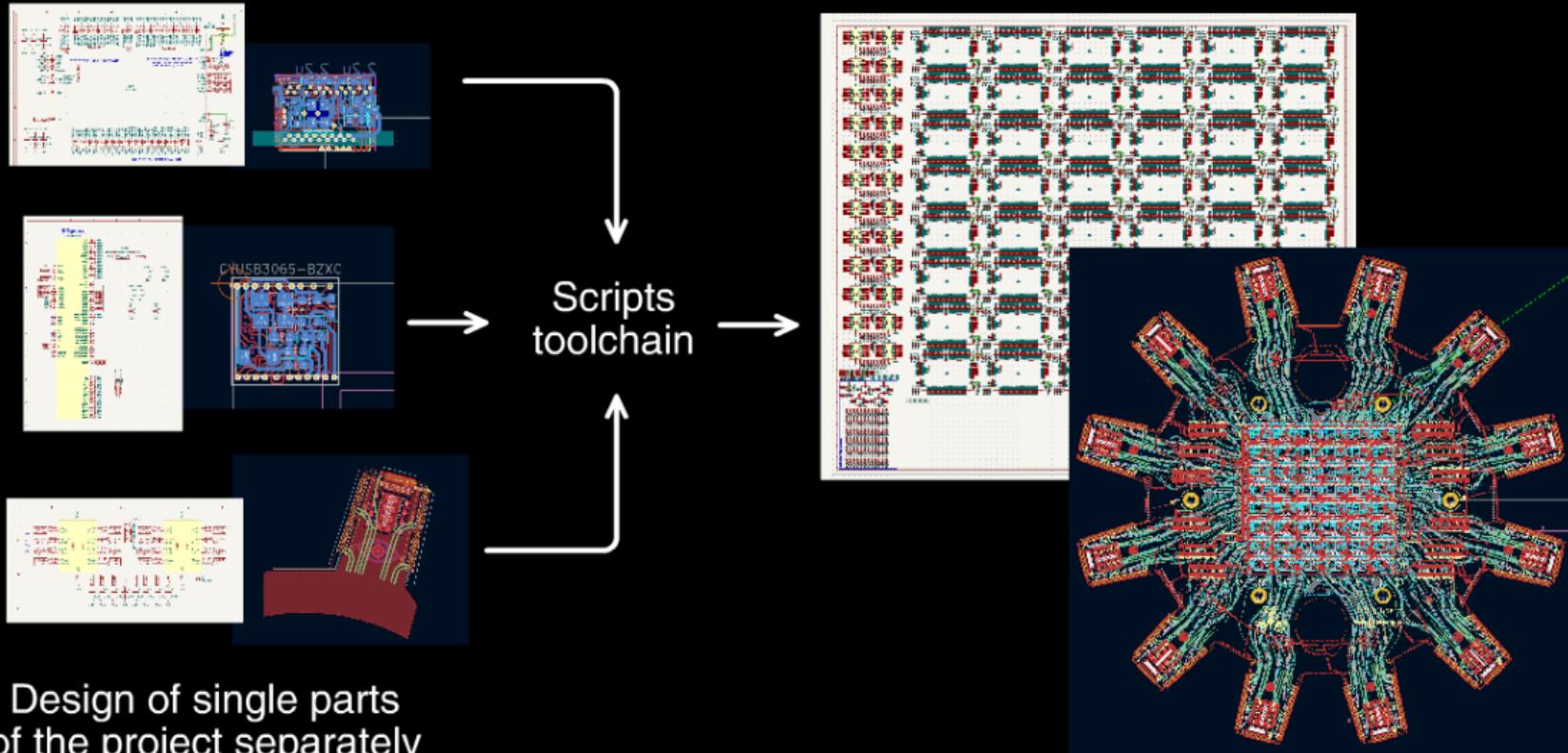
Design of single parts
of the project separately

Electronic design

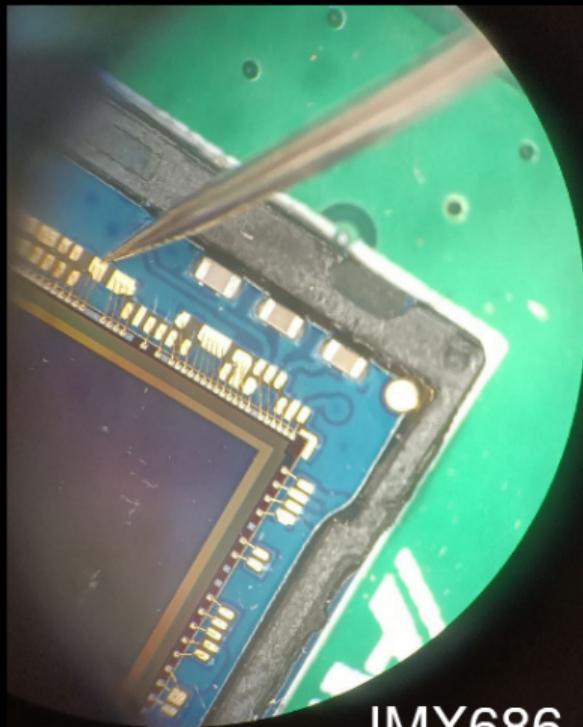
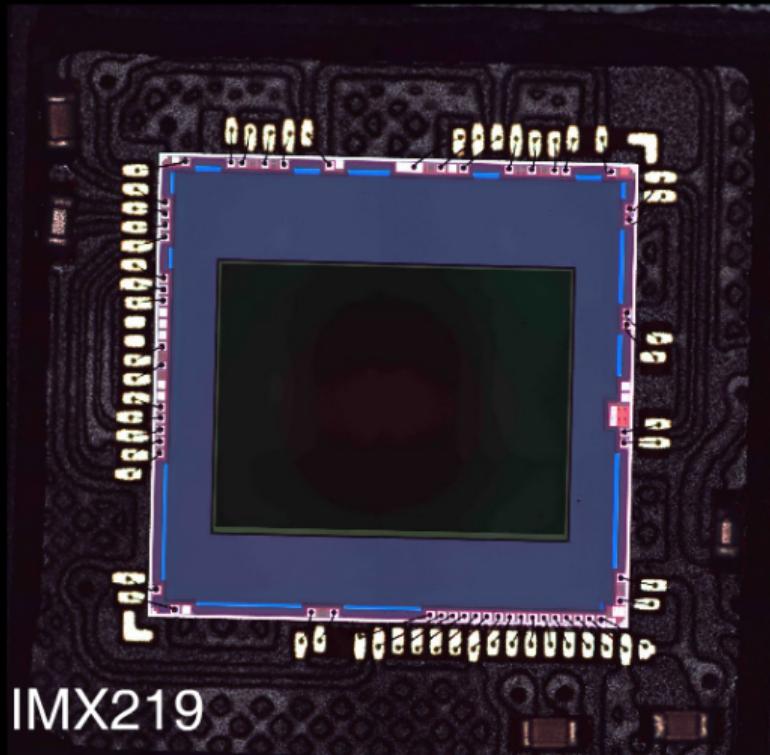


Design of single parts
of the project separately

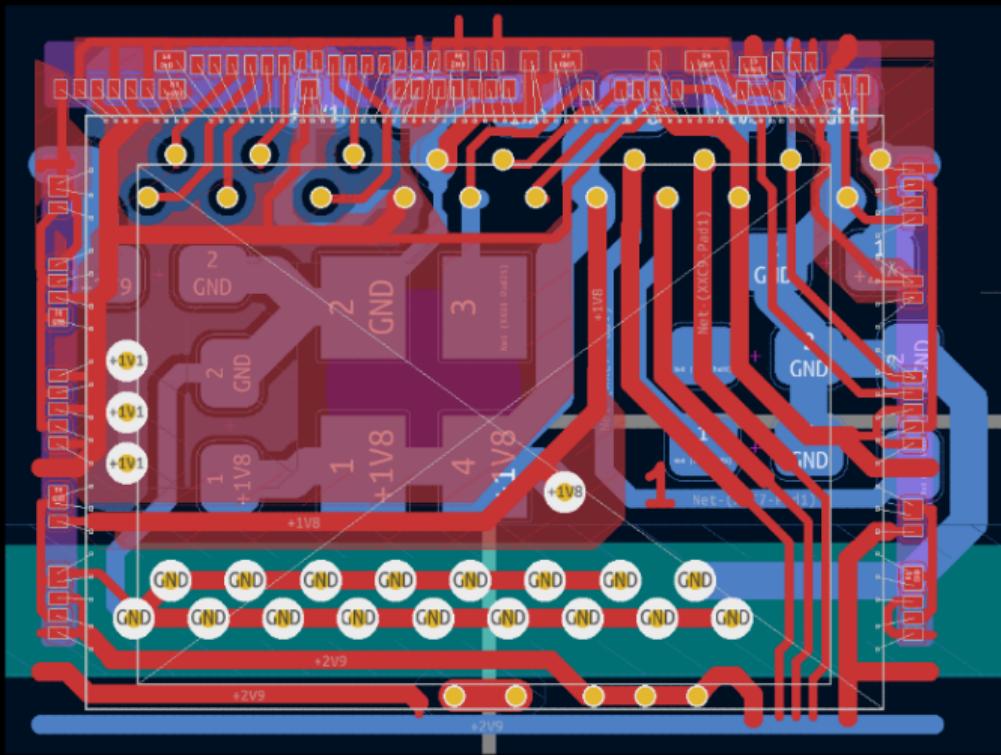
Electronic design



The most delicate part: the sensor

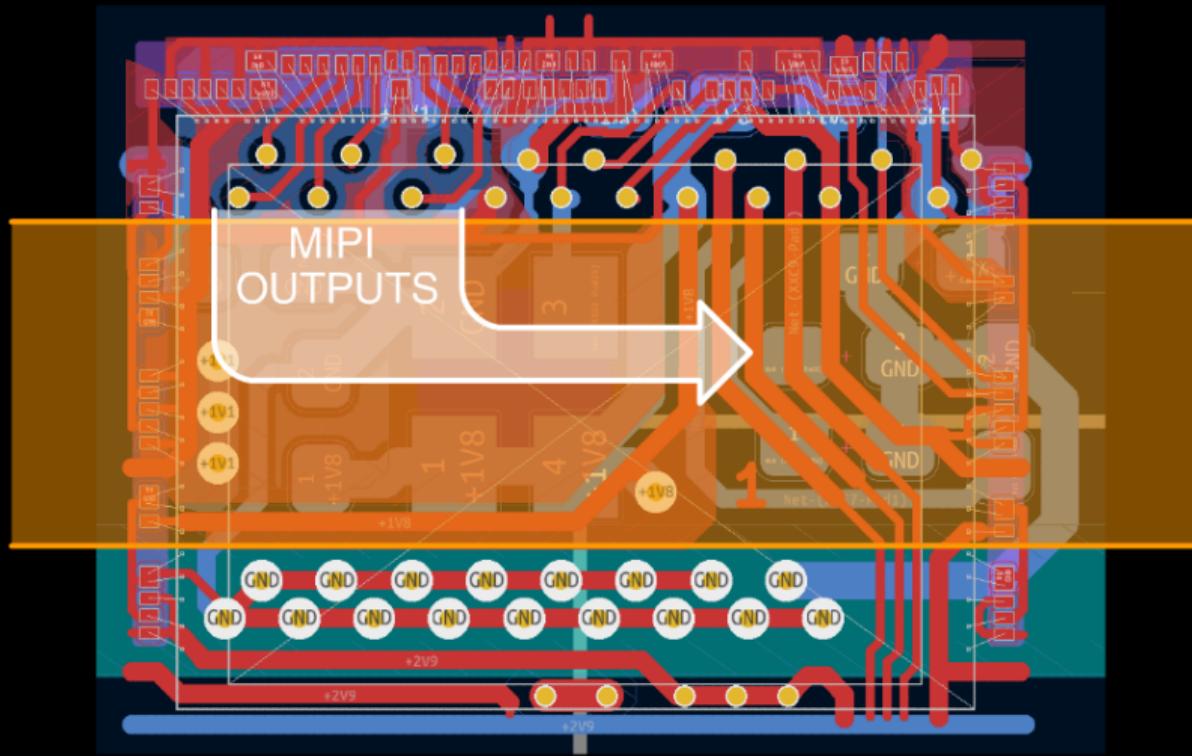


The most delicate part: the sensor

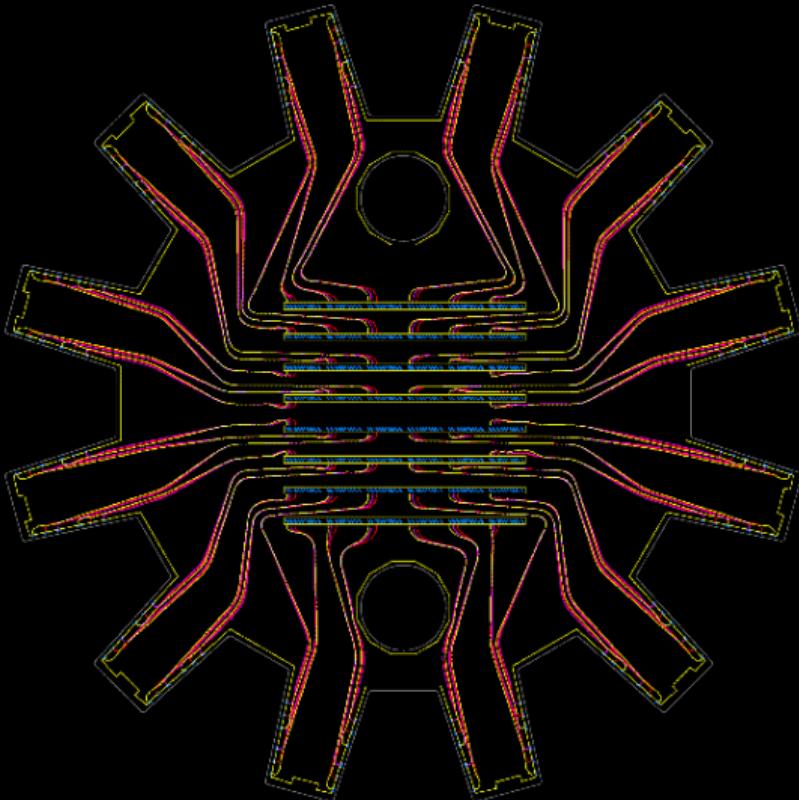


The most delicate part: the sensor

Central
Routing
Channel



Routing MIPI

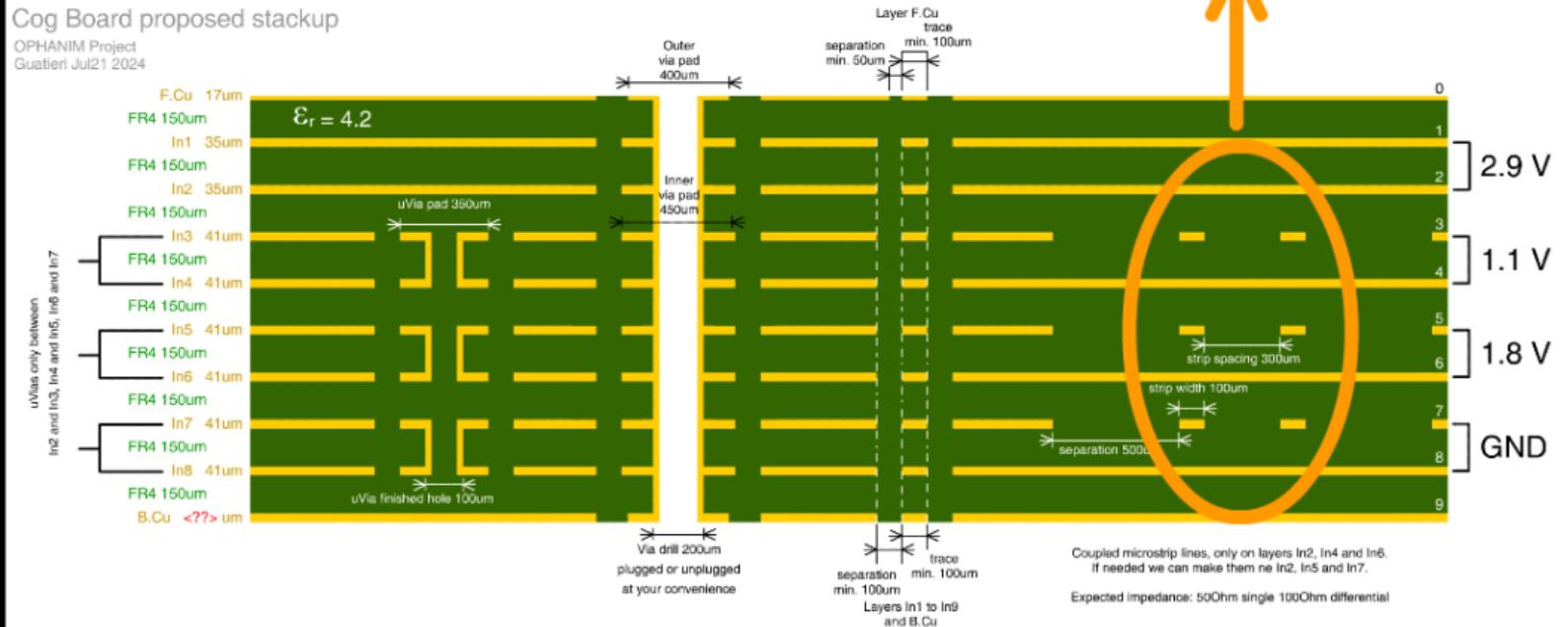


Stackup

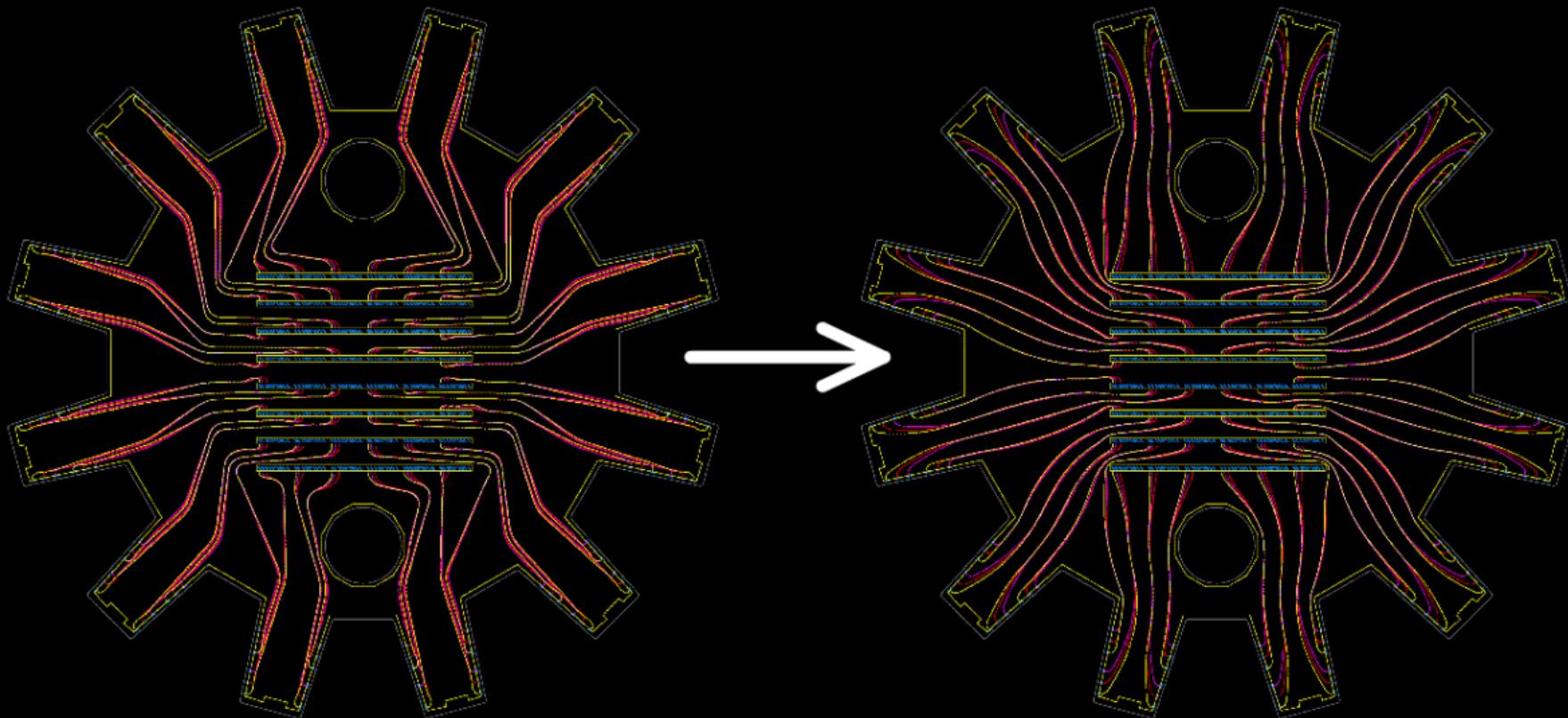
MIPI Lines

Cog Board proposed stackup

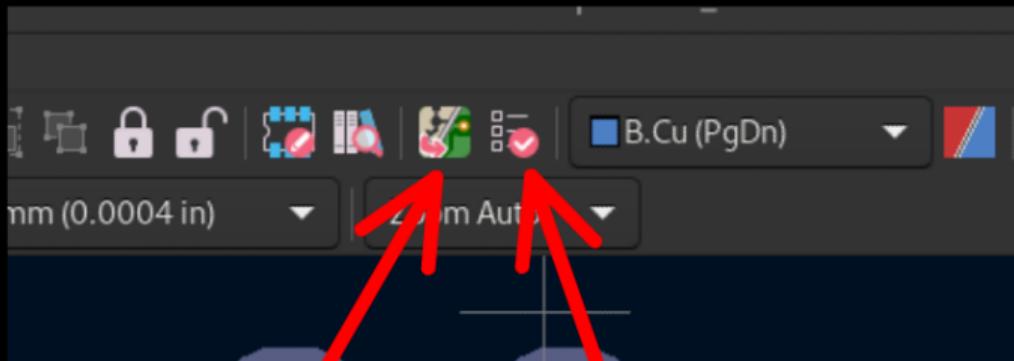
OPHANIM Project
Guatieri Jul21 2024



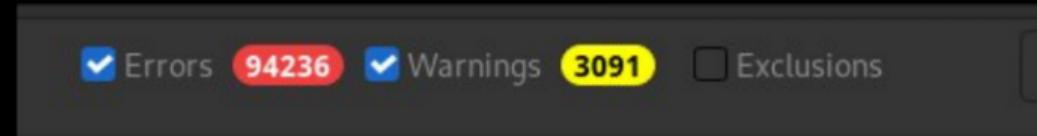
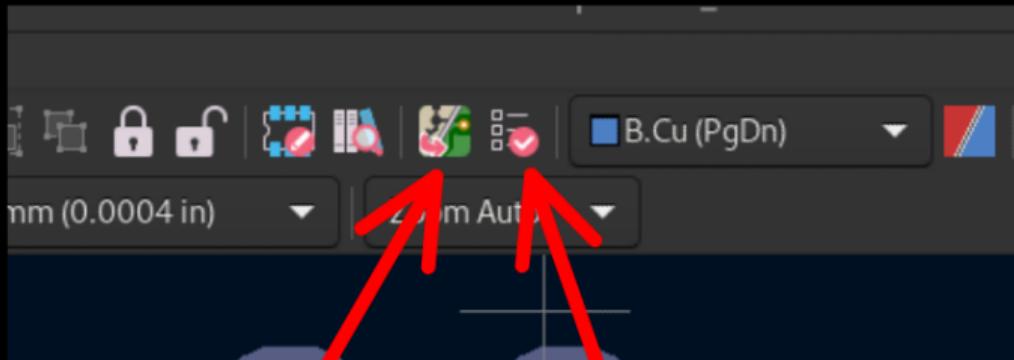
Procedural routing optimization



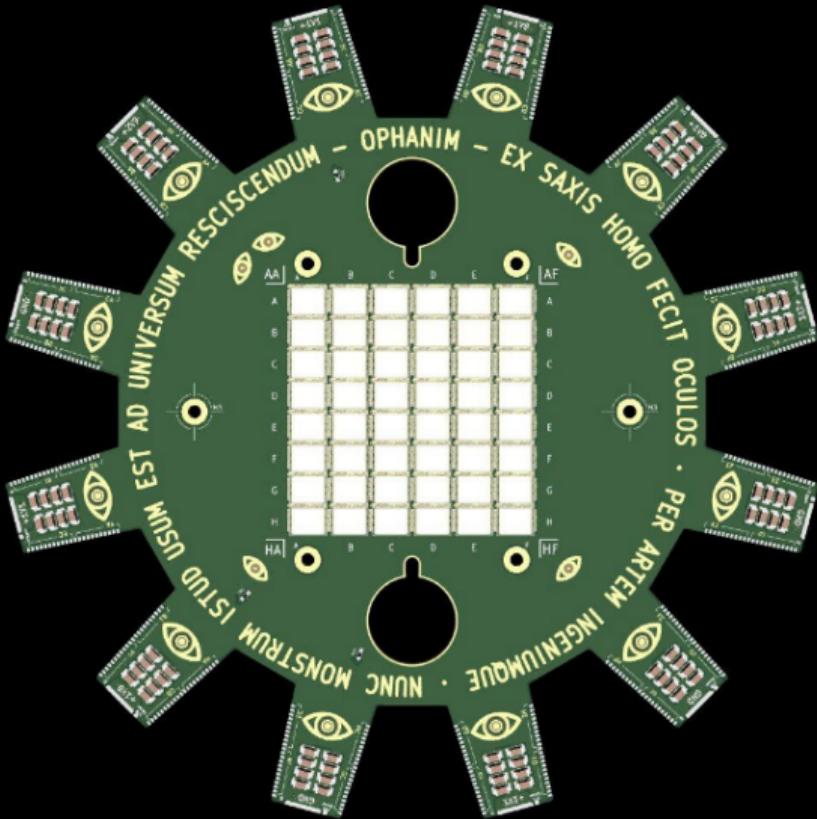
Parity and ERC



Parity and ERC



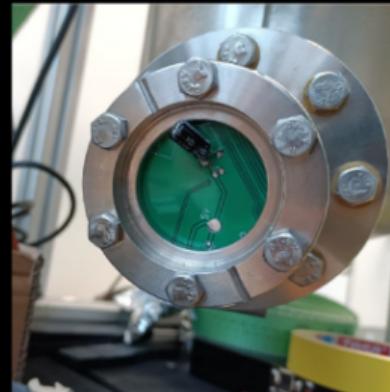
Sensor board design



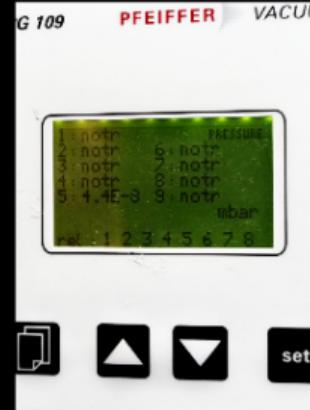
USB-C passthroughs?



Commercial solution
Difficult to order
only in KF flange
5Gb/s (no SS+)



A PCB clamped at 1 Guatieri of torque
Cheap, Flexible
Supports whatever
Single-use. Also, madness

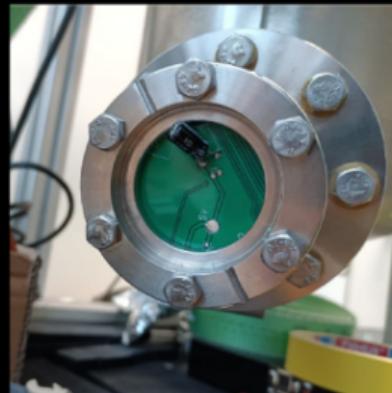


USB-C passthroughs?

End of June



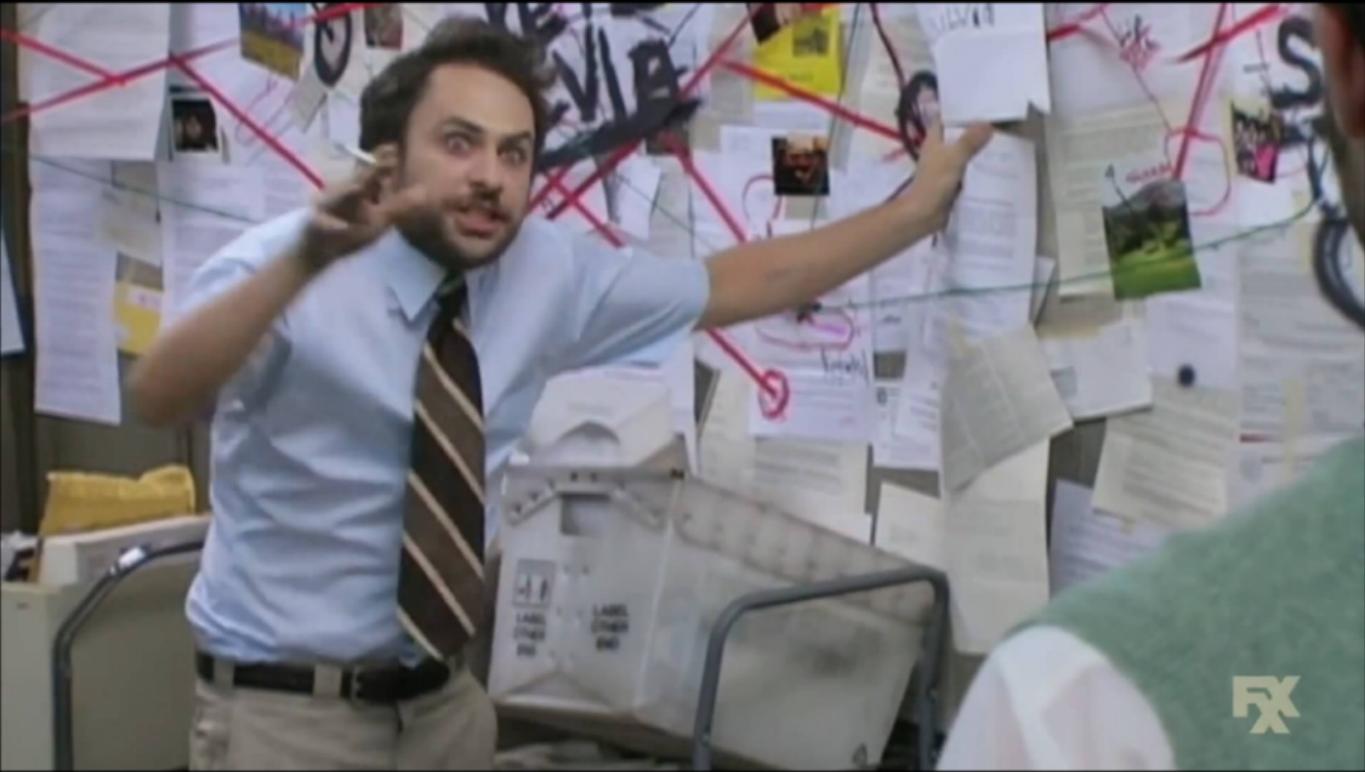
Commercial solution
Difficult to order
only in KF flange
5Gb/s (no SS+)



A PCB clamped at 1 Guatieri of torque
Cheap, Flexible
Supports whatever
Single-use. Also, madness

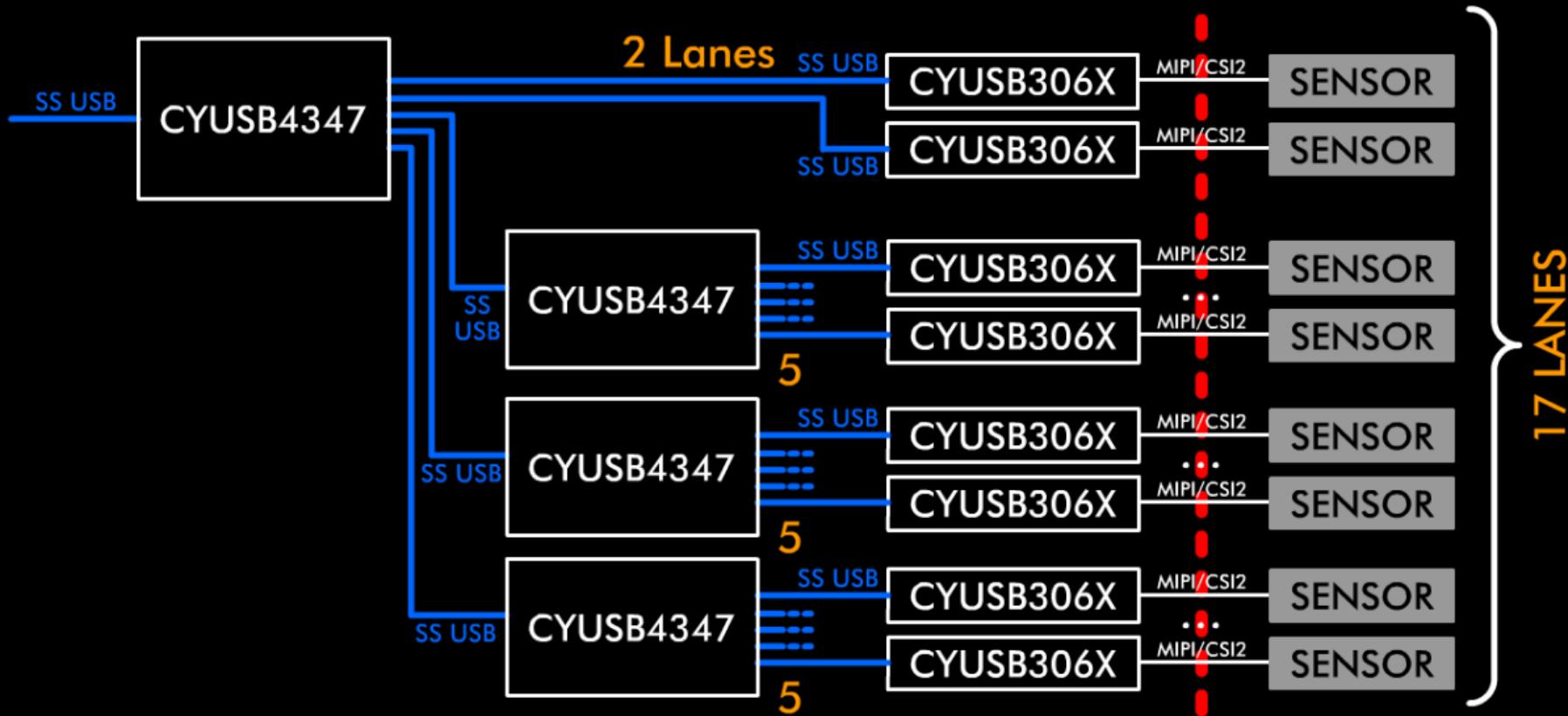


Wait a moment



What if?

VACUUM
FEEDTHROUGH



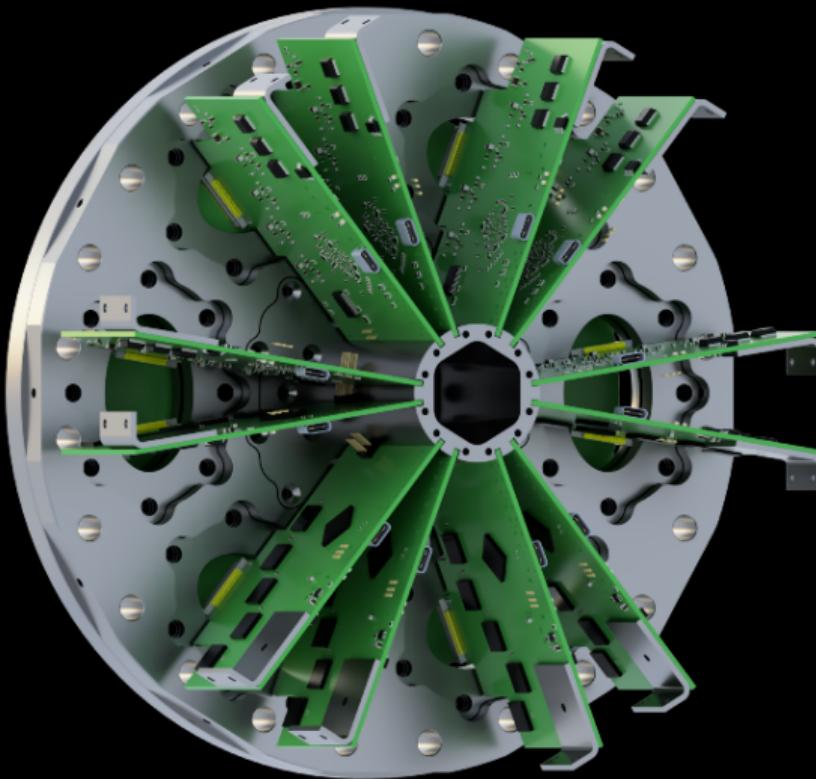
Why?

- No alignment issues
- Combined vacuum-power feedthroughs
- Support for SuperSpeed+ (12 of them, 15GB/s)
- Decouples sensor board from readout cards
- Modular readout cards
- Serviceable readouts
- 2 fewer power rails to vacuum
- Less than half the power in vacuum

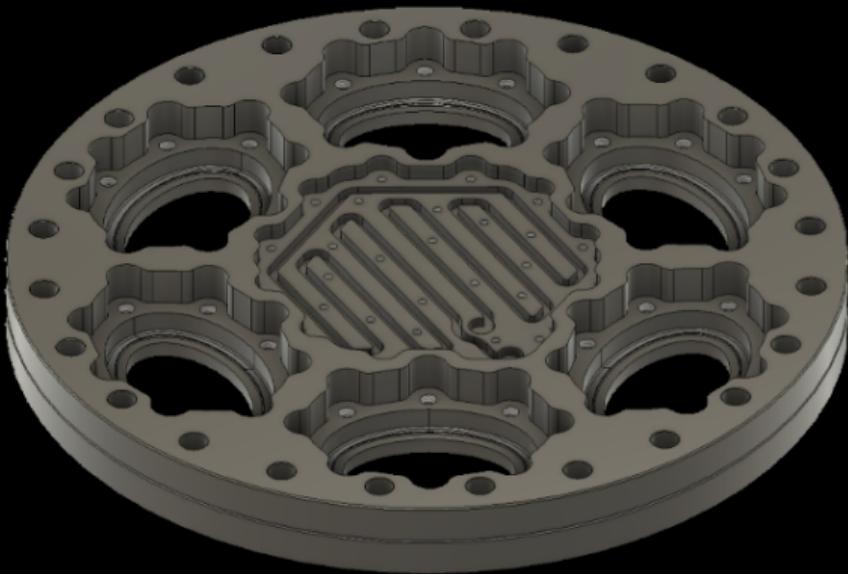
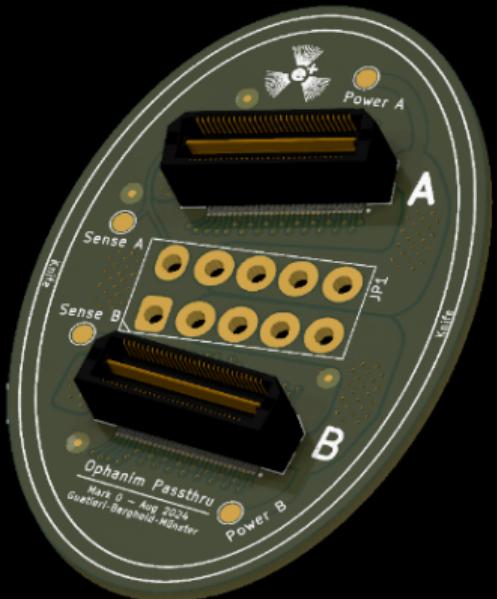
Afuera!



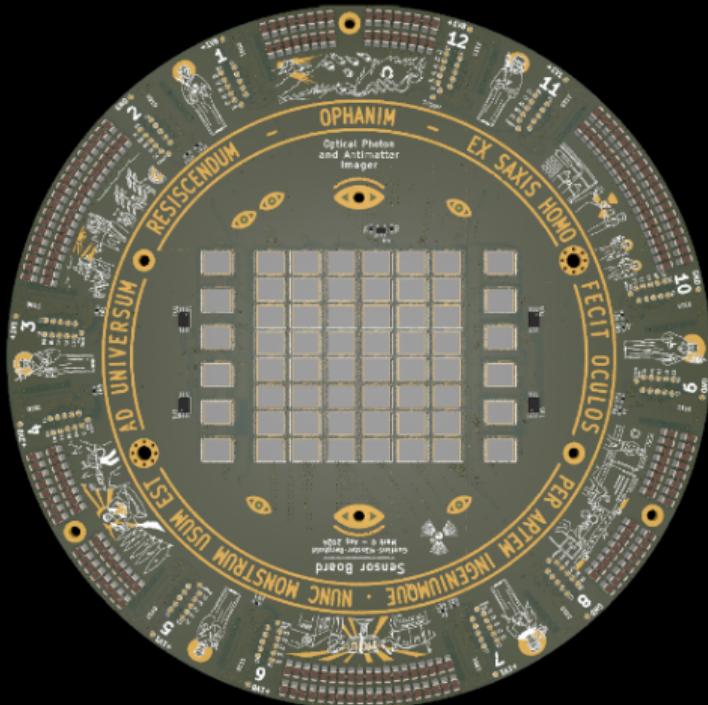
A new design



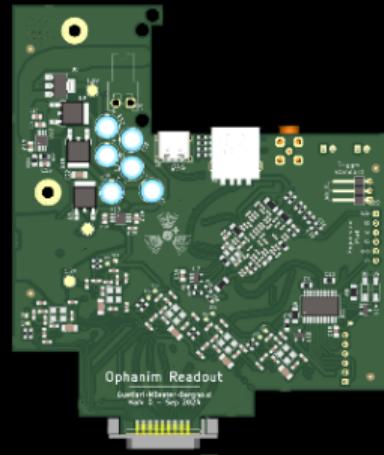
A new design



A new design

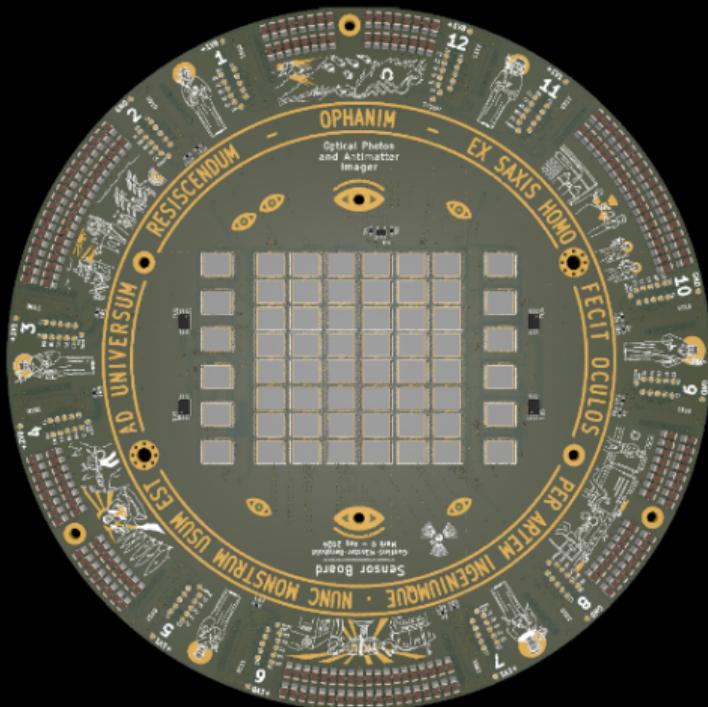


Design time: ~2 months



Design time: 10 days

A new design



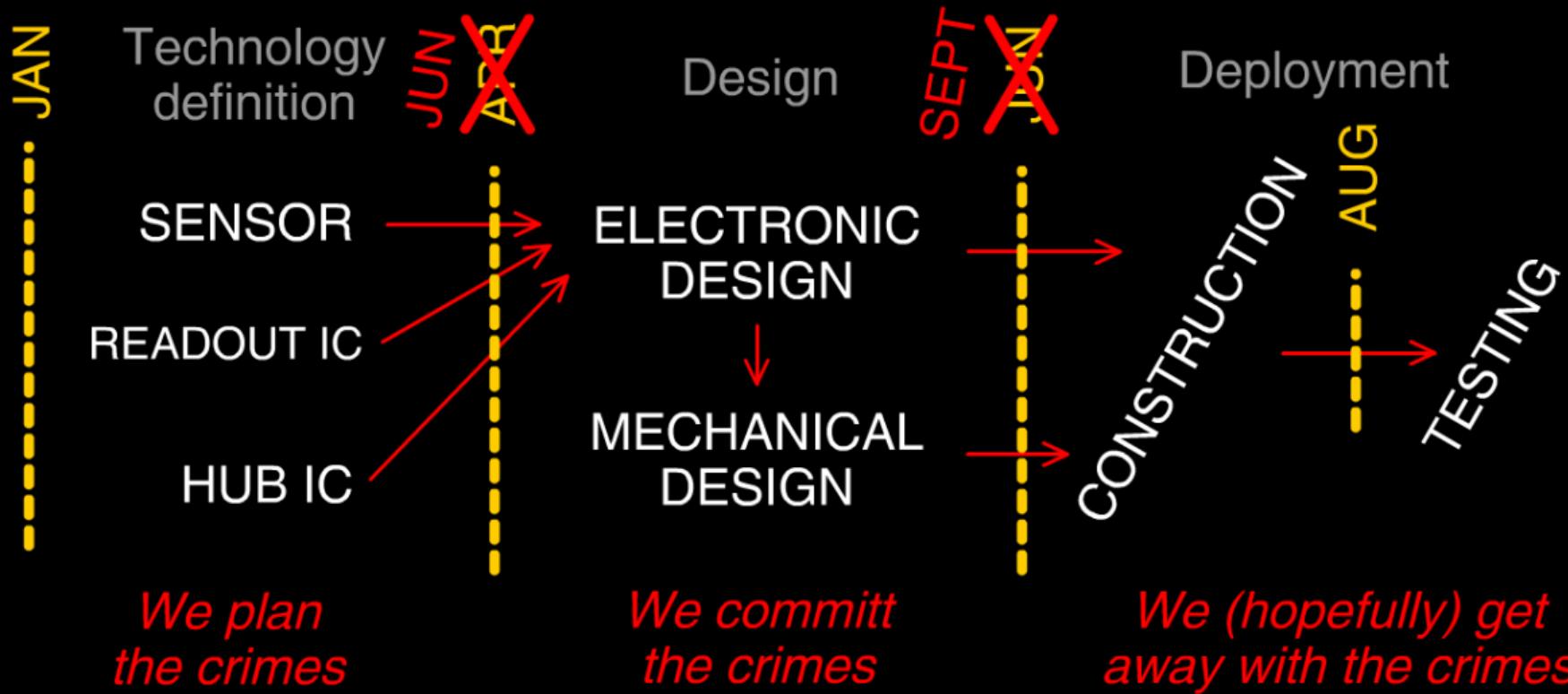
Design time: ~2 months



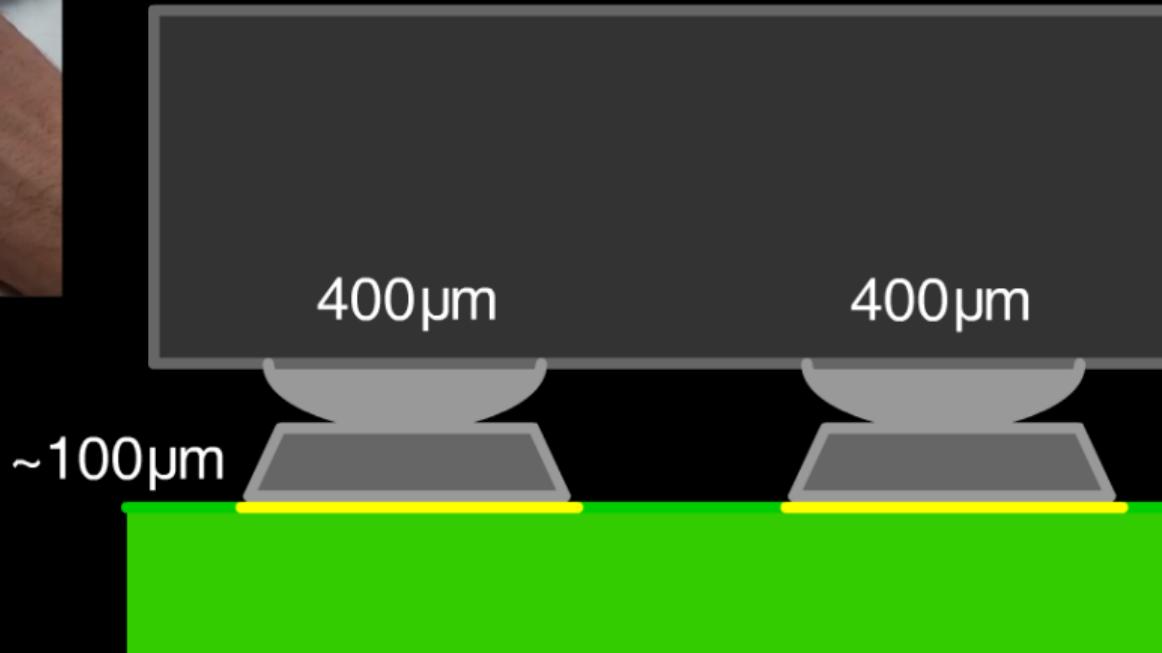
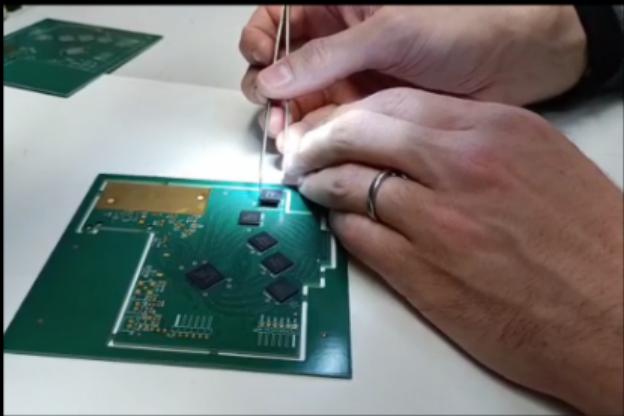
Design time: 10 days

End of September

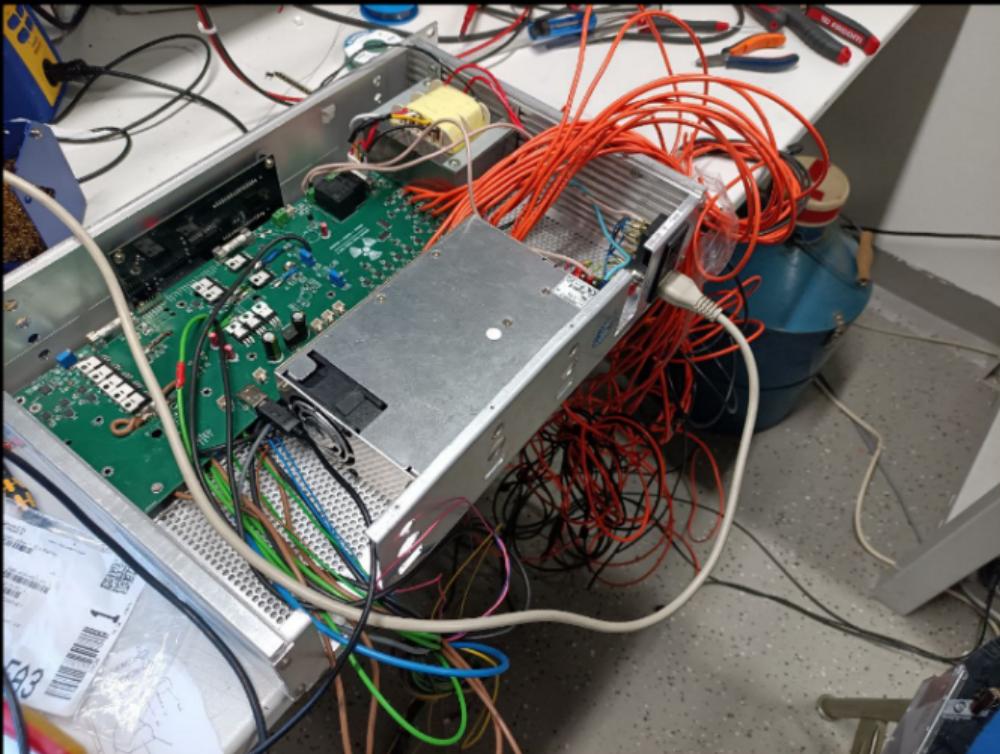
The big picture



New plan: hand assembly



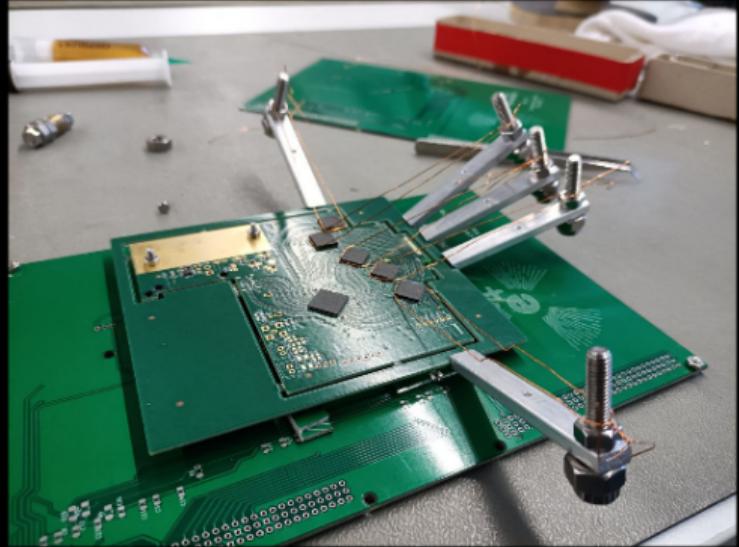
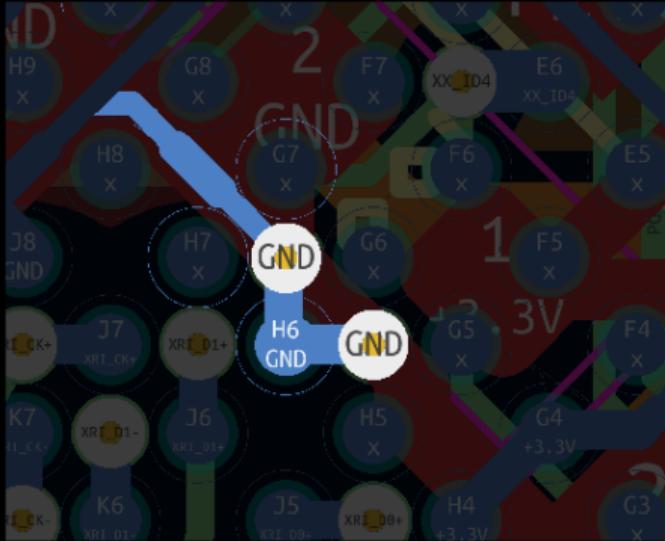
PSU trouble



- Time sink, delays testing the readout cards.
- ILFA fails the first print. Sensor boards delayed to the 8th of November

Readout troubles

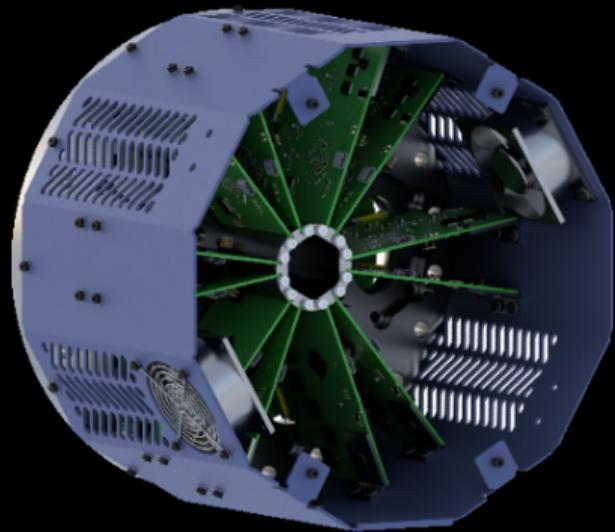
- Some lines require cutting, two below the readout chips
- Wrong chirality in the connector



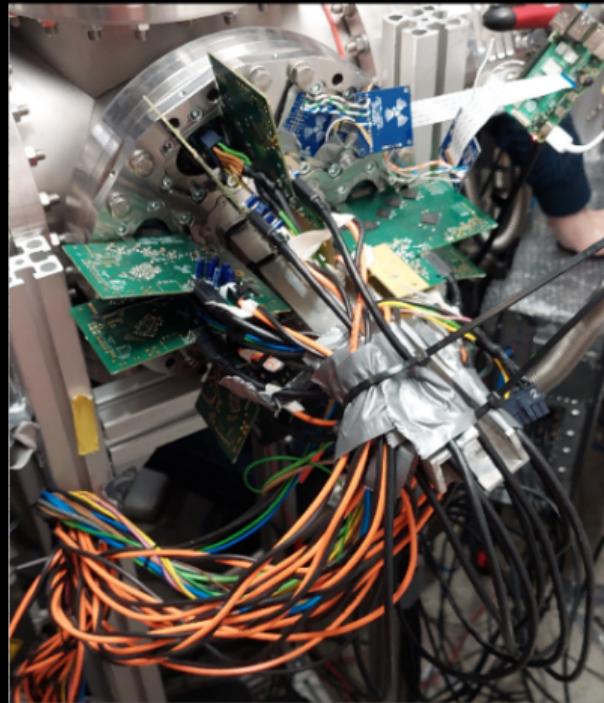
Three days to the CERN mission



Nothing to see here, officer

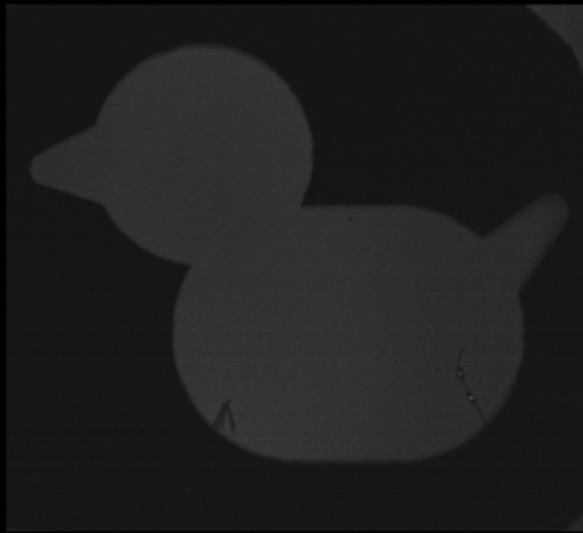


Expectation

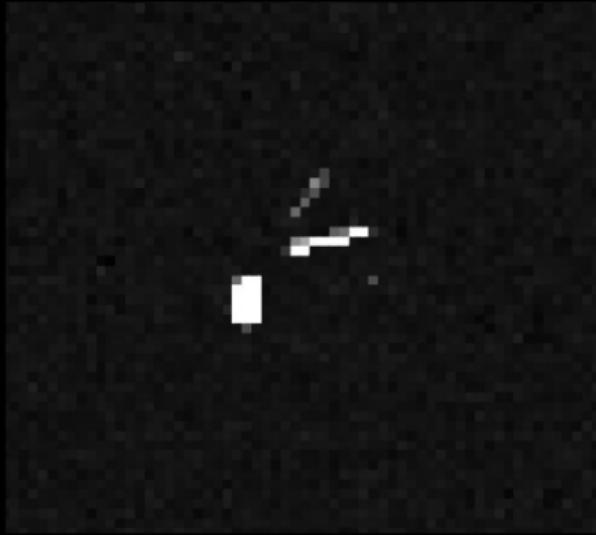


Reality

Also



Expectation



Reality

What next?

- Redesign holders for the passthroughs to address buckling
- Redesign readout cards
 - Correct all issues found during this run
 - Change hub chip (CYUSB4347 -> USB7026C)
- Find proper configuration for chips in sensor board
- Test serialization in PCIe
- Deploy

THANKS FOR YOUR ATTENTION

