AGH UNIVERSITY OF SCIENCE AND TECHNOLOGY

Presentation of Nuclear Electronics and Radiation Detection Group at AGH-UST

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Faculty of Physics and Applied Computer Science
AGH University of Science and Technology

Department of Nuclear Electronics

People:

- 8 scientific staff members (6 ASIC designers)
- Prof. W. Dabrowski (leader), Assoc. prof. M. Idzik, dr...
- 8 PhD students (6 ASIC designers)
- 2 technicians
- Few graduate students every year

Experience - completed projects:

- Multiplicity detector for NA50 at CERN
- Semiconductor Tracker for ATLAS at CERN
- Silicon Drift Detector for ALICE (works for INFN Torino)

Main current projects (collaborations):

- Semiconductor Tracker Readout for ATLAS-Upgrade
- Luminosity Detector (LumiCal) Readout for FCAL at ILC/CLIC
- X-ray silicon strip detector
- Readout of signals from live neuron systems (retina)
- Readout ASICs for gas (GEM, Straw) detectors

Department of Nuclear Electronics...

Technologies:

- AMS 0.35um, IBM 0.25um used in different projects
- IBM 130nm, AMS 180nm – just starting, first submissions in 2011

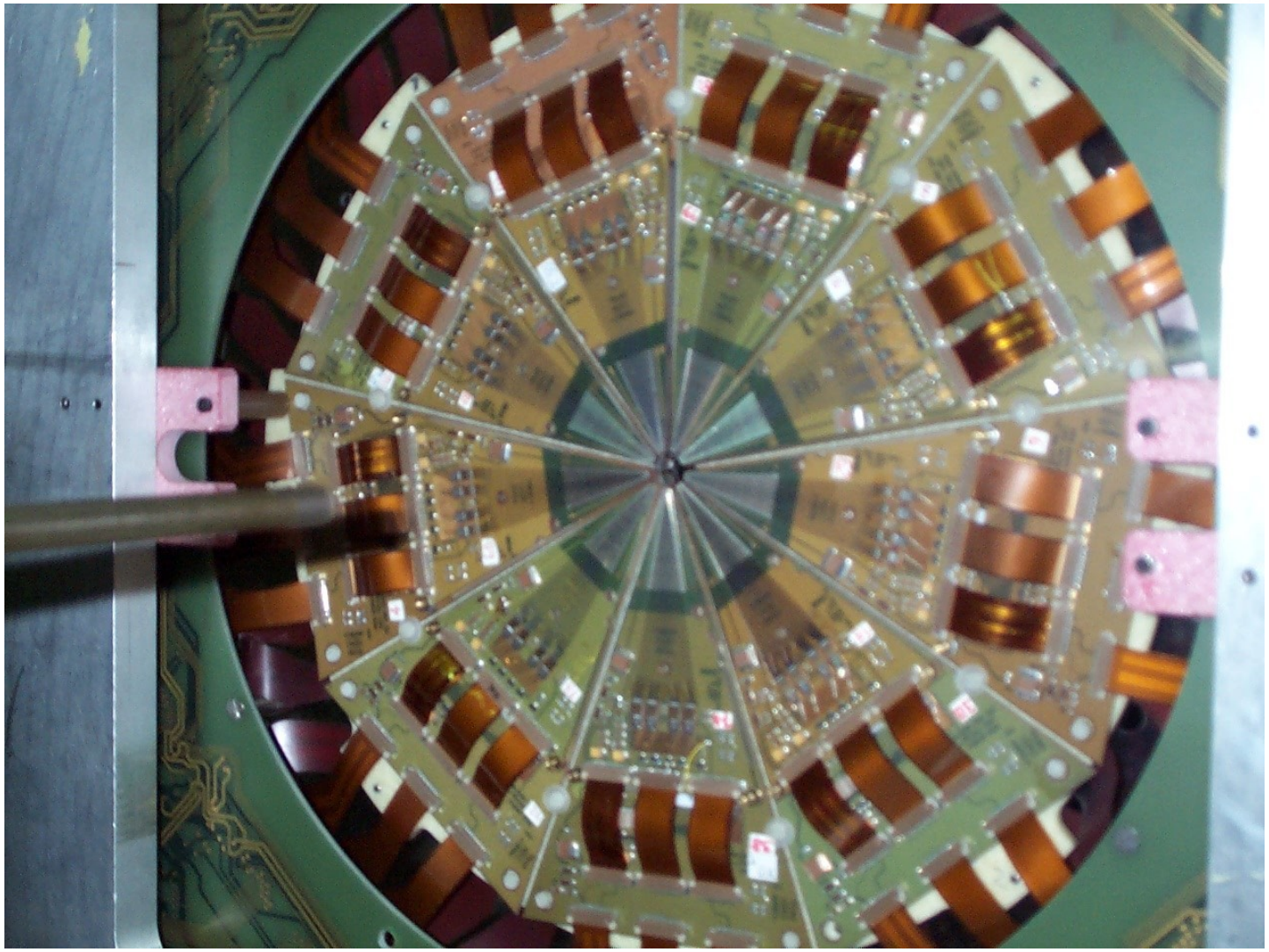
EU projects for HEP and particle detectors:

- FP6: NMI3 (W. Dabrowski), EUDET (M.Idzik)
- FP7: SLHC-PP (W. Dabrowski), MC-PAD (M. Idzik), AIDA (M. Idzik)

Lab/equipment:

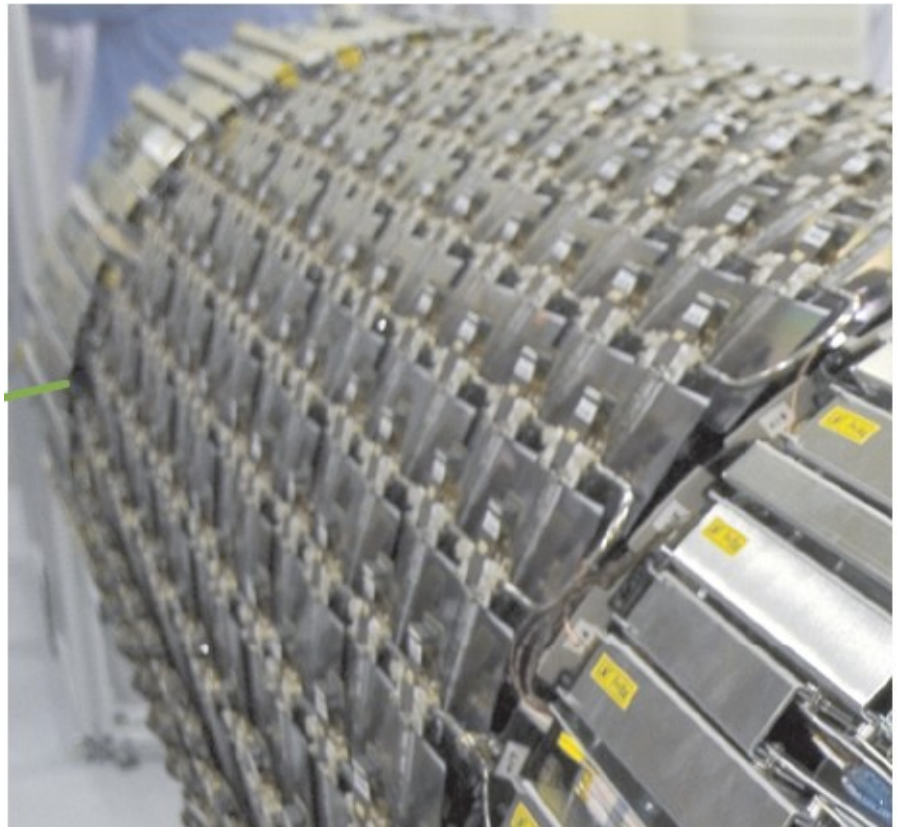
- Microelectronics and semiconductor detector labs
- Cadence software (>20 licenses), FPGA software (25 xilinx lic.), PCB tools,
- Cleanroom, probstation, bonder (F&K Delvotec 5330), Semic. Par. Analyzer (B1500A), Network/Spectrum anal. (Agilent 4395A), Scopes (<=40GHz), Picosecond laser system (PicoQuant PDL 800D), Generators, etc...
- In 2011 received ~600 000 Euro for further lab development

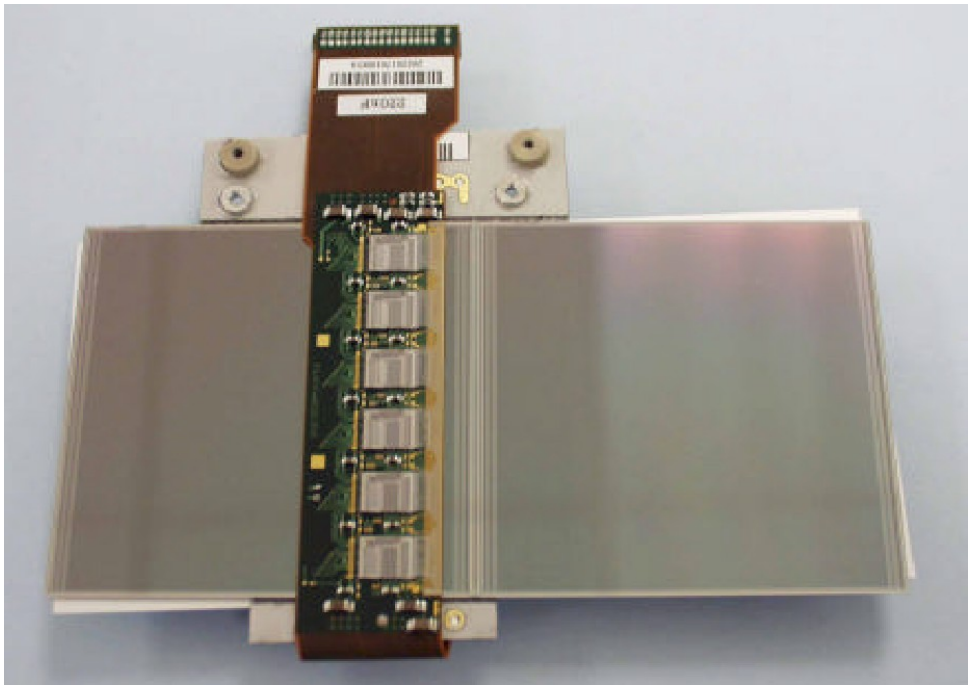
NA50 Multiplicity Detector



- ~15000 channels
- Silicon strips
- Binary front-end, 64 channels ASICs

ATLAS SCT

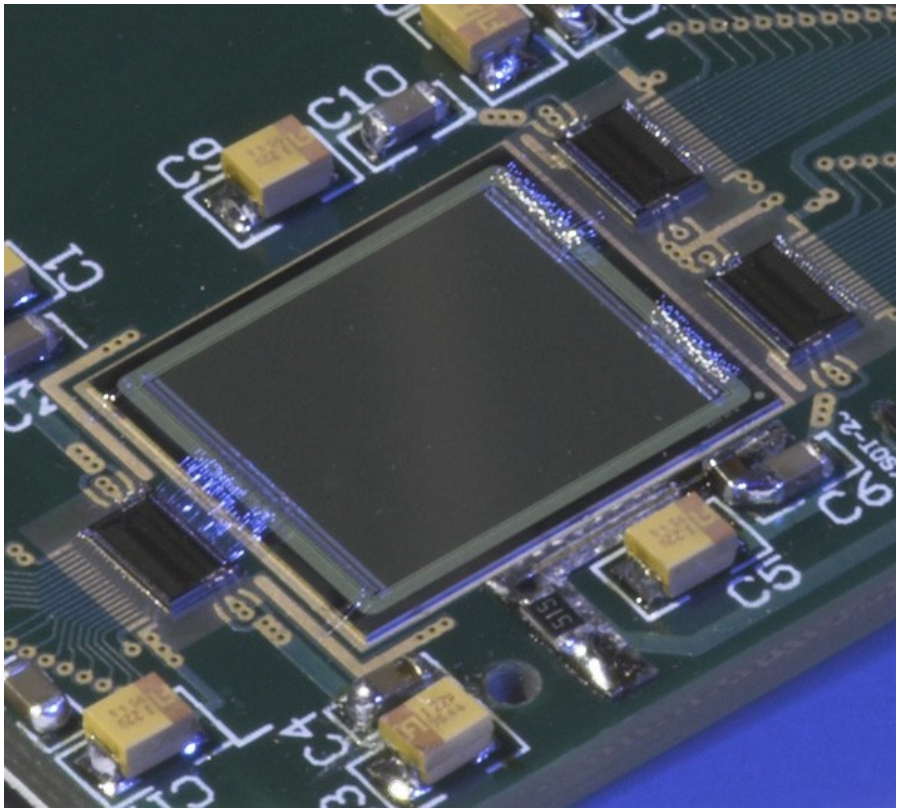


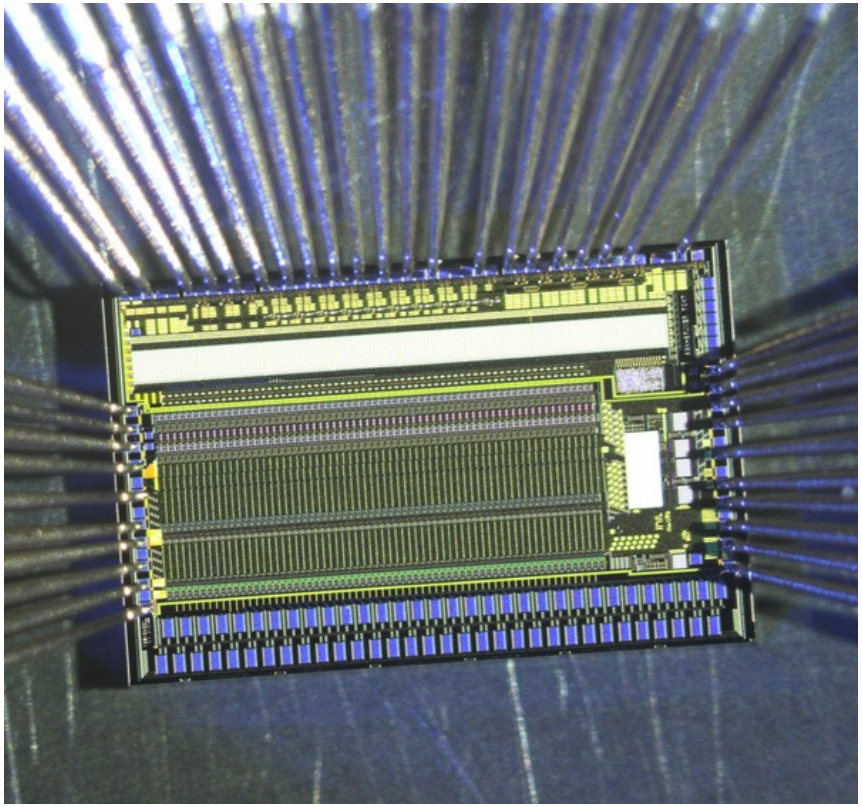


- 6 000 000 channels
- 4200 modules
- Silicon strips
- Binary front-end, 128 channels ASICs

W. Dabrowski – Coordinator
for SST front-end electronics

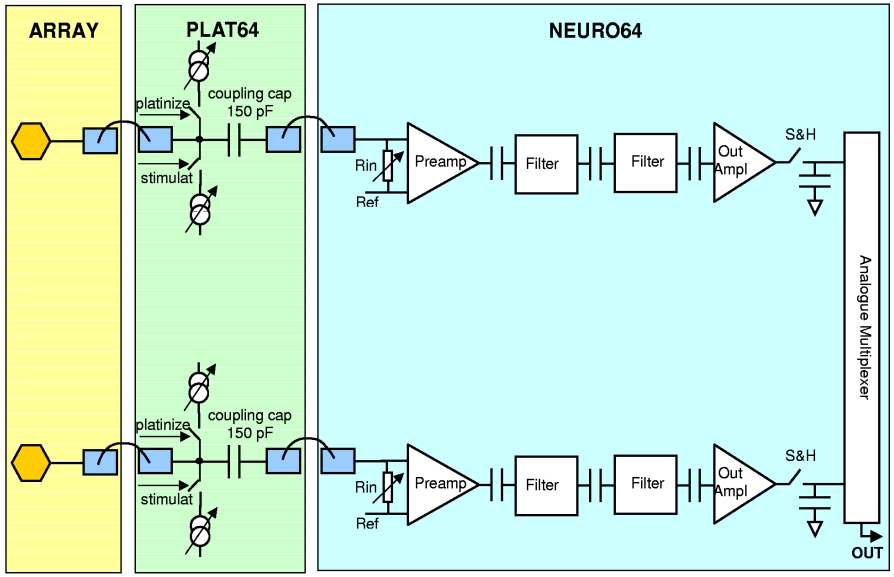
Low noise X-ray position detection system

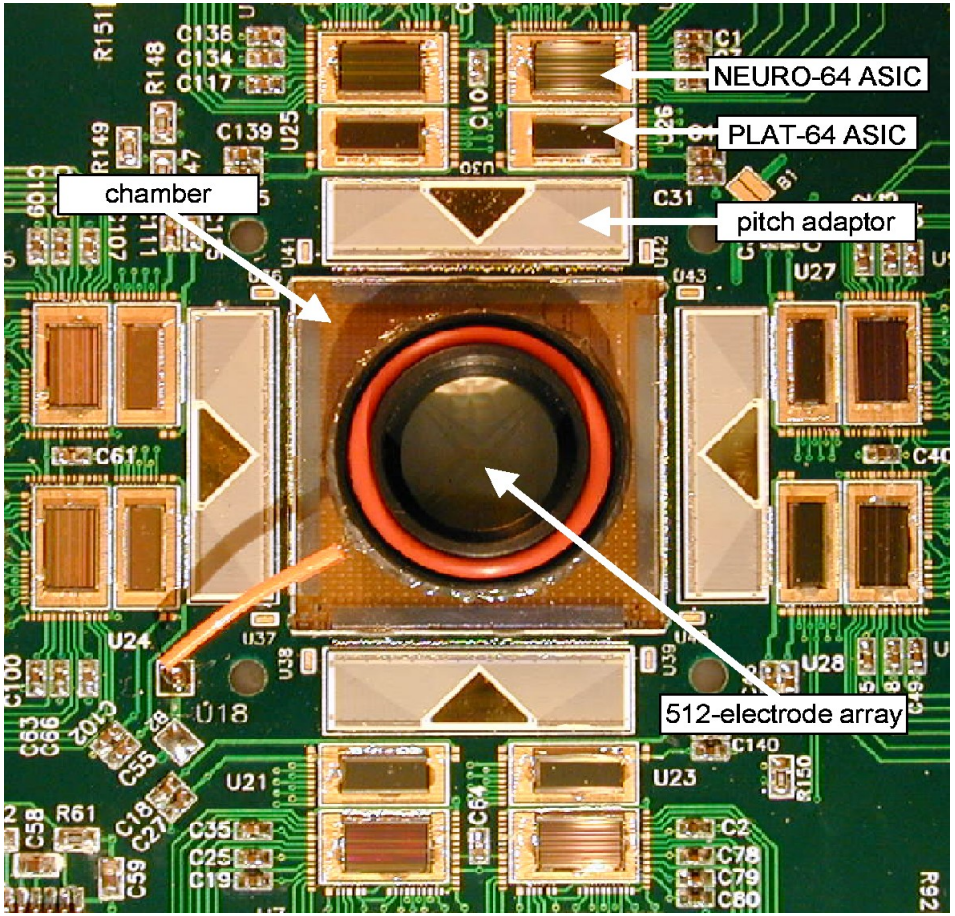




- Readout sustem for X-ray difractometer LynxEye
- Silicon strips
- Binary low noise front-end, 64 channels ASICs

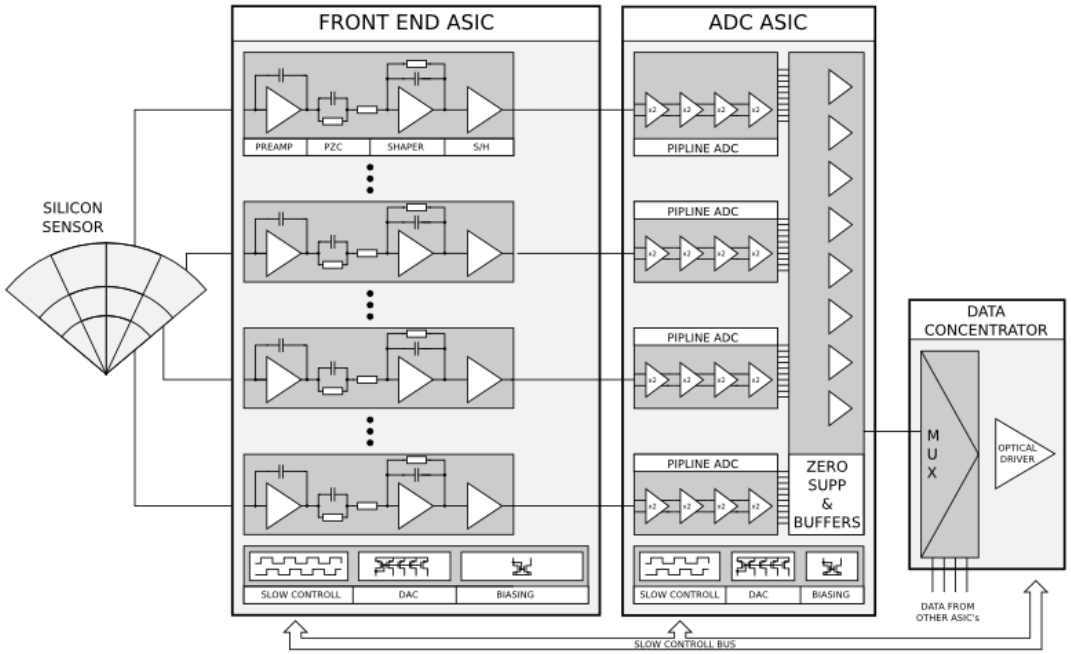
Retina – readout for neuron signals

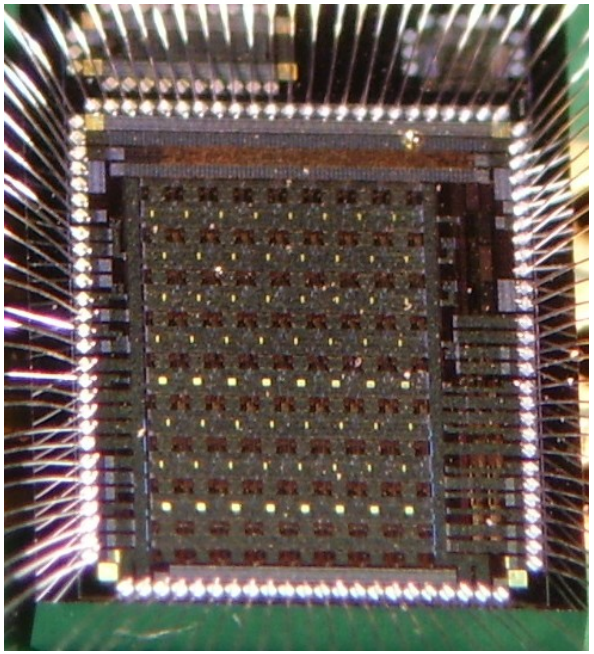


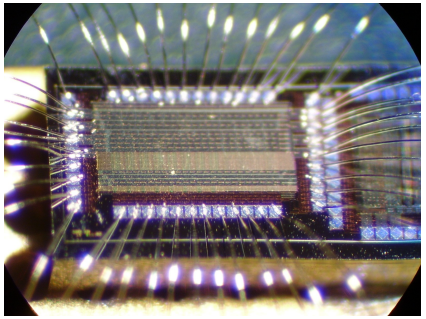


- 512 channels system
- Low noise analog front-end, 64 channels ASICs

LumiCal readout for FCAL – in progress...







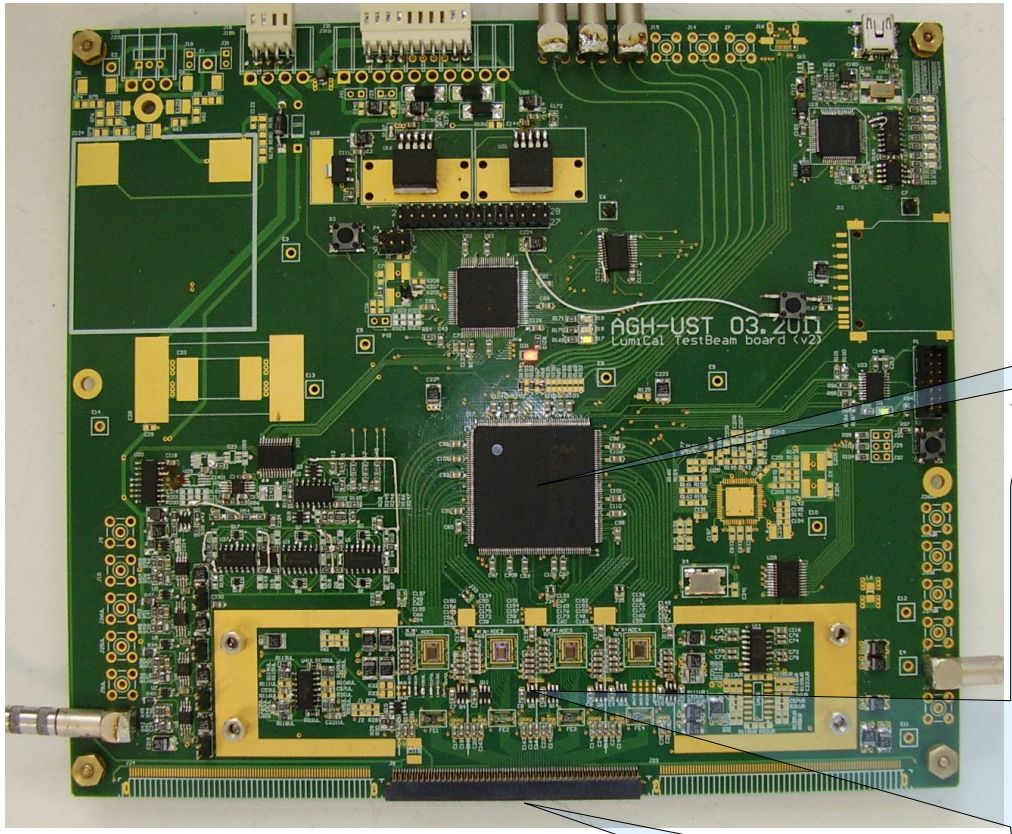
- 8 channels front-end
- Cdet ≈ 0 ÷ 100pF
- 1st order shaper (Tpeak ≈ 60 ns)
- Variable gain

- 8 channels 10 bit pipeline ADC
- Fsampling<=50MHz
- Scalable power
- Digital multiplexer/serializer
- SINAD ~60dB, ENOB 9.7 bit
- INL<0.7LSB, DNL<0.65 LSB

M. Idzik – Technical Coordinator
Of FCAL Collaboration

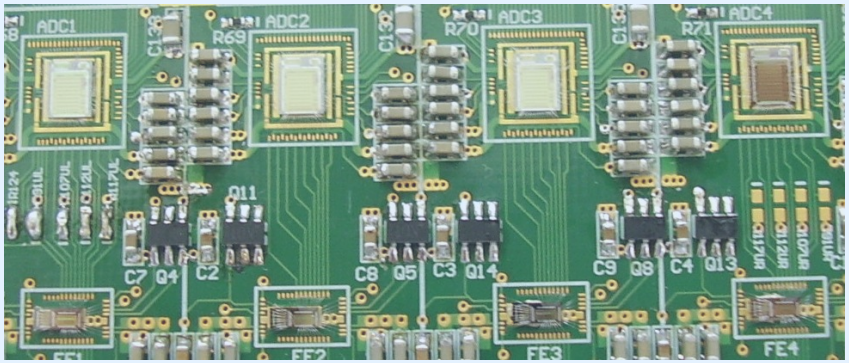
LumiCal detector prototype module - example of readout system

Whole system ASICs+FPGA+PCB designed and mounted at AGH-UST



Data concentrator
Xilinx Spartan 3E

4 pairs of front-end + ADC

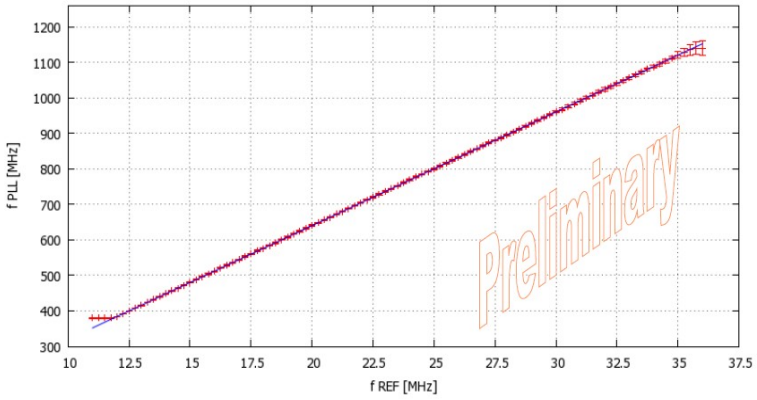


sensor connector

Example of other works - Serialization and fast data transmision 1 GHz PLL based transceiver

Prototype (AMS 0.35um) of PLL block fully functional

- Frequency range 380MHz-1.1GHz
- Power consumption(1GHz) 4.5mW
- Area 160um x 140um



First prototype (AMS 0.35um) of serial transceiver (PLL based), with Clock & Data Recovery, fully functional

- Transmitter (with 8 bit serializer) and receiver (with 8 bit deserializer) fabricated, data coding not yet implemented
- Wide frequency range 640MHz - 980MHz