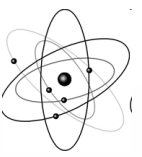




# Krakow interest in Si ASIC design for the future LHCb strip Vertex Locator

- Introduction
- Basic requirements for the front-end chip



# Introduction



- Noise level  $< 1000$  electrons @ 10 pF
- suited for both electron and hole charge collection (switchable)
- peaking time  $< 25$  ns - remainder at 25 ns after peak  $< 20\%$  - 50 ke-dynamic range - 40 MHz sampling clock - 4+ bit ADC per input
- offset correction 4bit tune per channel + 8 bit global
- ADC range tunable per 32 channels Digital:
- common mode subtractions (e.g. over 32 channels)
- can it be done at the analog level?
- clustering, 3 (5?) strips
- seed threshold + inclusion threshold
- zero suppression - derandomizing buffer, size t.b.d. - serializer 5 Gbit/s General: - 128 channels per chip
- power  $< 4$  mW/channel (but up to 8mW/ch is no problem)
- radiation hardness  $> 50$  MRad TID (and  $5E14$  1MeV neq)