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Open Logic –open-source FPGA Standard Library

Tuesday 20 May 2025 15:55 (35 minutes)

Open Logic is the fastest-growing open-source HDL standard library on the market, as measured by GitHub stars. It simplifies FPGA development with reusable, modular, and vendor-independent components. Bridging the gap between hand-optimized HDL code and high-level abstractions like HLS and IP integration, it offers a balanced approach to effort and resource optimization. With a strong focus on code quality, verification, documentation, and ease of use, Open Logic ensures both reliability and accessibility.

This presentation will highlight the library's philosophy, its place in the FPGA design landscape, and the advantages it offers, including device independence and reduced maintenance effort. Attendees will explore key features such as FIFOs, AXI utilities, and CAMs, and discover how to integrate Open Logic effectively into their projects.

Talk's Q&A

End of talk

Will you be able to present in person?

Yes

Talk duration

20'+10'

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Session Classification: Sharable HDL cores

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