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Error-Redundant Implementation of Commercial IP Cores: A Practical Example

Tuesday 20 May 2025 17:55 (30 minutes)

The reuse of predefined IP cores is a well-established practice in semiconductor design, offering cost and technical advantages. However, commercial providers must meet diverse implementation requirements, ensuring compliance with specifications while optimizing power, frequency, gate utilization, and feature scope. Additionally, IP cores must function reliably across FPGA and ASIC platforms, often under harsh conditions.
Fault tolerance demands techniques like triple-mode redundancy, error correction codes, and fail-safe state machines—but the greater challenge lies in verification and validation. These processes are time-intensive and costly, especially for third-party certification.
This paper presents a case study on implementing, verifying, and validating a PSI5 Controller IP core developed by SmartDV to meet ASIL-B certification under ISO 26262. It highlights key challenges and best practices for designing error-redundant IP cores.

Talk's Q&A

During the talk

Talk duration

20'+10'

Will you be able to present in person?

Yes

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