2nd FPGA Developers' Forum (FDF) meeting



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Standardizing SoC Development at CERN: A Build System for Xilinx Platforms

Wednesday 21 May 2025 16:50 (30 minutes)

With the increasing adoption of SoC-based systems at CERN, new initiatives have been put in place to ensure that systems of similar form share as many components (hardware, gateware and software) as possible. As part of the DI/OT framework - now being integrated also into CERN's ATS SoC Common Framework Project - a new standardized build system has been developed to generate boot images for these platforms. This build system is modular, expandable and designed to streamline the HDL synthesis and compilation of Xilinx SoC-based projects, with strong emphasis on re-usability and standardization. It is also CI-friendly, aligning with CERN IT's new CI4FPGA developments for CI runners and Docker images. The use of this build system will be encouraged by the ATS sector, which constitutes Work Package Task 1.1 within the SoC Common Framework.

Talk's Q&A

During the talk

Talk duration

20'+10'

Will you be able to present in person?

Yes

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Session Classification: Solutions to everyday digital design problems

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