Brookhaven National Laboratory

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U.S. DEPARTMENT of ENERGY | Office of Science

Low Jitter Frame Clock Recovery in Xilinx UltraScale+ Transceivers

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FPGA Developers' Forum 2025 – CERN

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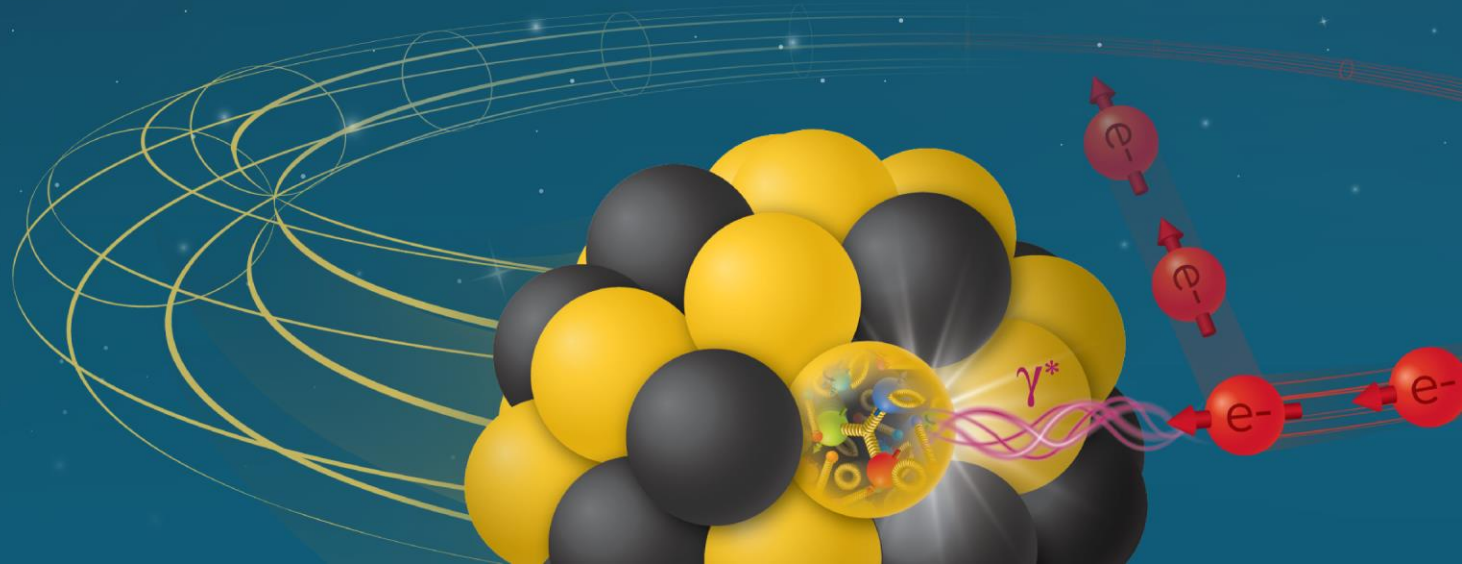
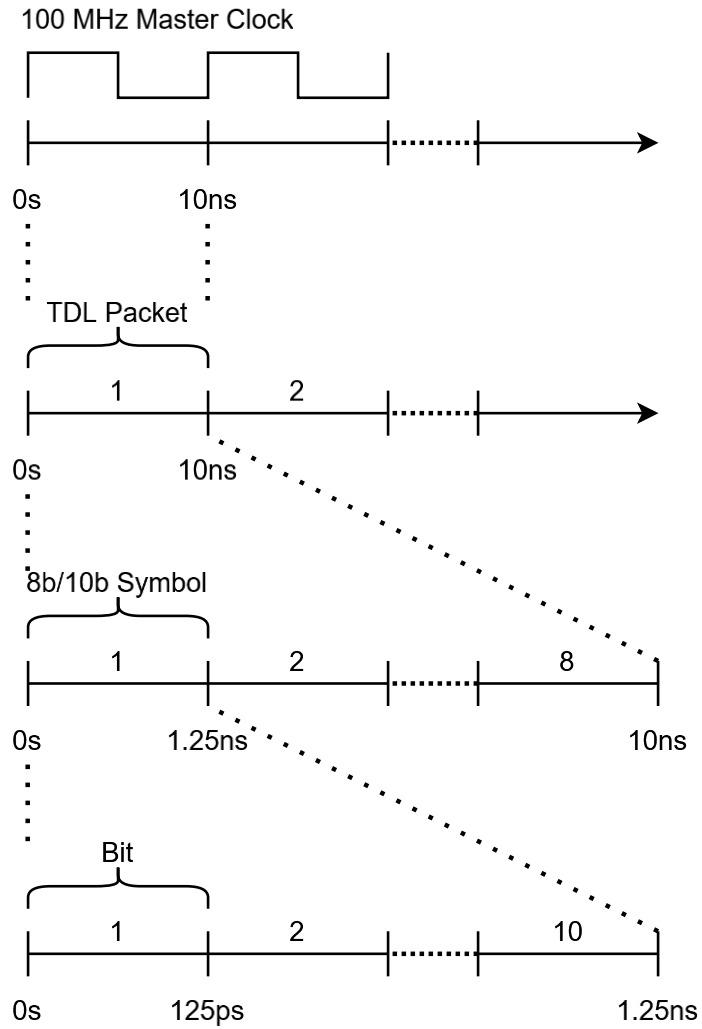
Electron-Ion Collider



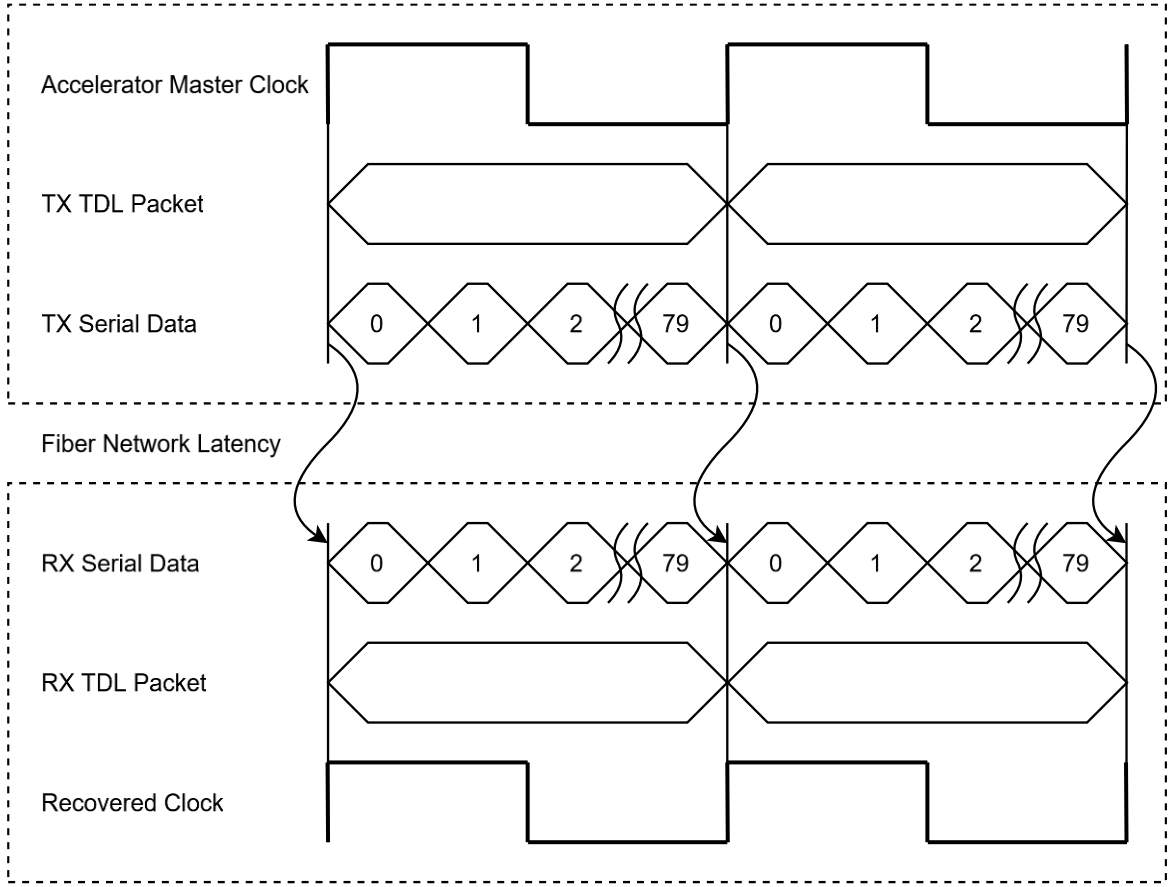
EIC Timing Data Link (TDL)

- 100 MHz Accelerator Master Clock
  - Used to synthesize RF and Beam Sync clocks
- 64-bit TDL Packets transmitted continuously
- 8b/10b byte encoding yields 80 bits per TDL Packet
- Line rate of 8 Gbps
  - 100 MHz * 80 bits = 8 Gbps
- Transmitted long distances via SFP+ fiber modules



Clock Distribution

- Transmitter serializes TDL Packet frames synchronous with master clock
- Receiver deserializes TDL Packet frames and recovers master clock from data frame clock
- Synchronous clock recovery is trivial
- Deterministic phase alignment requires careful consideration



Transmitter Clock

- PISO parallel clock controls data framing
  - Internally divided down serial clock
  - Nondeterministic phase relationship with MGTREFCLK
- Set TXOUTCLK to TXOUTCLKPMA
- Must align TXOUTCLK with Accelerator Master Clock
- Accelerator Master Clock drives MGTREFCLK
- The Phase Interpolator (PI) can be manually controlled via the Dynamic Reconfiguration Port (DRP)

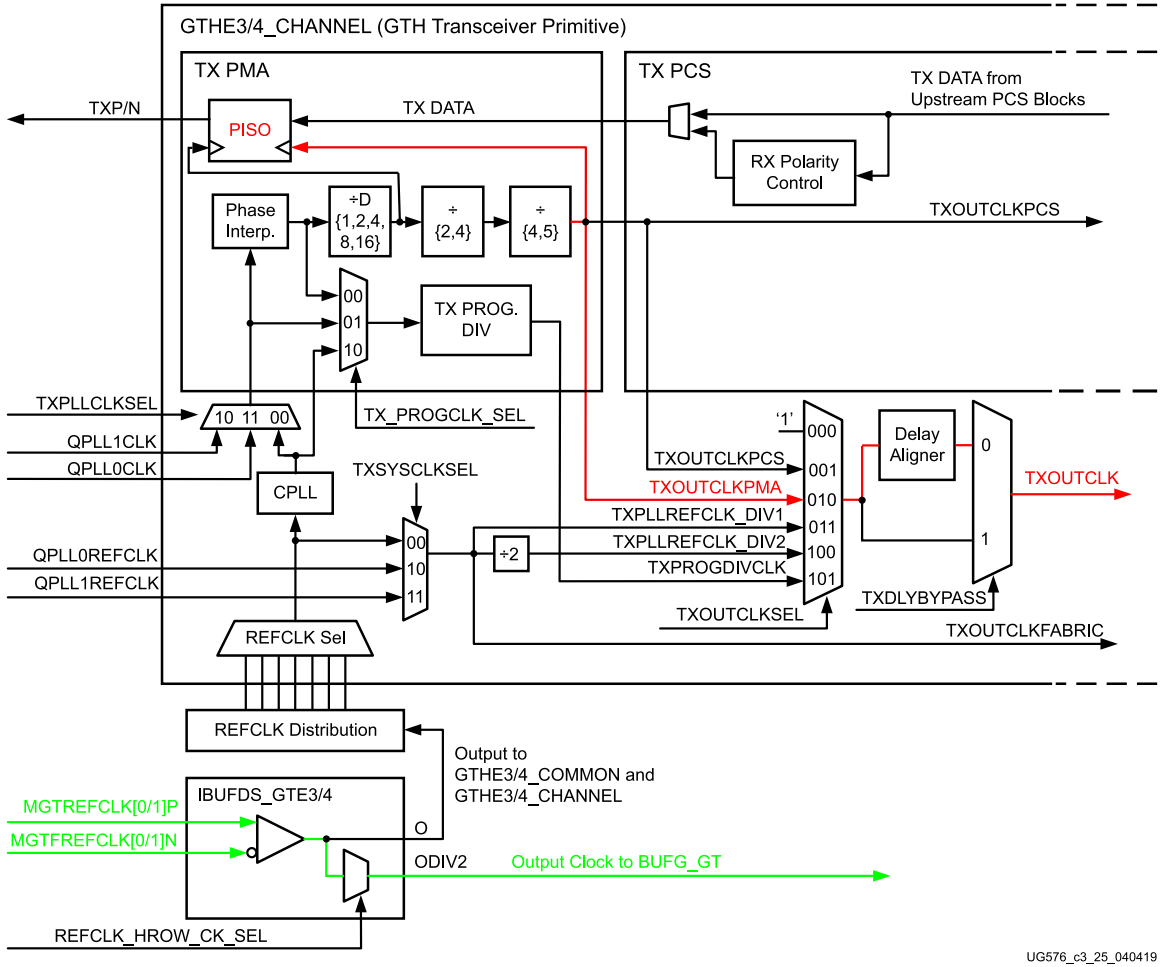
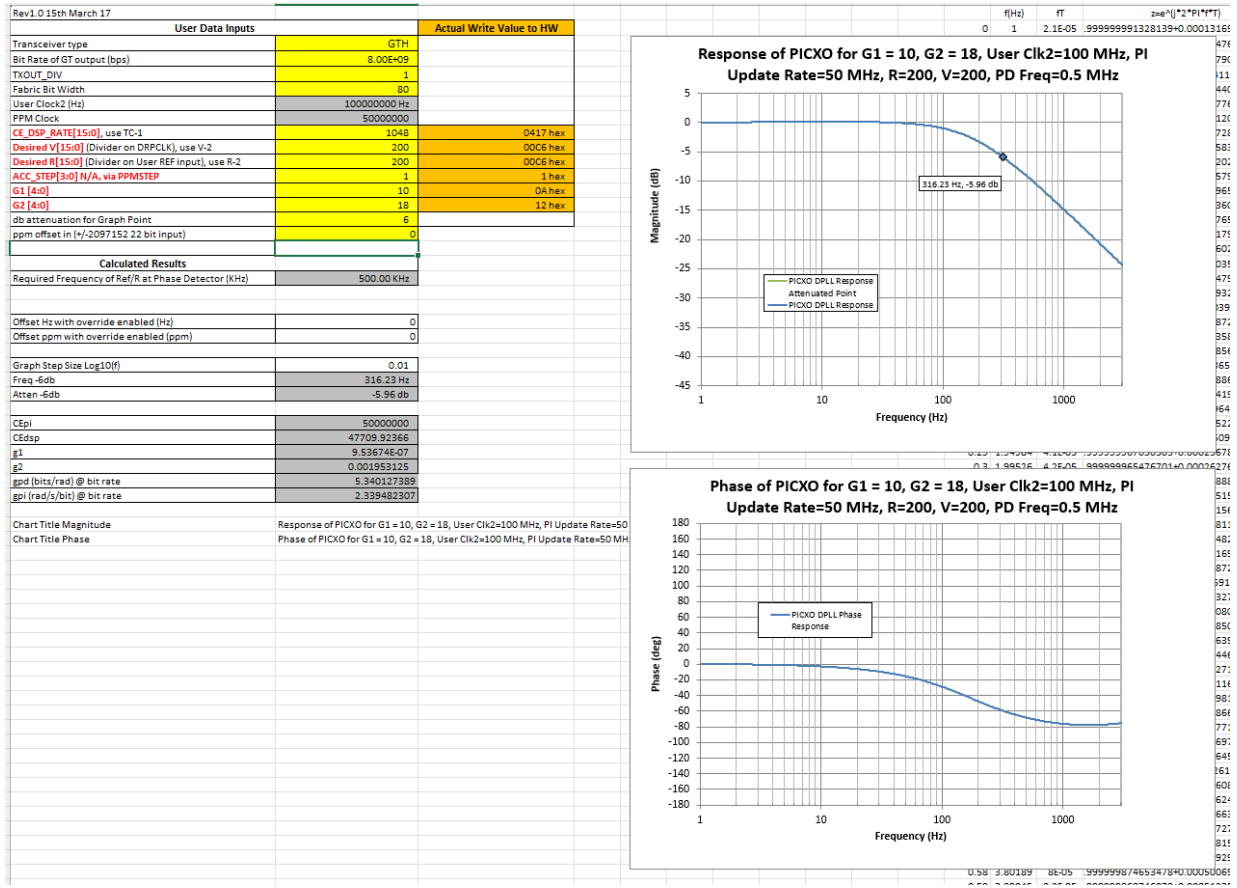


Figure 3-29: **TX Serial and Parallel Clock Divider**

Source: UG576 UltraScale Architecture GTH Transceivers User Guide

Transmitter Phase Control

- Xilinx PICXO FRACXO IP Core provides TXOUTCLK alignment functionality by modulating PI
- Allows the GT TXOUTCLK to be phase aligned to a reference clock from fabric
  - MGTREFCLK routed to fabric via BUFG_GT
- Convenient tool provided for calculating optimal digital PLL loop gains



Rev1.0 15th March 17		
User Data Inputs		**Actual Write Value to HW**
Transceiver type	GTH	
Bit Rate of GT output (bps)	8.00E+09	
TXOUT_DIV	1	
Fabric Bit Width	80	
User Clock2 (Hz)	100000000 Hz	
PPM Clock	50000000	
CE_DSP_RATE[15:0], use TC-1	1048	0417 hex
Desired V[15:0] (Divider on DRPCLK), use V-2	200	00C6 hex
Desired R[15:0] (Divider on User REF input), use R-2	200	00C6 hex
ACC_STEP[3:0] N/A, via PPMSTEP	1	1 hex
G1 [4:0]	10	0A hex
G2 [4:0]	18	12 hex
db attenuation for Graph Point	6	
ppm offset in (+/-2097152 22 bit input)	0	
Calculated Results		
Required Frequency of Ref/R at Phase Detector (KHz)	500.00 KHz	
Offset Hz with override enabled (Hz)	0	
Offset ppm with override enabled (ppm)	0	
Graph Step Size Log10(f)	0.01	
Freq -6db	316.23 Hz	
Atten -6db	-5.96 db	
CEpi	50000000	
CEdsp	47709.92366	
g1	9.53674E-07	
g2	0.001953125	
gpd (bits/rad) @ bit rate	5.340127389	
gpi (rad/s/bit) @ bit rate	2.339482307	
Chart Title Magnitude	Response of PICXO for G1 = 10, G2 = 18, User Clk2=100 MHz, PI Update Rate=50	
Chart Title Phase	Phase of PICXO for G1 = 10, G2 = 18, User Clk2=100 MHz, PI Update Rate=50 MH	

Receiver Clock Recovery

- SIPO Parallel Clock controls data framing
  - Internally divided down serial clock
  - Can be sent to fabric via RXOUTCLK then output via OBUFDS to IO pins
- Phase shift SIPO Parallel Clock to align data
  - Buffer Bypass with RXSLIDE PMA mode
  - Phase shift granularity is limited by the SIPO Serial Clock period
  - Reset and retry if aligned on alternate edge
- Problems
  - RXSLIDE PMA can cause the Buffer Bypass Delay Aligner to lose alignment
  - Inconsistent phase across resets due to Auto Alignment algorithm
  - Delay Aligner introduces nonlinear phase drift
  - FPGA clocking network introduces phase jitter

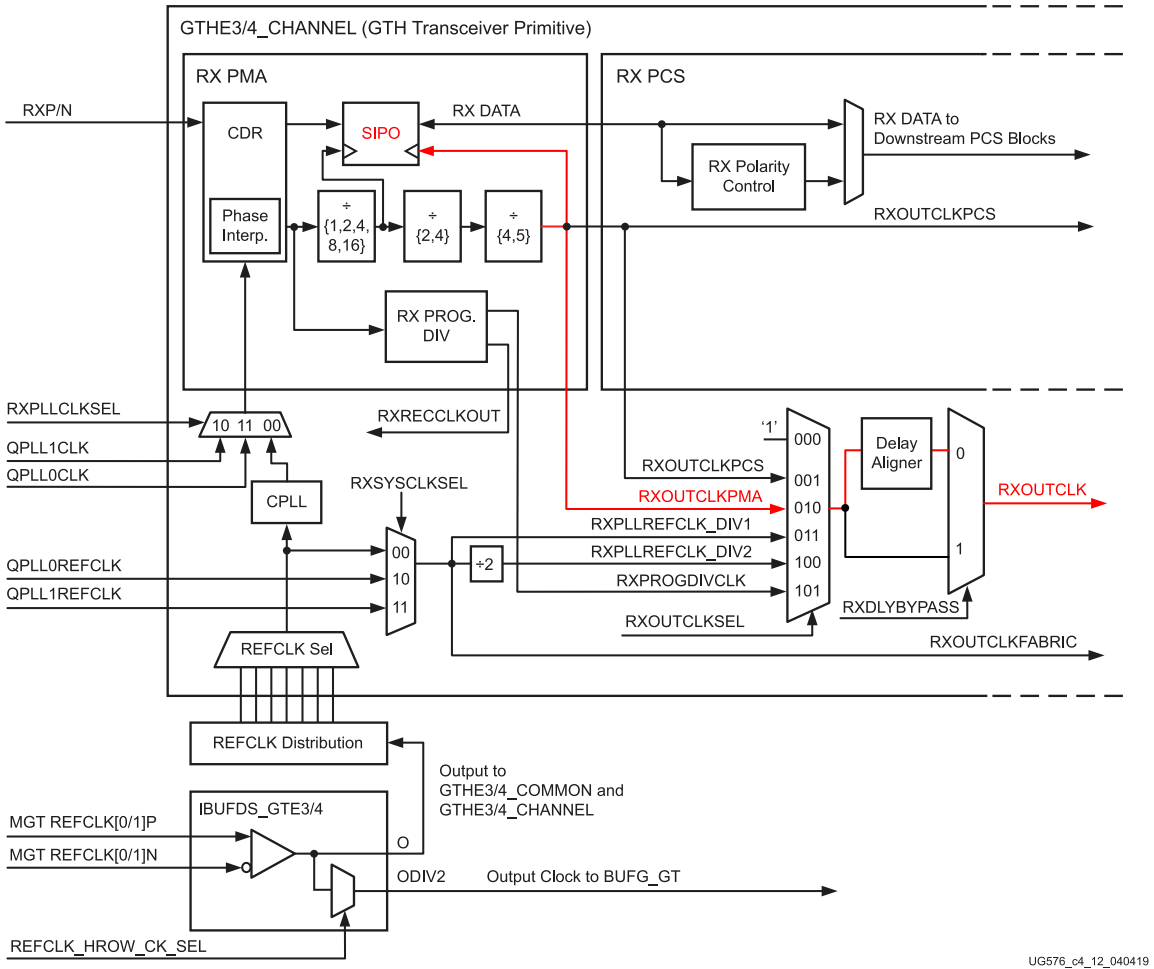


Figure 4-17: **RX Serial and Parallel Clock Divider**

Source: UG576 UltraScale Architecture GTH Transceivers User Guide

Receiver RXRECCLKOUT

- Benefits
  - Dedicated clock routing within GT
  - Output via OBUFDS_GTE4 to MGTREFCLK pins
  - Not affected by Delay Aligner
  - Does not change between builds
- Problem
  - No phase relationship with SIPO Parallel Clock for alignment with data frames
- Solution
  - Manually align SIPO Parallel Clock with RXRECCLKOUT

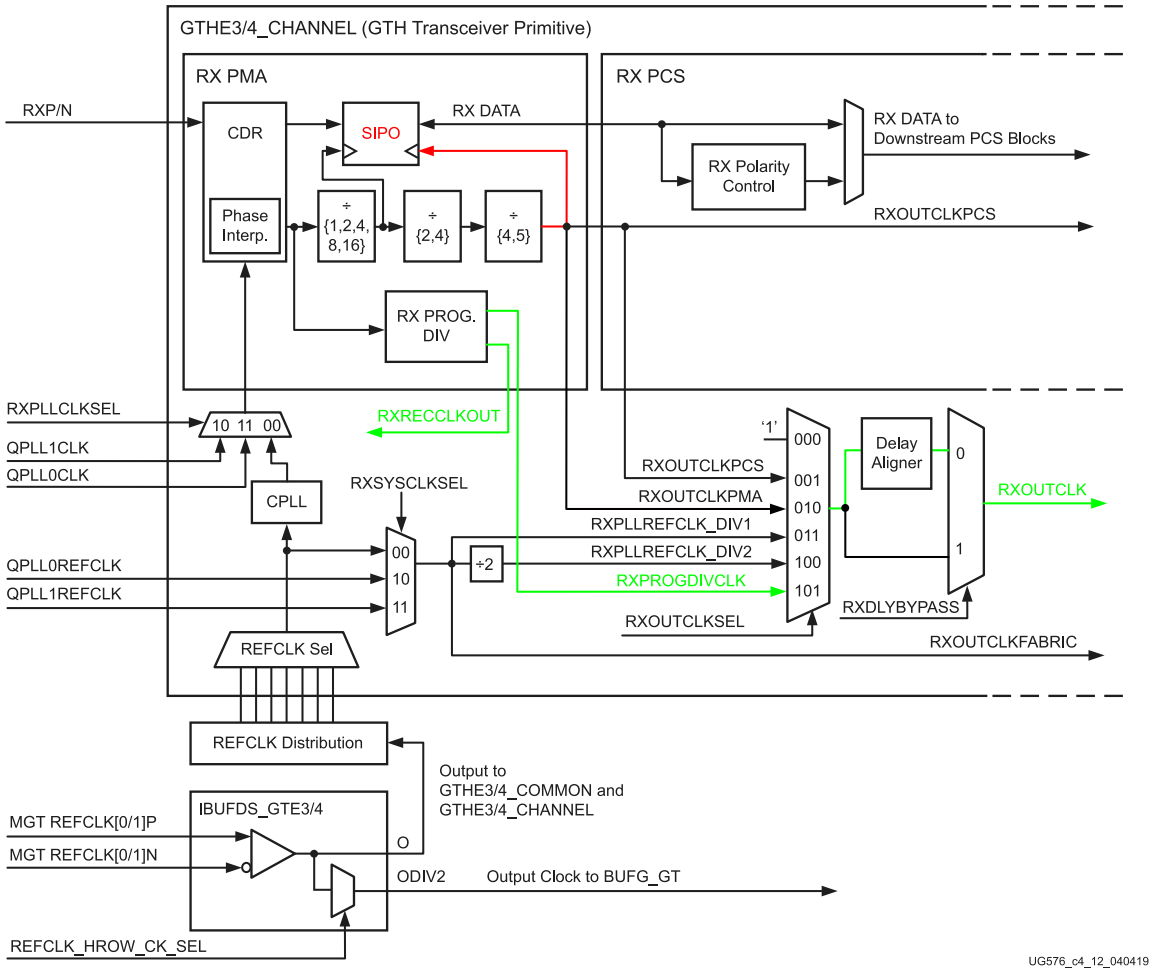
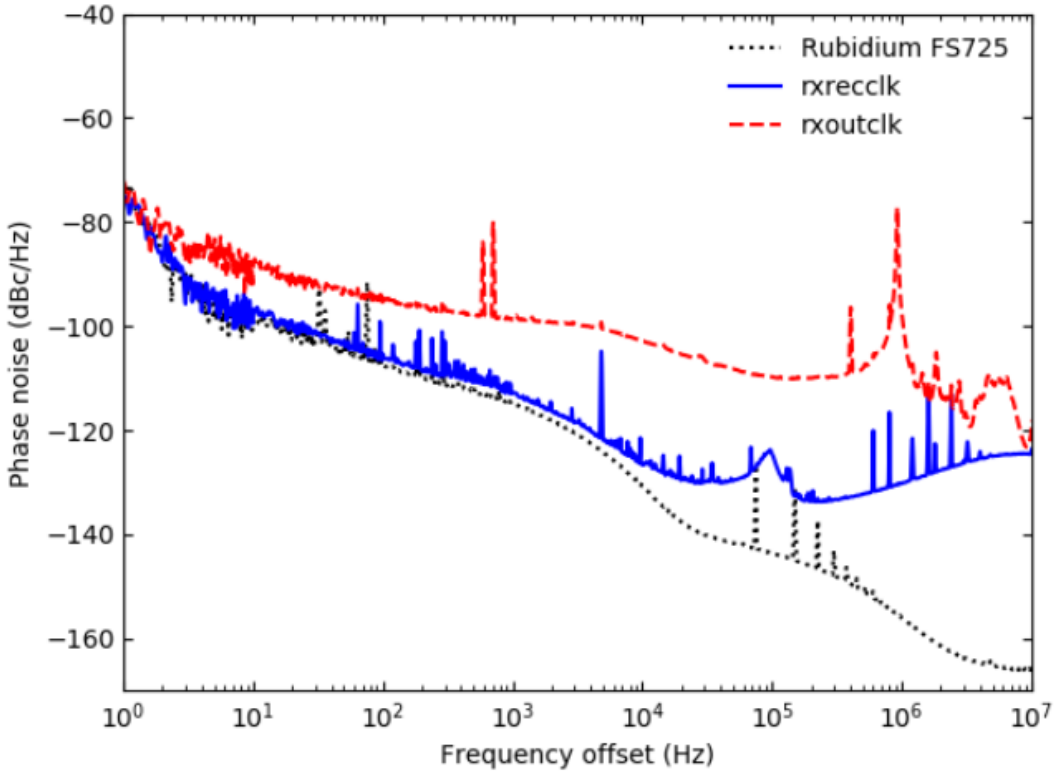


Figure 4-17: **RX Serial and Parallel Clock Divider**

Source: UG576 UltraScale Architecture GTH Transceivers User Guide

Phase Noise Comparison

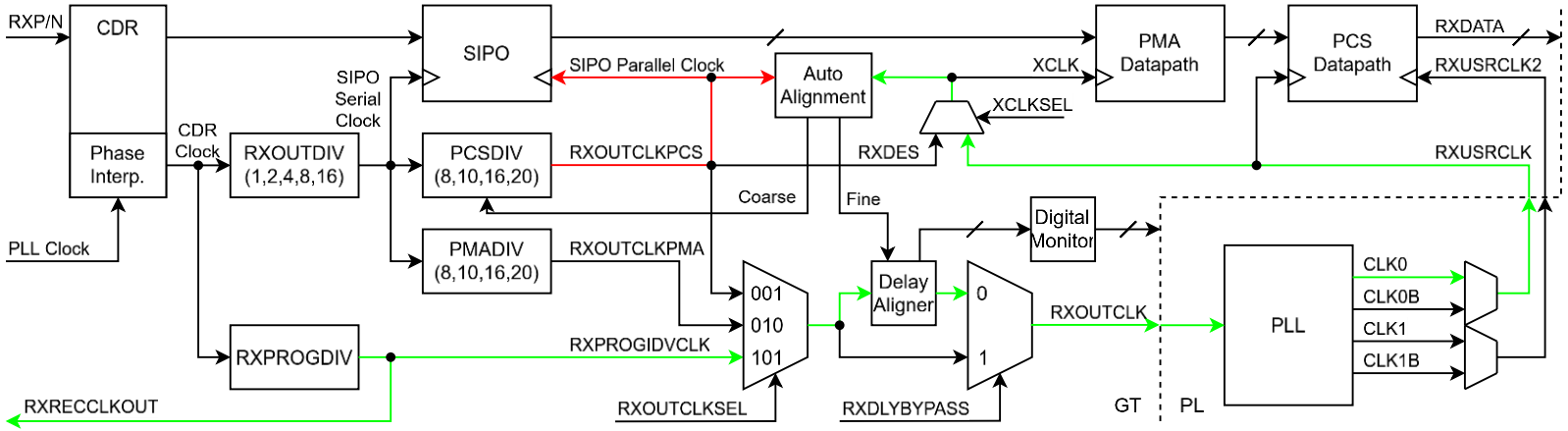
- Measurements taken by the High Precision Timing Distribution (HPTD) project group at CERN
- Up to 20 dB phase noise improvement of RXRECCLKOUT vs RXOUTCLK
- Lower integrated phase noise eases requirements on the subsequent clock cleaner PLL



Credit: E. Mendes, S. Baron, C. Soos, J. Troska, and P. Novellini, “Achieving picosecond-level phase stability in timing distribution systems with Xilinx ultrascale transceivers,” IEEE Trans. Nucl. Sci., vol. 67, no. 3, pp. 473–481, Mar. 2020.

RXRECCLKOUT Phase Alignment

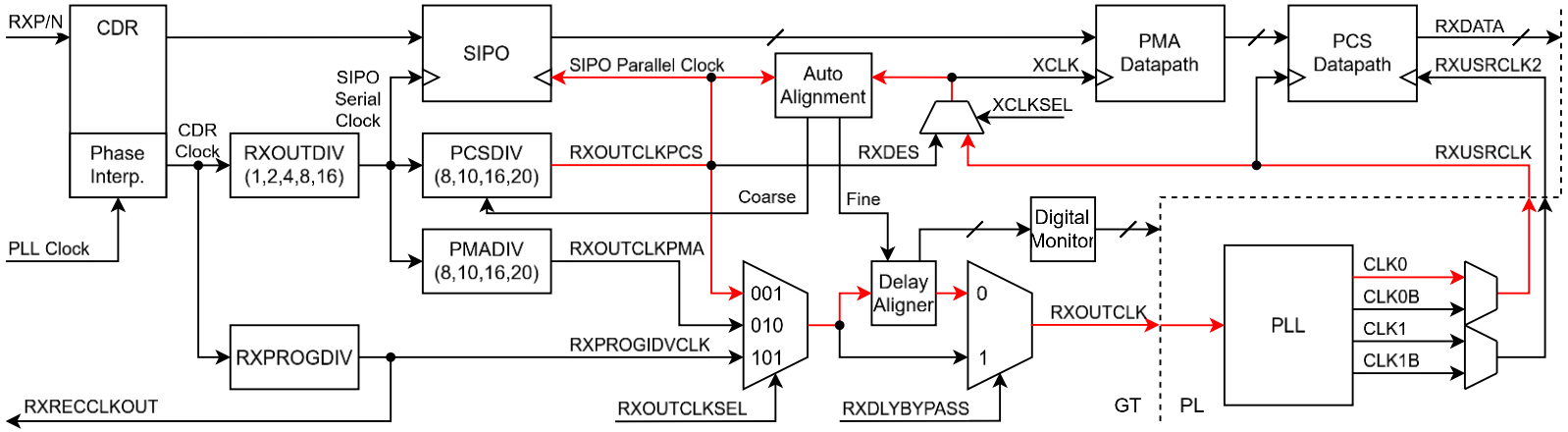
- How to align SIPO Parallel Clock and RXRECCLKOUT
  1) Enable Buffer Bypass mode
  2) Set RXOUTCLK to RXRECCLKOUT by selecting RXPROGDIVCLK
  3) Enable Auto Alignment to shift the SIPO Parallel clock in phase with XCLK
- Problems
  - RXPROGDIVCLK is delayed through the clock routing to XCLK before alignment
  - RXSLIDE PMA mode cannot be used for data alignment without also losing RXRECCLKOUT phase alignment



XCLK Skew Measurement

- How to measure XCLK skew
  1) Set RXOUTCLK to SIPO Parallel Clock by selecting RXOUTCLKPCS
  2) Enable Auto Alignment
  3) Read the stable Delay Aligner tap number
- Coarse phase shift has no effect
- Fine phase shift must compensate for entire path delay using Delay Aligner

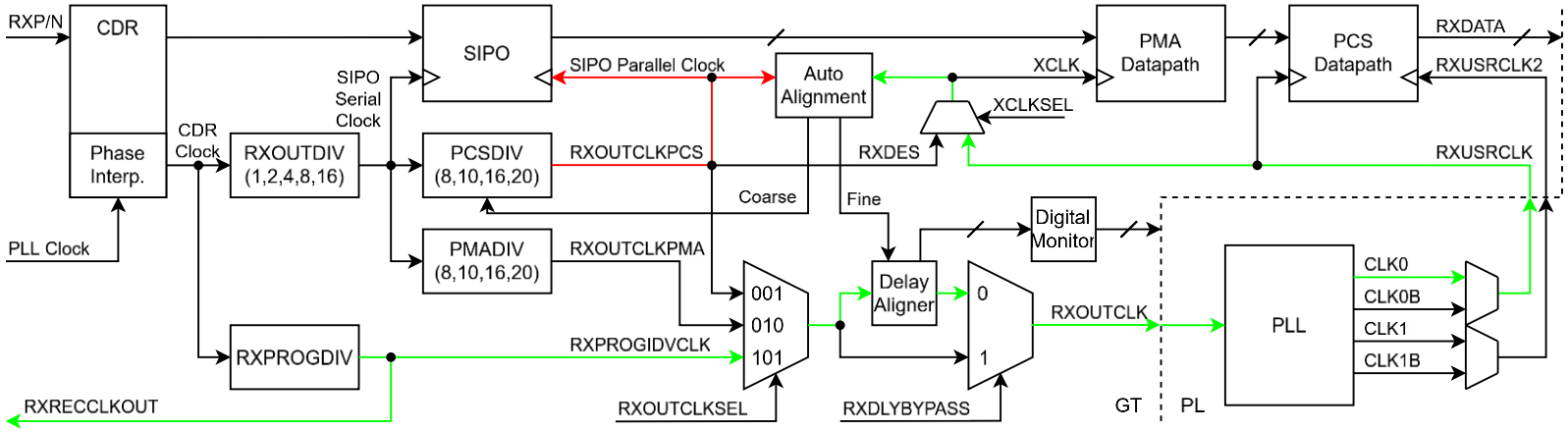
- GT configuration
  - RXPH_MONITOR_SEL = 0x03
  - DMONITOR_CFG1 = 0x03
  - DMONITOR[7:0] outputs an 8-bit value representing the Delay Aligner tap number
- Delay Aligner is a 256-tap calibrated delay chain with a 4 ns range
  - Each delay tap is 15.625 ps



RXRECCLKOUT Phase Measurement

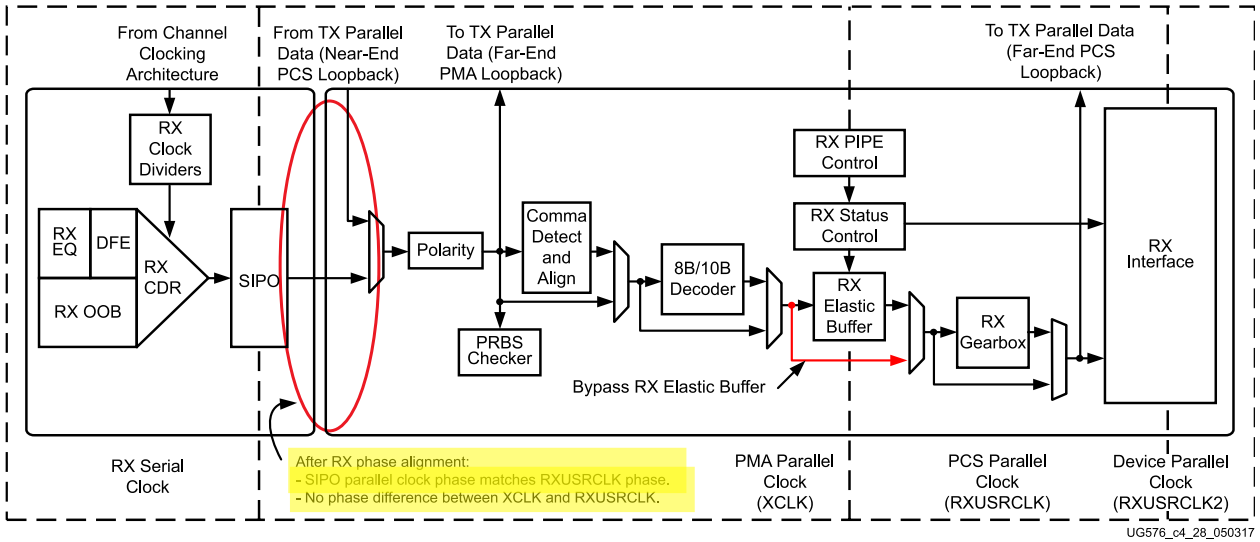
- How to measure relative phase between SIPO Parallel Clock and RXRECCLKOUT
  1) Set RXOUTCLK to RXPROGDIVCLK
  2) Enable RXSLIDE PMA mode via DRP to manually shift SIPO Parallel Clock
  3) Count the number of RXSLIDE shifts required for the Delay Aligner tap number to match the measured XCLK skew
  4) Shift to restore original clock alignment

- Clock Data Recovery (CDR) Clock generates both SIPO Parallel Clock and RXRECCLKOUT
- The measured number of RXSLIDE shifts represents the relative clock phase in integer number of CDR Clock periods
- Original phase set by Auto Alignment must be restored for proper Clock Domain Crossing (CDC)



RXRECCLKOUT Phase Compensation

- Cannot have SIPO Parallel Clock aligned with RXRECCLKOUT while maintaining valid CDC
- But the ultimate goal is to align RXRECCLKOUT with RXDATA frames
  - Can be achieved by compensating for SIPO Parallel Clock relative phase
- How to align RXRECCLKOUT with RXDATA frames
  1) Enable RXSLIDE PCS mode via DRP to manually barrel shift RXDATA
  2) Shift RXDATA by the measured number of CDR Clocks between SIPO Parallel Clock and RXRECCLKOUT phase
- RXDATA now appears as if SIPO Parallel Clock and RXRECCLKOUT are aligned
  - Independent of XCLK skew



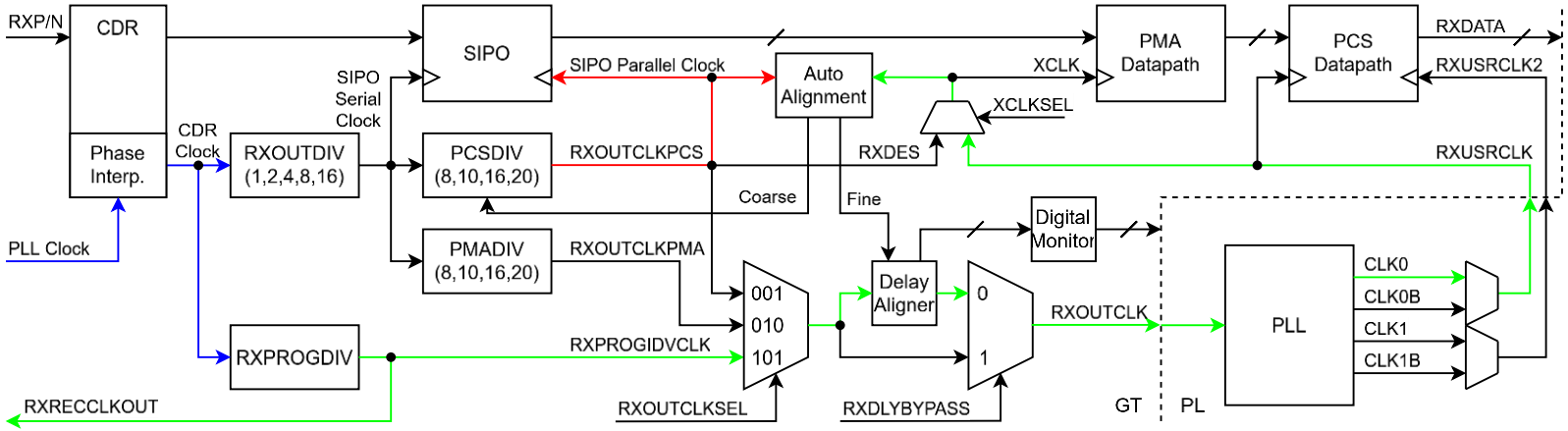
Source: UG576 UltraScale Architecture GTH Transceivers User Guide

Figure 4-34: **Using RX Phase Alignment**

RXDATA Comma Alignment

- RXRECCLKOUT and RXDATA frames can now be deterministically aligned
  - But RXDATA is not yet comma aligned
  - Cannot use RXSLIDE PCS or PMA without losing RXRECCLKOUT alignment
- Must manually phase shift CDR Clock
  - Shifts SIPO Parallel Clock and RXRECCLKOUT simultaneously maintaining alignment

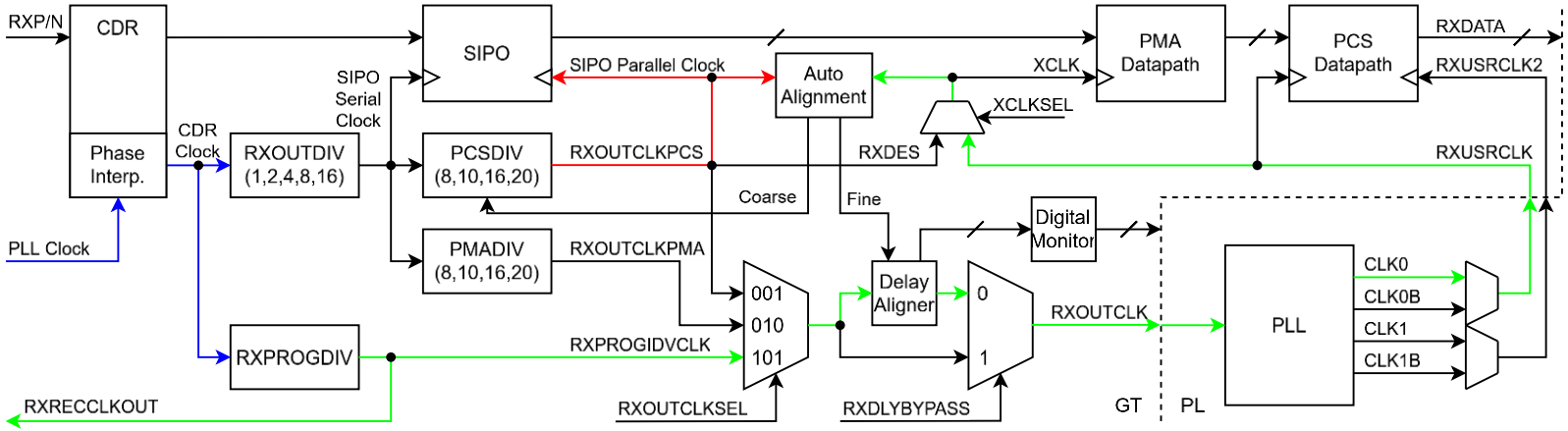
- CDR Clock
  - Generated from PLL Clock through CDR PI
  - PI is a 128-tap calibrated delay chain
    - Each delay tap is 1/128th of one PLL Clock period
  - Can be phase shifted by manually controlling the PI tap number
- Burst-Mode Clock Data Recovery with GTH and GTY Transceivers XAPP1252
  - Demonstrates how to read and control the PI tap number



CDR Clock Phase Shift

- GT configuration
  - DMONITOR_CFG1 = 0x01
  - DMONITOR[6:0] outputs a 7-bit value representing the PI tap number
  - See XAPP1252 for all required attribute settings
- Manual CDR PI control
  - RXCDR_CFG1[15:9]
    - DRP register 0x00F
    - Write new value for 7-bit PI tap number
  - Pulse RXCDROVRDEN high to apply the new PI tap number

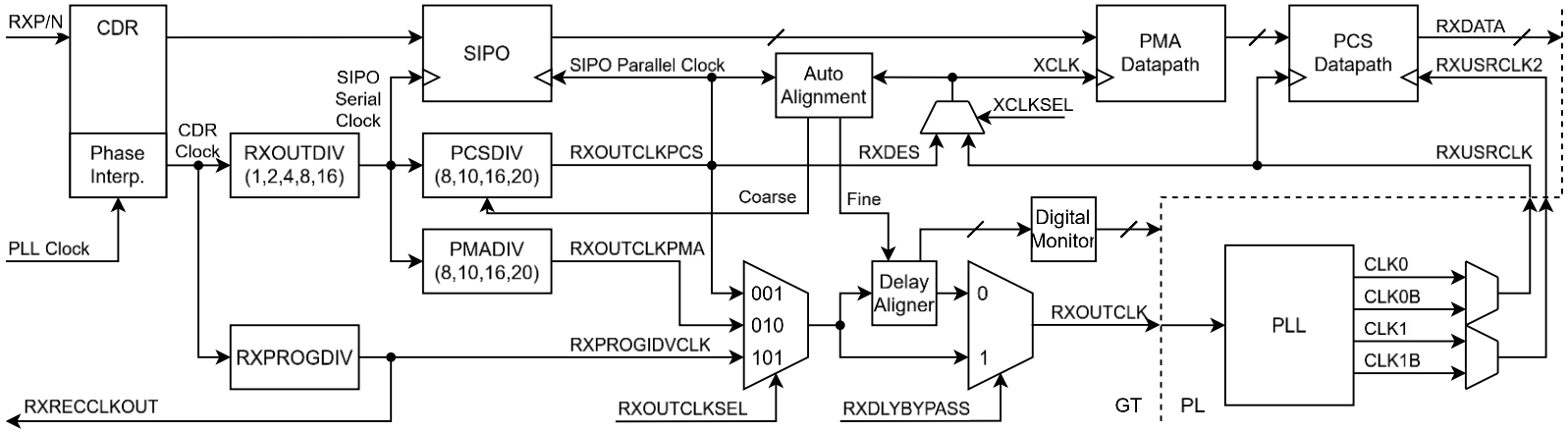
- How to manually phase shift CDR Clock in Unit Interval (UI) increments
  1) Read the current PI tap number
  2) Write new values for the PI tap number in quick succession starting with the current value and incrementing until rollover at 128
  3) Continue incrementing until it is returned to its original value
- This procedure affects a single UI phase shift in the CDR Clock



Summary

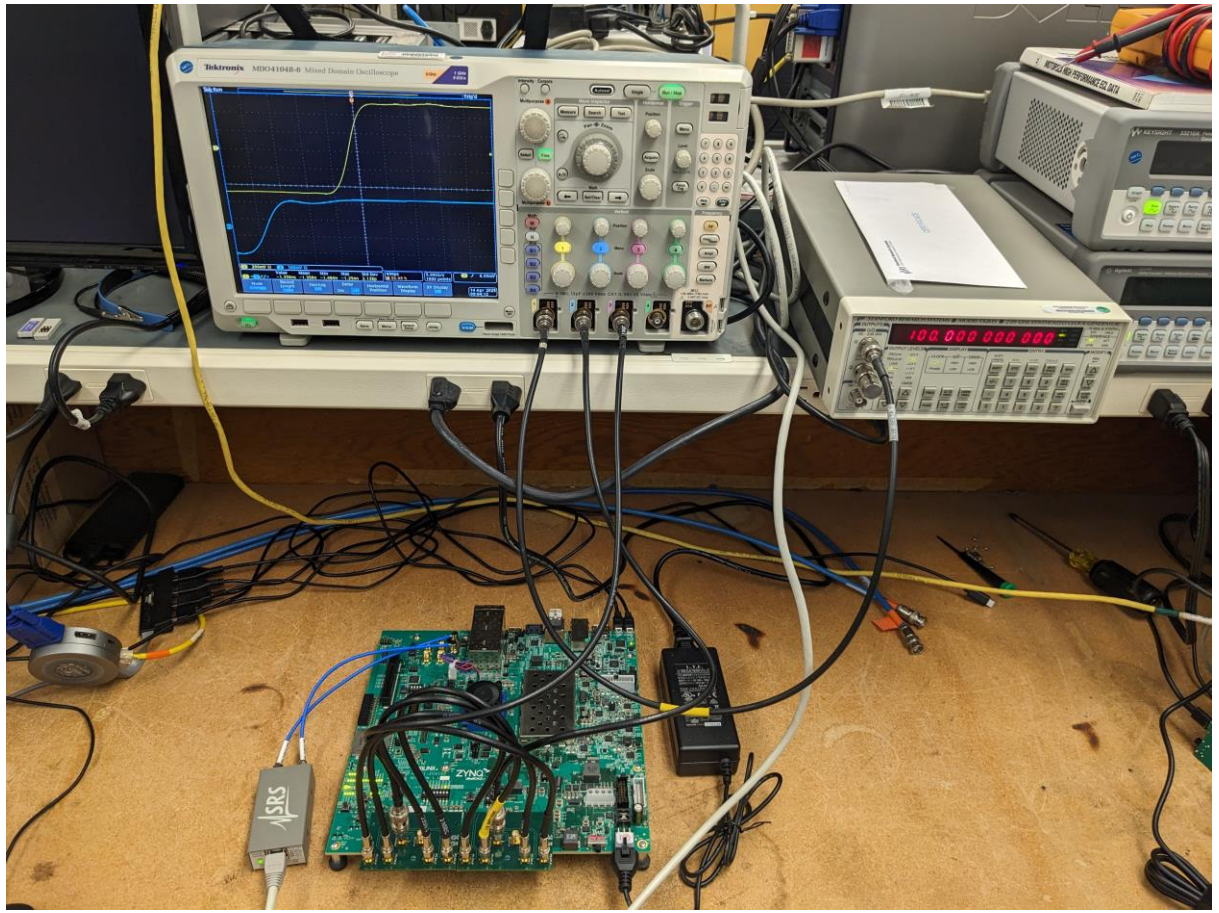
1) Align SIPO Parallel Clock and RXRECCLKOUT using Buffer Bypass Auto Alignment
2) Measure and compensate for XCLK skew using RXSLIDE
3) Comma align RXDATA by manually phase shifting CDR Clock

- Potential Complications
  - If one RXRECCLKOUT half period is larger than the 4 ns Delay Aligner range
    - XCLK skew measurement may require a phase shifted version of RXOUTCLK
  - SIPO Parallel Clock RXSLIDE PMA phase shift granularity limited by RXOUTDIV
    - May have to reset RXPROGDIV and retry if they are on alternate CDR Clock edges
  - If RXUSRCLK2 different than RXUSRCLK
    - SIPO Parallel Clock frequency must be temporarily changed for XCLK skew measurement
    - PLL or MMCM required to generate RXUSRCLK



Testing

- Clock recovery test with 2 independent GTH transceiver channels
  - 64-bit words, 100 MHz MGTREFCLK, 8 Gbps line rate, 40-bit GTH internal datapath, 200 MHz RXUSRCLK, equalizer in LPM mode
  - Copper SMA loopback via FMC breakout
  - No clock skew variations measured across hundreds of reset cycles down to 1 ps measurement resolution of oscilloscope
- Equipment
  - Zynq UltraScale+ ZCU102 Evaluation Board XCZU9ED-FFVB1156-2-E
  - Stanford Research Systems CG635 Clock Generator with 0.0001 ppm Rb timebase
  - Tektronix MDO4104B-6 5 GS/s oscilloscope with acquisition averaging enabled



References

[1] E. Mendes, S. Baron, C. Soos, J. Troska, and P. Novellini, “Achieving picosecond-level phase stability in timing distribution systems with Xilinx ultrascale transceivers,” IEEE Trans. Nucl. Sci., vol. 67, no. 3, pp. 473–481, Mar. 2020.

[2] Xilinx, “UltraScale Architecture GTH Transceivers User Guide UG576 (v1.7.1),” Aug. 18, 2021. https://docs.amd.com/v/u/en-US/ug576-ultrascale-gth-transceivers

[3] Xilinx, “Burst-Mode Clock Data Recovery with GTH and GTY Transceivers XAPP 1252 (v1.3),” Apr. 12, 2019. https://docs.amd.com/v/u/en-US/xapp1252-burst-clk-data-recovery