Contribution ID: **9** Type: **not specified**

Reset Usages in FPGAs

Wednesday 21 May 2025 17:20 (30 minutes)

I will talk about reset usages in FPGAs and some solutions to practical problems in asynchronous, synchronous and no reset scenarios on different FPGA families. I will point out that the optimum reset usage depends on not only coding styles but also built-in reset features and behavioral differences (e.g. RAM-based vs FLASH-based FPGAs) of the FPGA family in use. Moreover, I will explain how to integrate reset related linting checks into CDCI cycles so that potentially hazardous design and or verification issues are diagnosed at the early stages of projects. I will exemplify some problems I solved in the past. Planning to also mention tools like Questa Lint, RDC, CDC and their Open Source alternatives.

Talk's Q&A

End of talk

Talk duration

25'+12'

Will you be able to present in person?

Yes

Author: KARAKURT, Koray

Presenter: KARAKURT, Koray

Session Classification: Solutions to everyday digital design problems

Track Classification: Solutions to everyday digital design problems