



OST

Eastern Switzerland
University of Applied Sciences

Exploring Stability in Time-to-Digital Converters

FDF2025

Gian-Luca Brazerol, Lukas Leuenberger, Paul Zbinden

19.05.2025

IMES

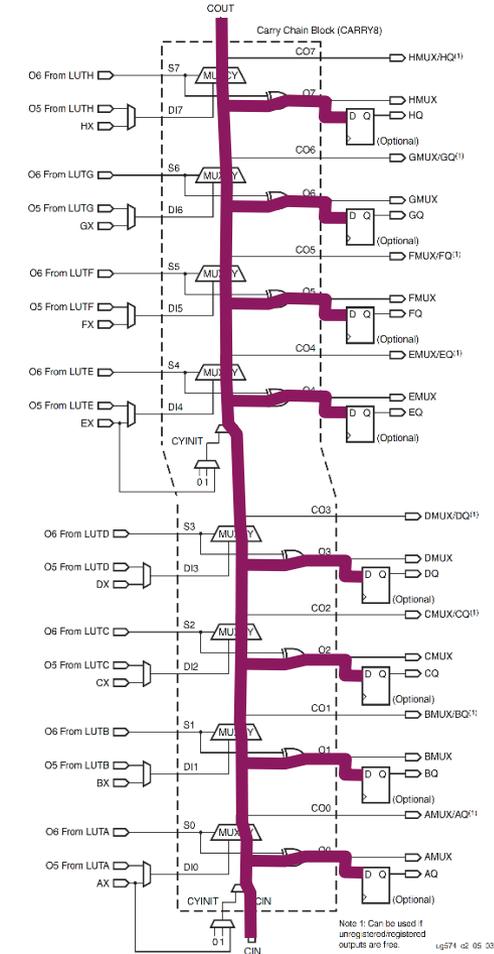
Agenda

- Introduction
- Considerations for Linearity
- Temperature Stability
- Performance Overview
- Conclusion

Introduction

Key Performance Indicators

- Measuring Range
- Resolution
 - LSB (mean delay)
- Dead Time
- Bubbles
 - 00**100**1111 → 000011111
 - 11**0101**000 → 111100000
- Nonlinearities
 - DNL
 - INL
- Precision
 - $\sigma^2_{TDC} \propto \sigma^2_{clk} + \sigma^2_{INL}$ [5]

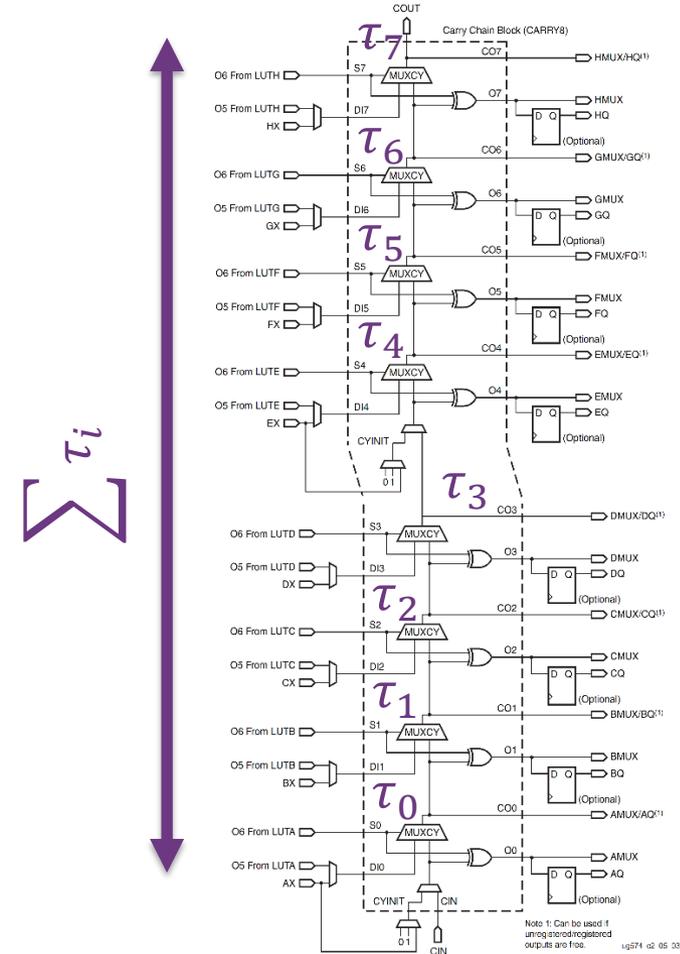


[5] [128-Channel High-Linearity Resolution-Adjustable Time-to-Digital Converters for LiDAR Applications: Software Predictions and Hardware Implementations](#)

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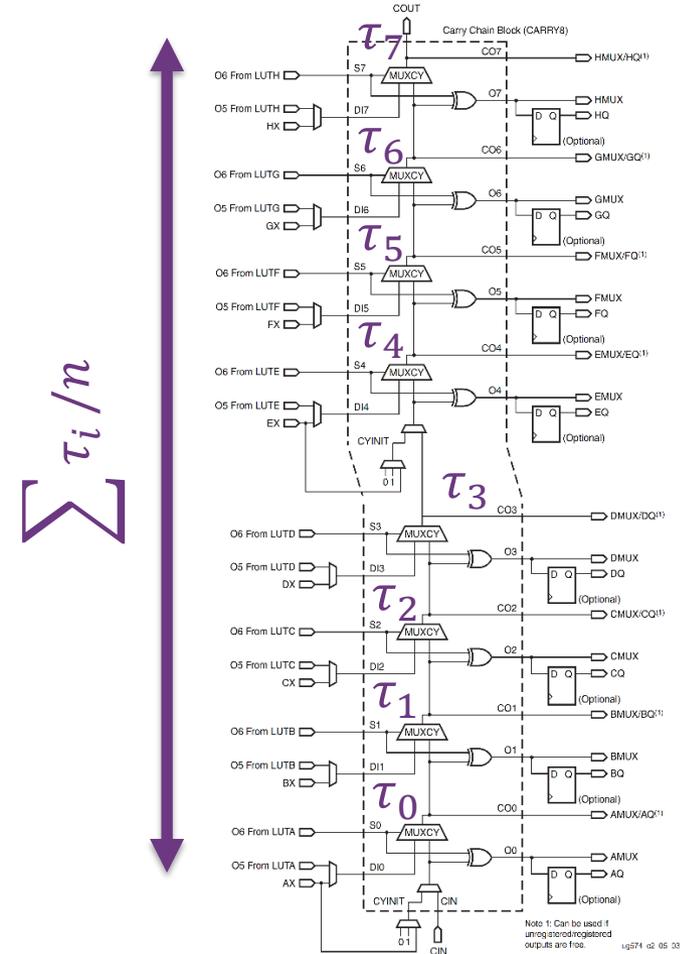


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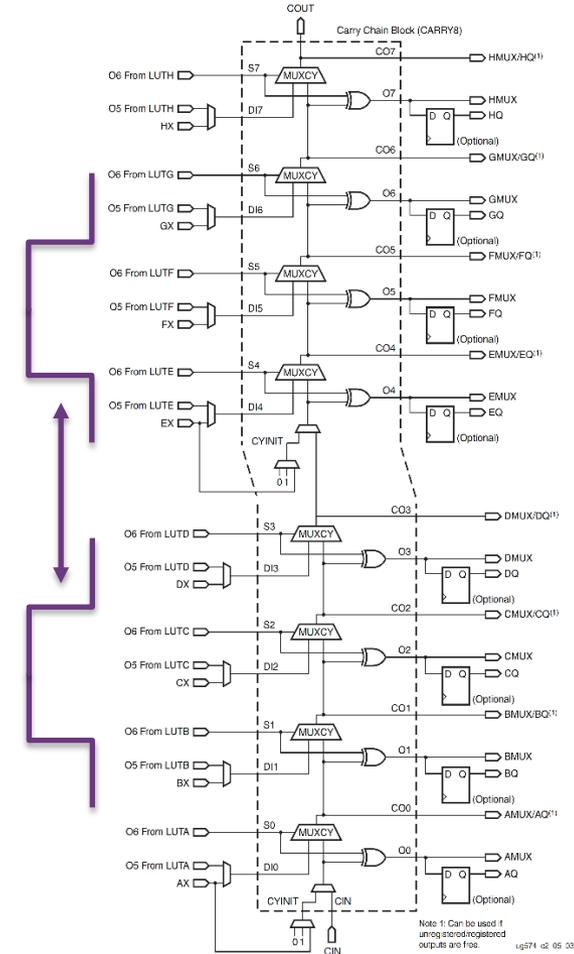


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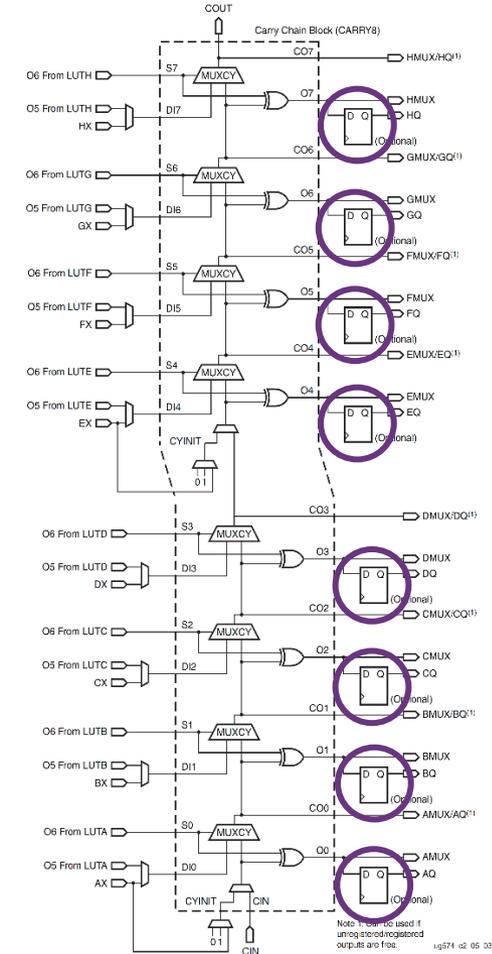


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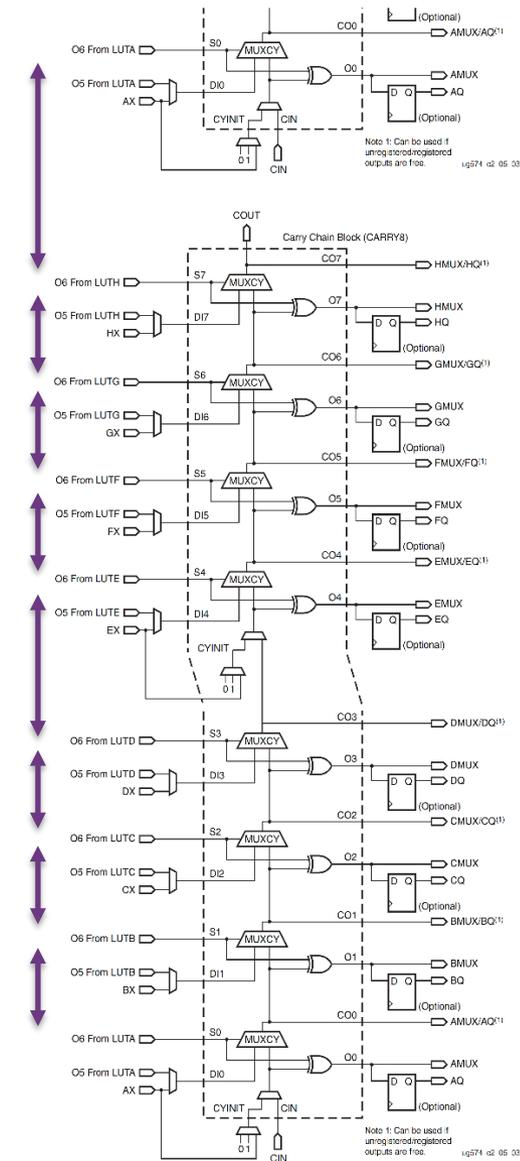


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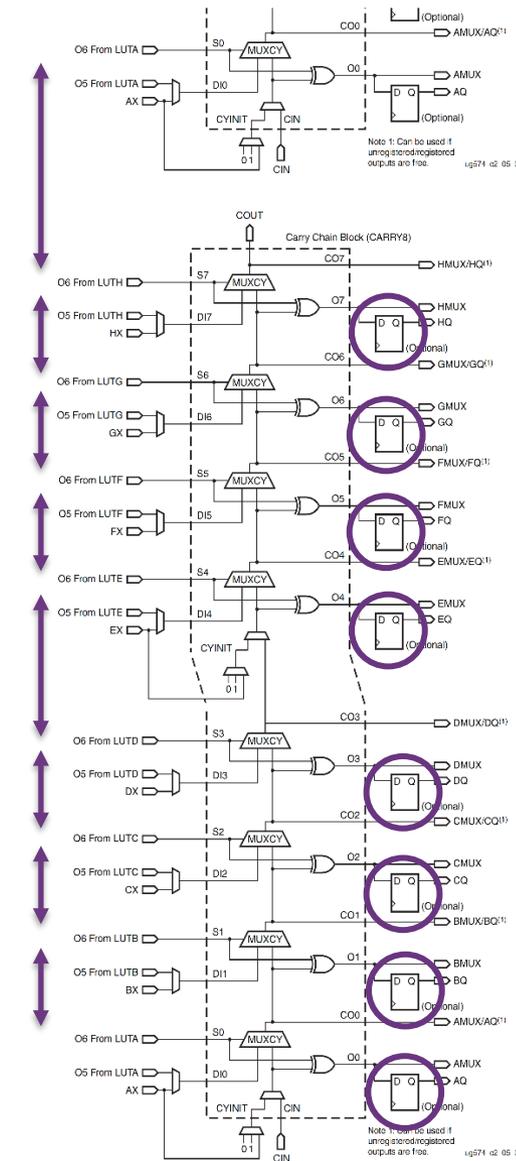


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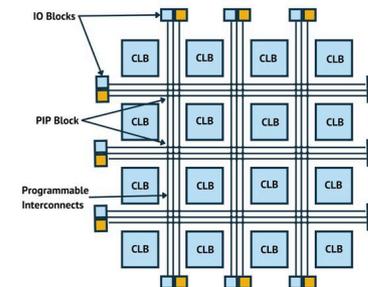
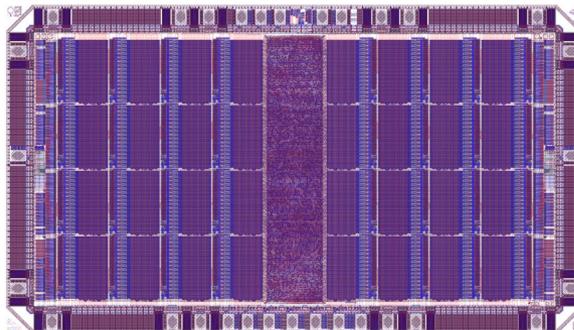
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TDC: ASIC vs. FPGA

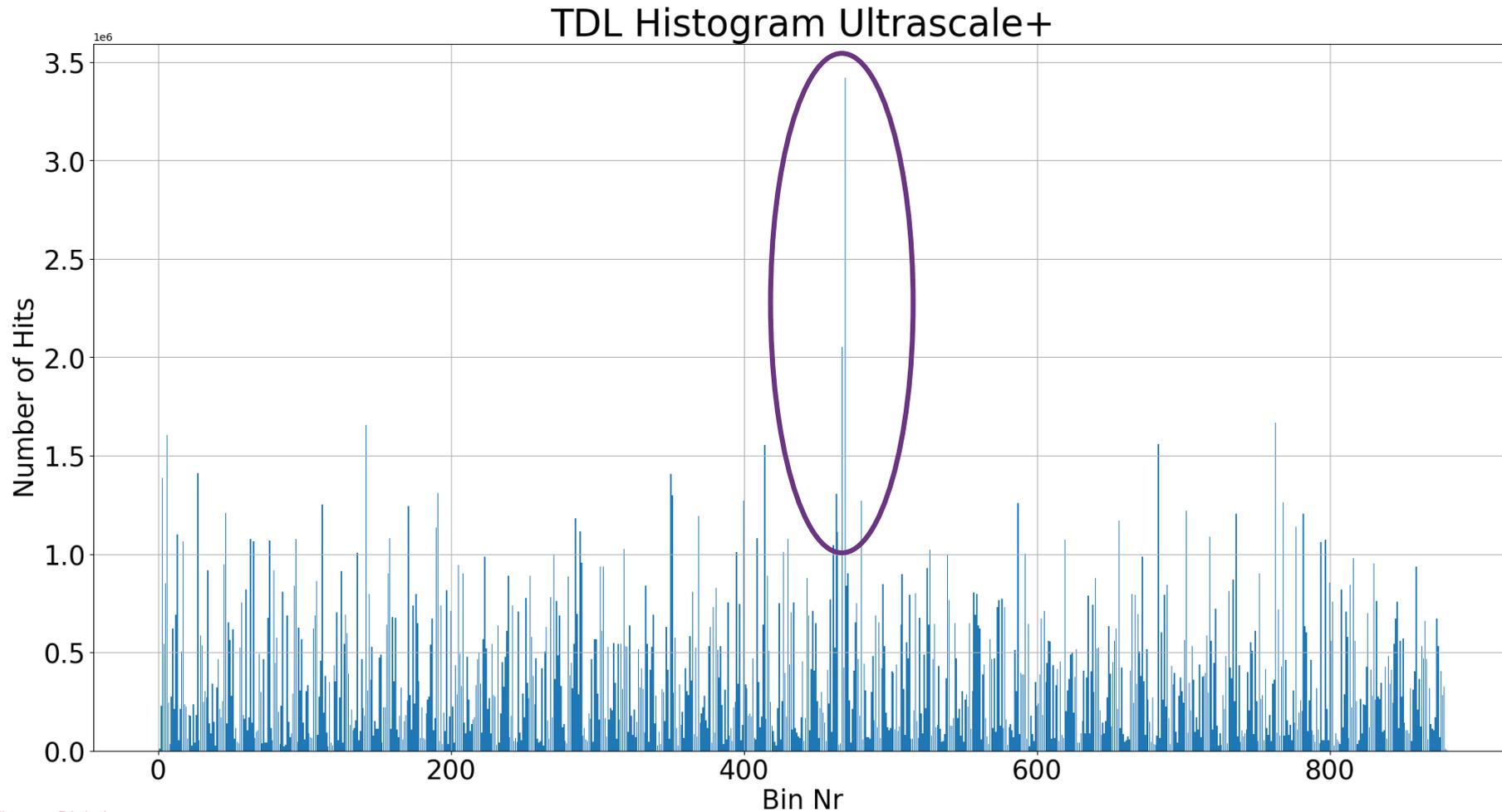
ASIC	FPGA
✓ Linearity	✗ Linearity
✗ Fixed Design	✓ Scalability & Flexibility
✗ High-Cost	✓ Cost-Effective
✗ Long Development Time	✓ Fast Prototyping



[6] [What is an FPGA and how does it work](#)

Considerations for Linearity

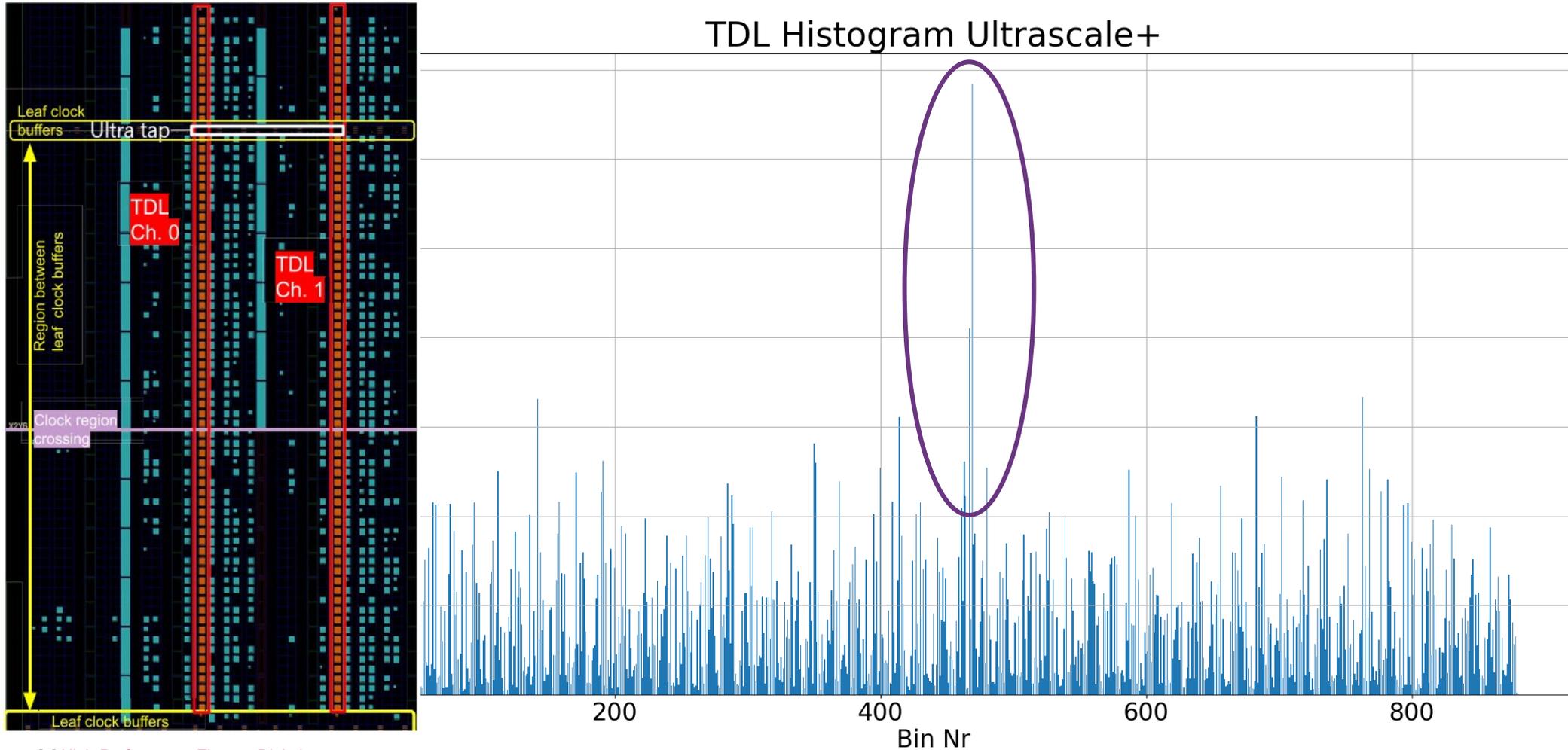
Nonlinearity Effects



[7] [High-Performance Time-to-Digital Conversion on a 16-nm Ultrascale+ FPGA](#)

Considerations for Linearity

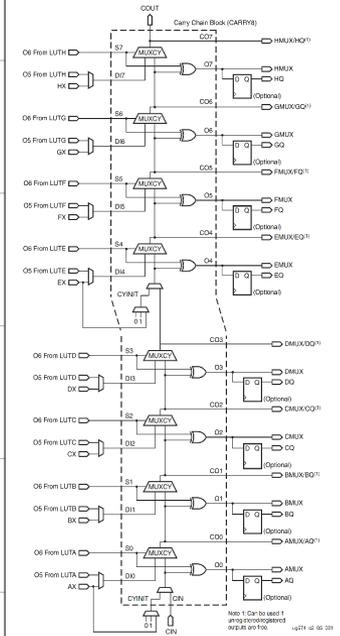
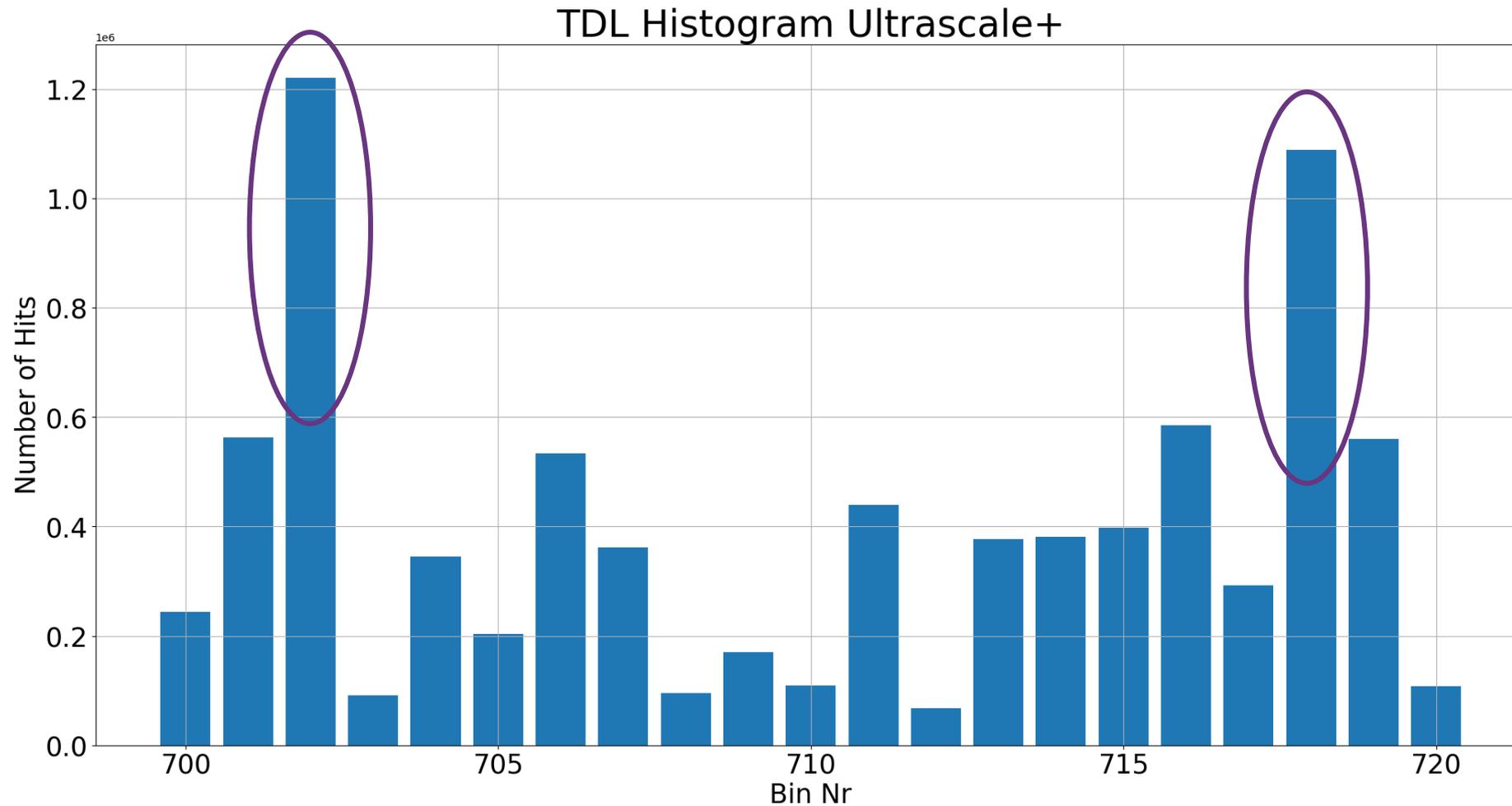
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[7] [High-Performance Time-to-Digital Conversion on a 16-nm Ultrascale+ FPGA](#)

Considerations for Linearity

Nonlinearity Effects

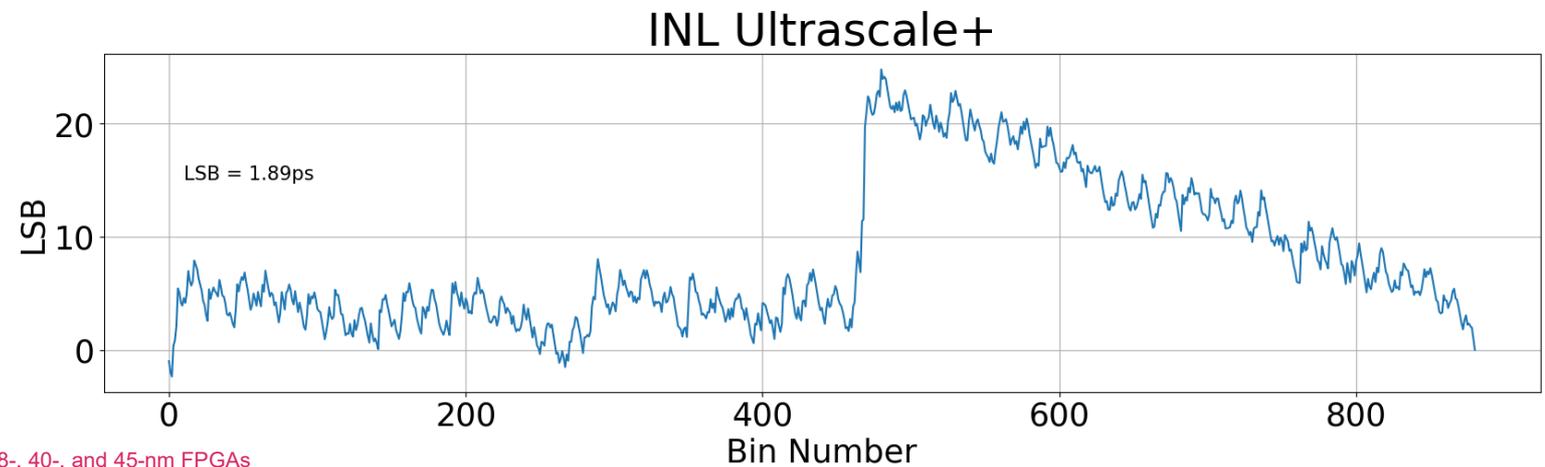
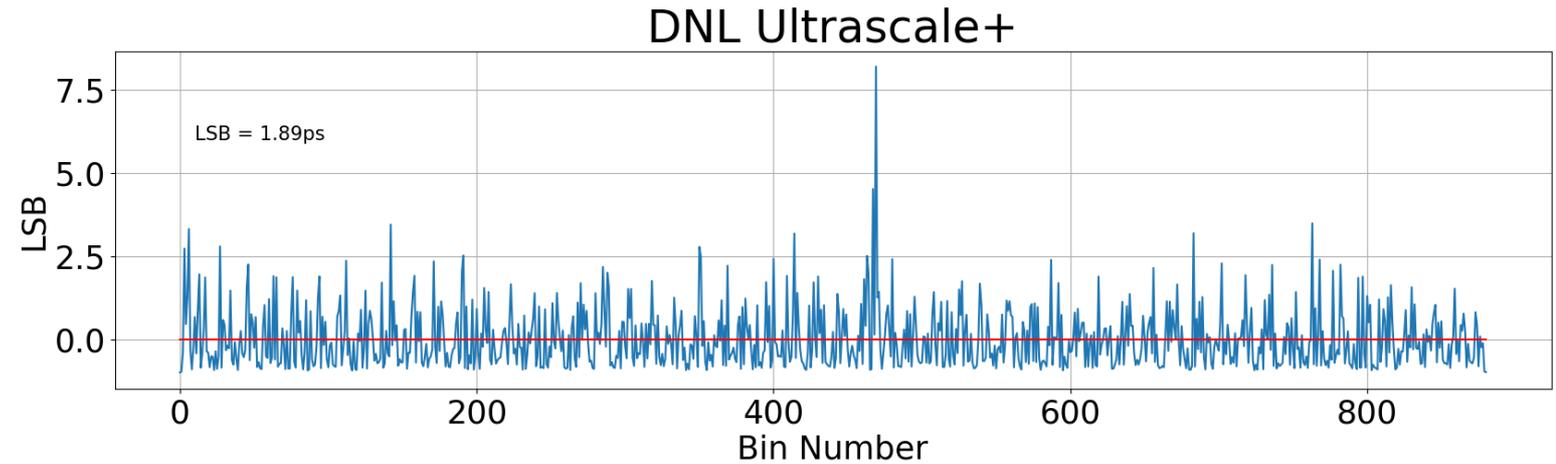


Considerations for Linearity

DNL and INL

- $$DNL[k] = \frac{N_k \cdot L_{TDL}}{N} - 1$$

- $$INL[k] = \sum_{i=0}^k DNL[i]$$

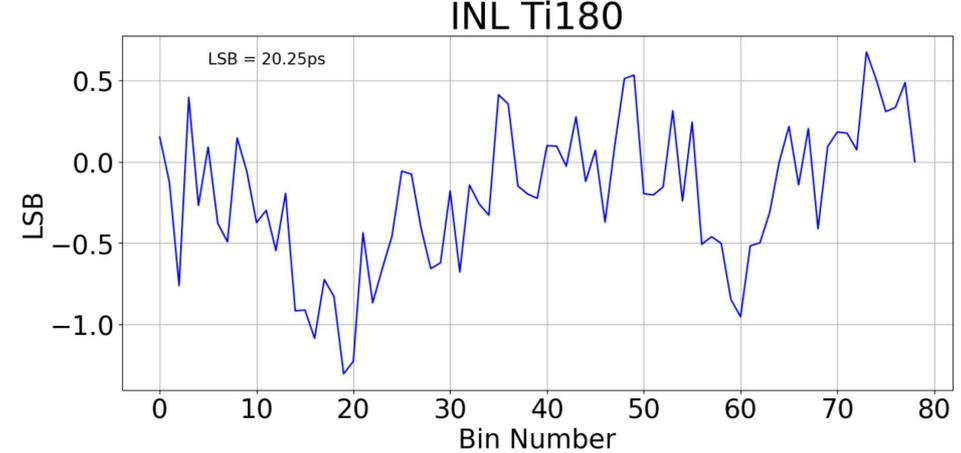
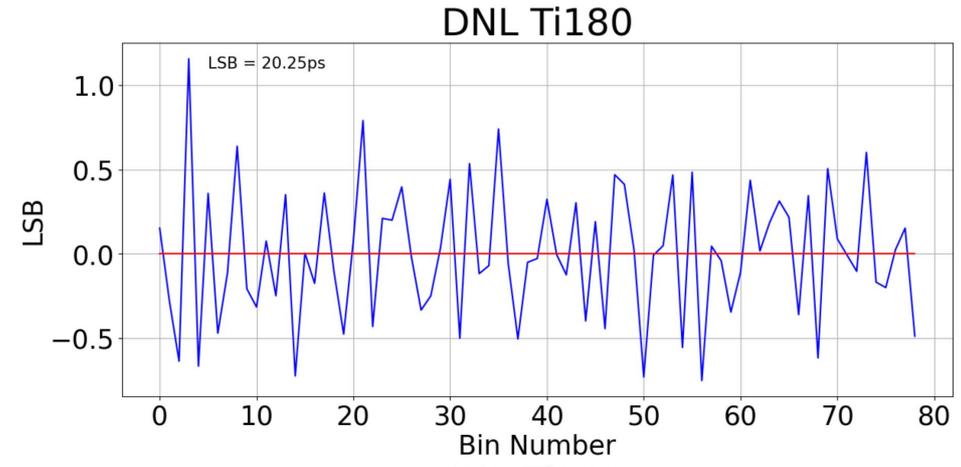
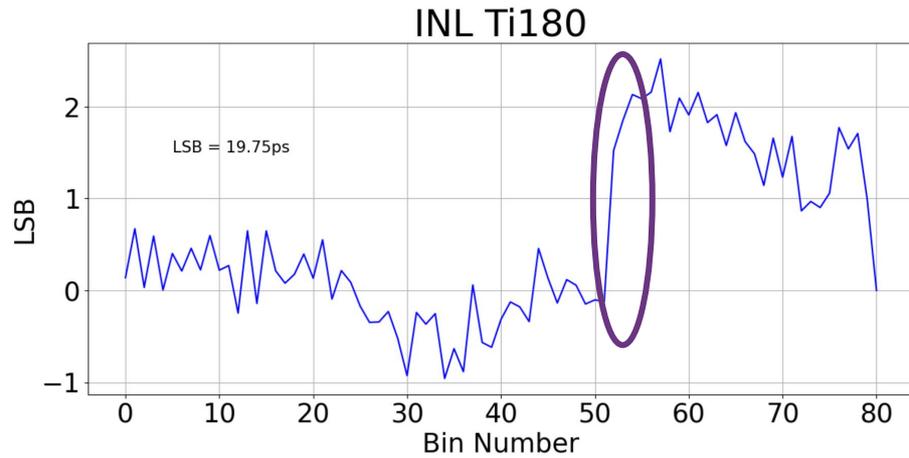
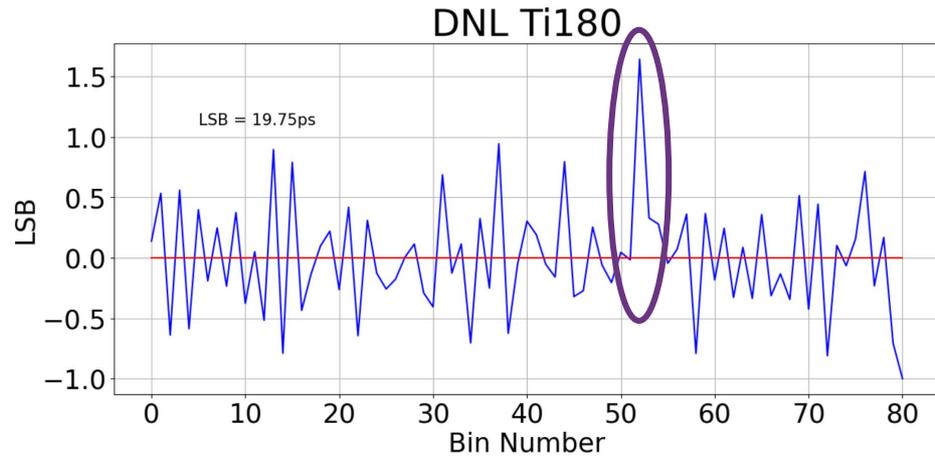


[8] [Time-to-Digital Converter Using a Tuned-Delay Line Evaluated in 28-, 40-, and 45-nm FPGAs](#)

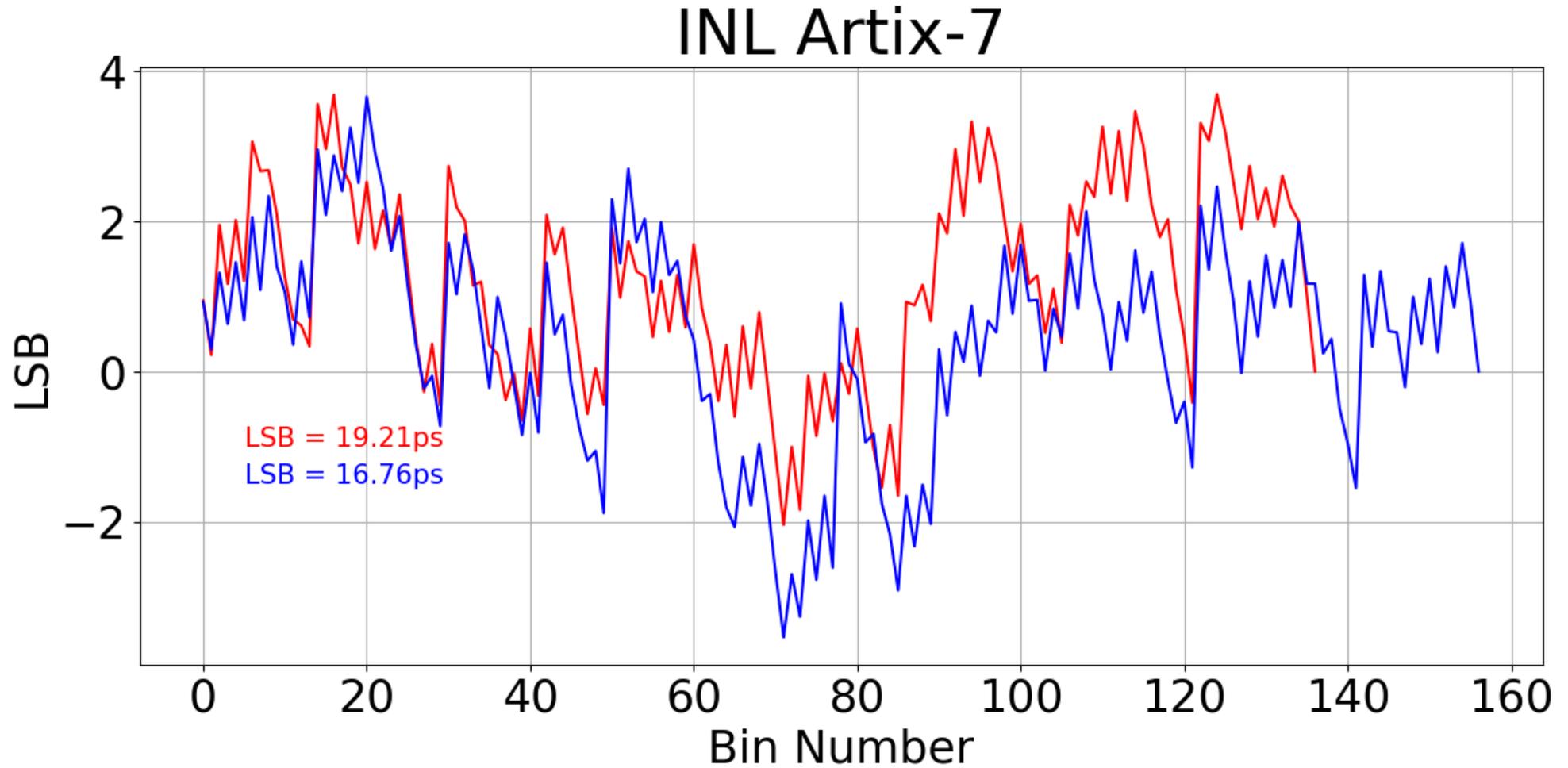
[9] [Calibration Methods for Time-to-Digital Converters](#)

Considerations for Linearity

TDL Placement



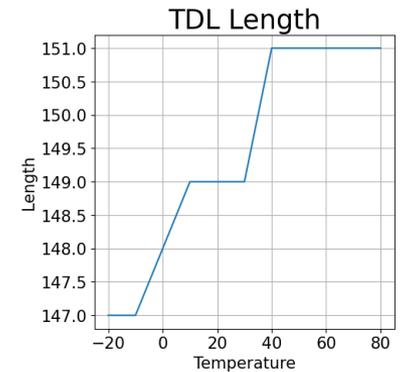
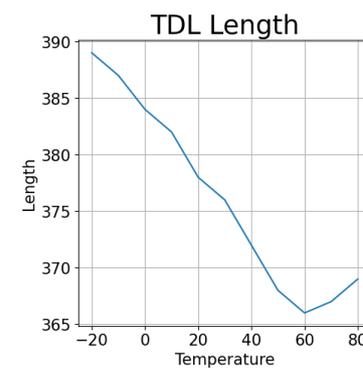
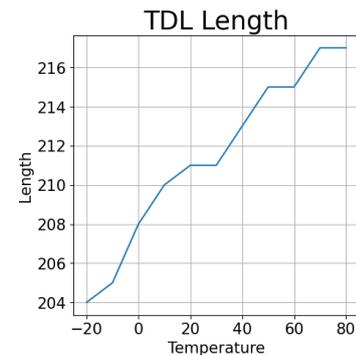
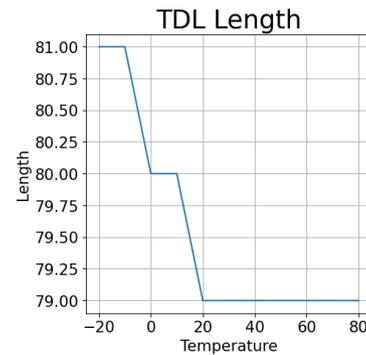
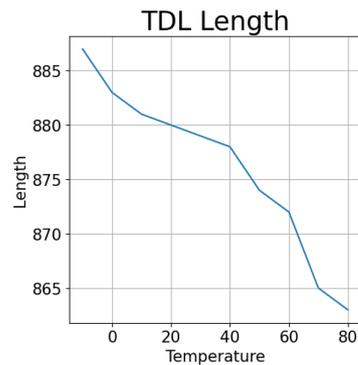
Die vs. Die



Temperature Stability

TDL Length vs. Temperature

- Determination of the number of delay elements required to map one period of a 600MHz (Ultrascale+ & Arria10), 625MHz (Ti180), 400MHz (Cyclone V), 380MHz (Zynq7000) clock



	Ultrascale+ [16nm]	Ti180 [16nm]	Arria10 GX [20nm]	Cyclone V [28nm]	Artix-7 [28nm]
TDL Length	863 - 887	79 - 81	204 - 217	366 - 389	147 - 151
LSB	1.88ps – 1.93ps	19.75ps – 20.25ps	7.68ps – 8.17ps	6.77ps – 7.19ps	17.43ps – 17.90ps
Relative Variation	2.78%	2.53%	6.37%	6.26%	2.72%

Performance Overview

Overview

- Measurements from -20°C to 80°C

	Ultrascale+ [16nm]		Ti180 [16nm]		Arria10 GX [20nm]		Cyclone V [28nm]		Artix-7 [28nm]	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
TDL Length	863	887	79	81	204	217	366	389	147	151
LSB	1.88ps	1.93ps	19.75ps	20.25ps	7.68ps	8.17ps	6.77ps	7.19ps	17.43ps	17.90ps
DNL min	-0.99	-0.99	-0.79	-0.73	-1	-0.99	-1	-1	-0.99	-0.97
DNL max	7.24	9.92	0.80	1.48	7.82	9.67	4.4	5.95	3.03	3.26
INL min	-3.23	-2.26	-1.63	-1.11	-4.07	-2.03	-30.78	-21.97	-4.04	-1.38
INL max	23.58	28.99	0.55	1.11	10.64	13.59	17.43	22.91	1.87	4.64

Conclusion

Take-Aways

- Deep Understanding of Low-Level Architecture Required
- Precise TDL Placement is Critical
- Each TDL Requires Individual Calibration

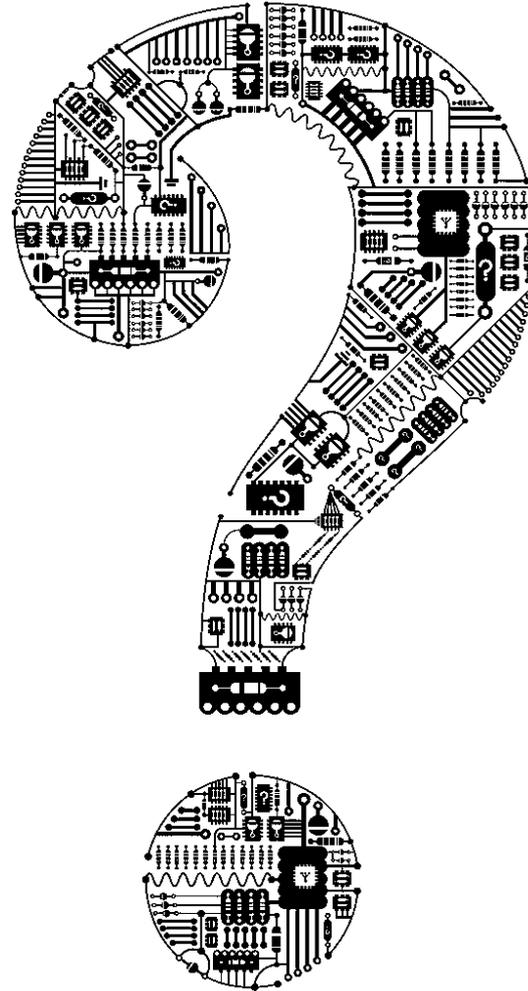
Efinix Ti180 [16nm]	Artix-7 [28nm]	Ultrascale+ [16nm]	Arria10 GX [20nm]	Cyclone V [28nm]
~ Big LSB	~ Big LSB	✓ Low LSB	✓ Low LSB	✓ Low LSB
✓ Good Linearity	✓ Good Linearity	✗ Bad Linearity	~ Moderate Linearity	✗ Bad Linearity
✓ Good Temperature Stability	✓ Good Temperature Stability	✓ Good Temperature Stability	~ Moderate Temperature Stability	~ Moderate Temperature Stability
✓ Almost no Bubbles	✓ Small Bubbles	~ Moderate Bubbles	~ Moderate Bubbles	✗ Big Bubbles

Conclusion

Questions

IMES

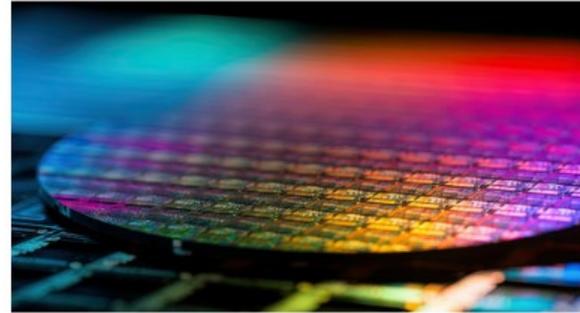
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Schweiz



Introduction

IMES: Overview Expertise

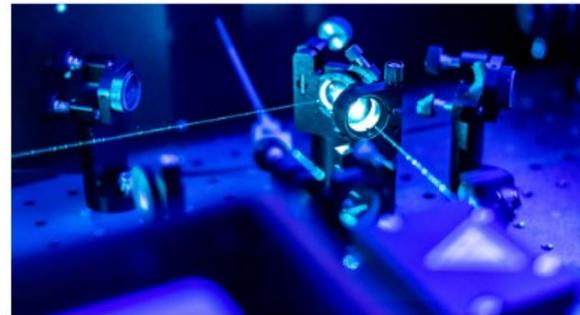
- **Microelectronics:**
 - ASIC Design Analog
 - ASIC Design Digital
 - ASIC Design Mixed – Signal
 - Design for Test
- **Embedded Systems:**
 - Ultra Low Power Systems
 - Edge Computing
 - Robotics and Smart Drives
 - Embedded Artificial Intelligence
 - Real-Time Data Processing
- **Sensors**
 - Photonics
 - Medical
 - Inductive Sensors
 - Capacitive Sensors
 - Ultrasonic Sensors
 - Further Sensor Principles
- **Advanced System Technologies**
 - FPGA Design
 - Hardware acceleration for cryptographic systems
 - Side Channel analysis in cryptographic systems
 - Time to Digital Converters
 - Hardware acceleration for stream-based data processing
 - Hardware acceleration for machine learning/deep learning



Microelectronics

We develop application specific CMOS circuits (ASIC) with analogue and digital functions. Our focus is on sensor front-end circuits and low power systems.

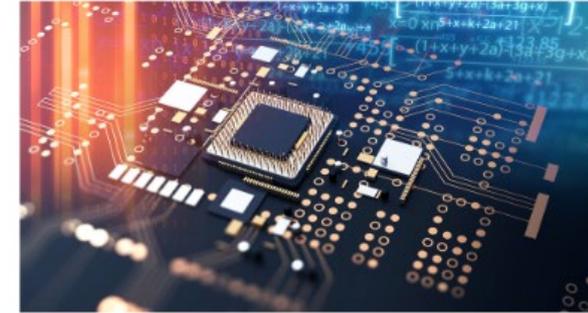
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Sensors

We are pleased to offer our support in the development of sensor systems, from feasibility studies and prototype development through to qualification and product development.

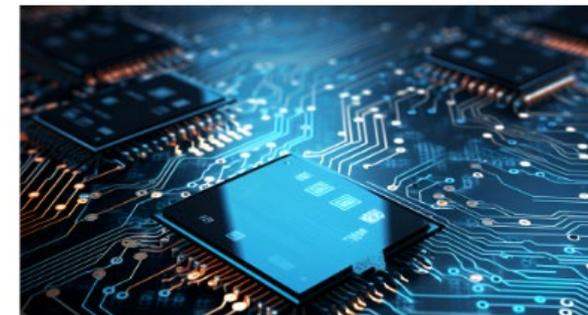
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Embedded Systems

From ultra-low power to real-time data processing: We implement intelligent microcontroller and FPGA solutions from resource-constrained devices to high-performance multiprocessor systems.

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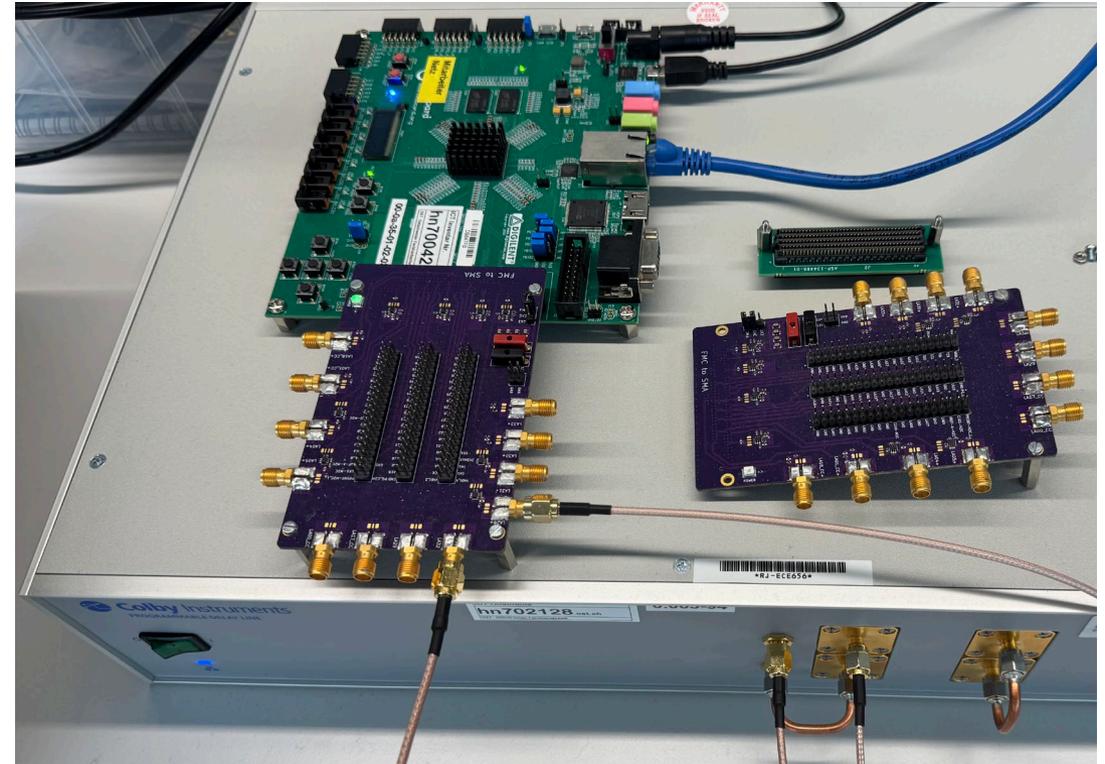
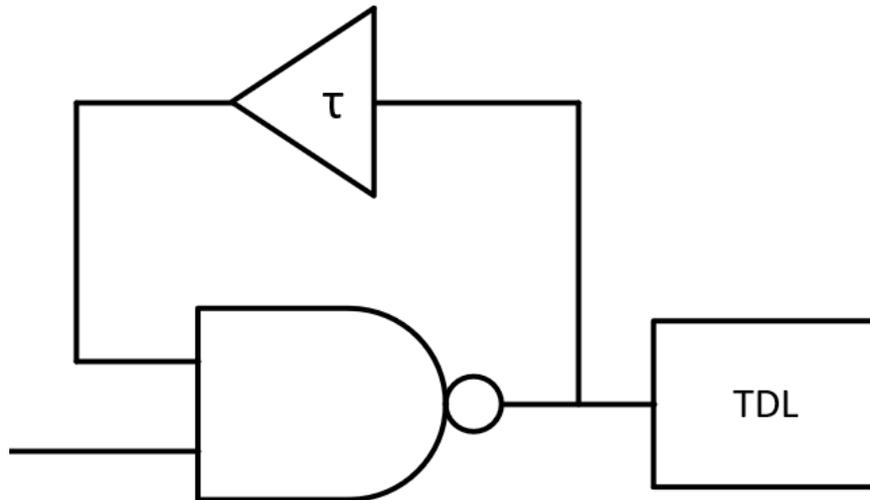
Advanced System Technologies

Do you have innovative ideas and need help implementing them with a new type of computing technology? Are you interested in low latency or high throughput?

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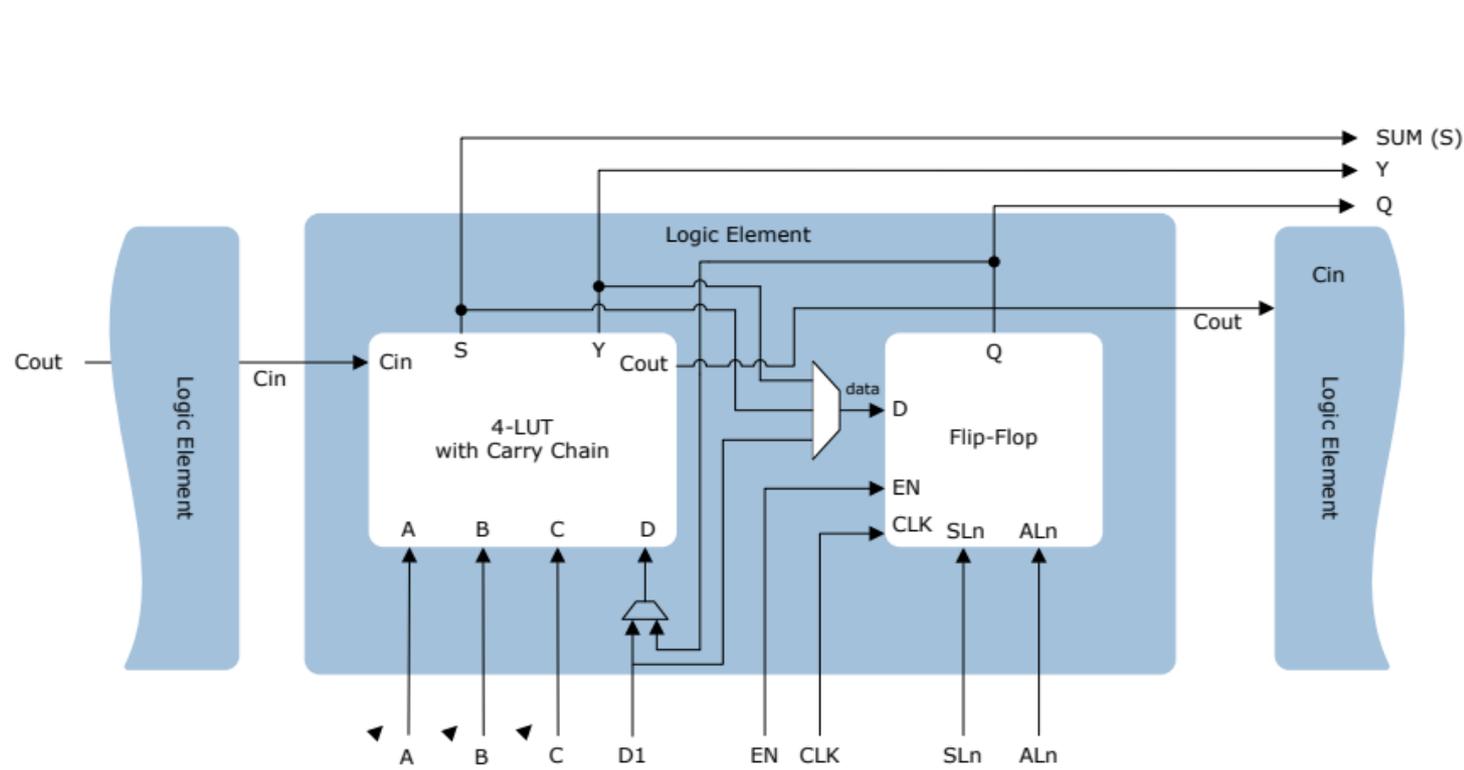
Considerations for Linearity

Code Density Test

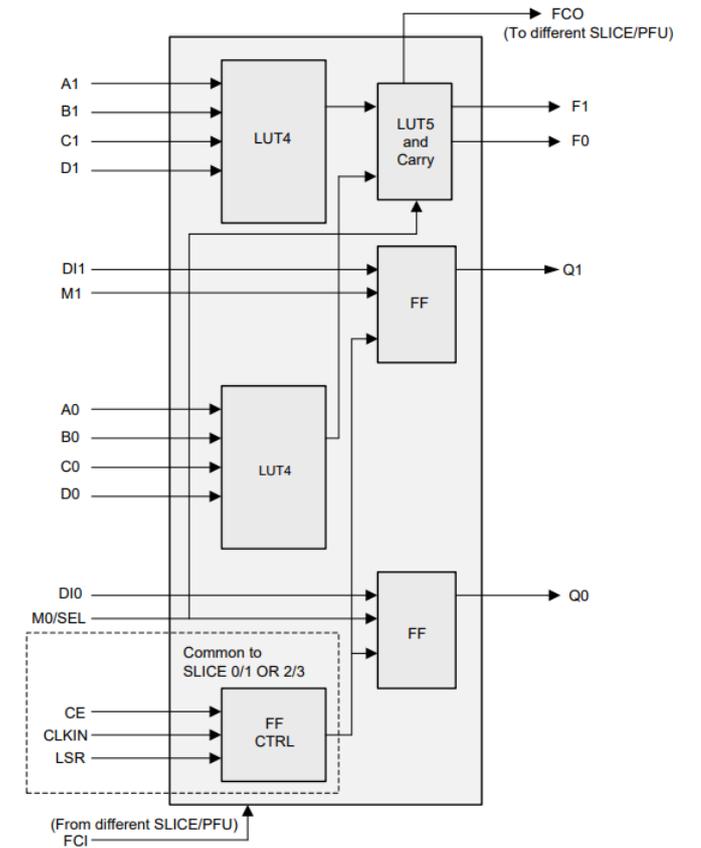


FPGA Families

Different Families



Microchip PolarFire



Lattice Certus-NX

[12] [PolarFire SoC Fabric UG VB](#)
[13] [Certus-NX Family Data Sheet](#)