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Customized eFPGAs with FABulous

Thursday 22 May 2025 09:30 (30 minutes)

FABulous is an eFPGA (embedded FPGA) framework comprising a full ecosystem for specifying, simulating, emulating and implementing FPGA ASIC macros as well as for providing the corresponding FPGA CAD suite for implementing user designs (the bitstreams) for the custom-defined eFPGAs.

[<https://fabulous.readthedocs.io/en/>]

This ecosystem integrates a range of open-source tools, including Yosys, nextpnr, Verilator and can use OpenLane and industry tools for the ASIC backend. FABulous FPGAs have been manufactured in Skywater 130, GF 180, TSMC 180, 130, 28nm nodes and the framework has users such as SLAC at Stanford University and New York University.

This talk will introduce the framework and demonstrate how a fabric with LUTs, DSP blocks, and BRAMs can be specified in just a minute. Moreover, it will also be shown how complex custom primitives can be added into FABulous fabrics and then instantiated in the FPGA bitstream generation flow. We will also reveal our FABulous chip gallery.

Talk's Q&A

During the talk

Talk duration

25'+12'

Will you be able to present in person?

Yes

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