



# Disruptive Efinix Quantum Architecture.

Harald Werner, Managing Director EMEA

V: 1.0.0

# An International Footprint

- HQ in Cupertino
- Founded 2012
- R&D Centers In Silicon Valley, Toronto, Penang, and Hong Kong
- ~200 Employees

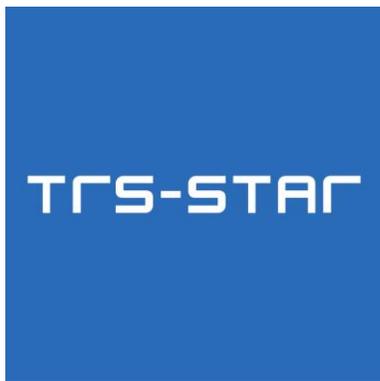


# Distribution Network Europe :

**DigiKey**



**RUTRONIK**  
ELECTRONICS WORLDWIDE



**FUTURE**  
**ELECTRONICS**



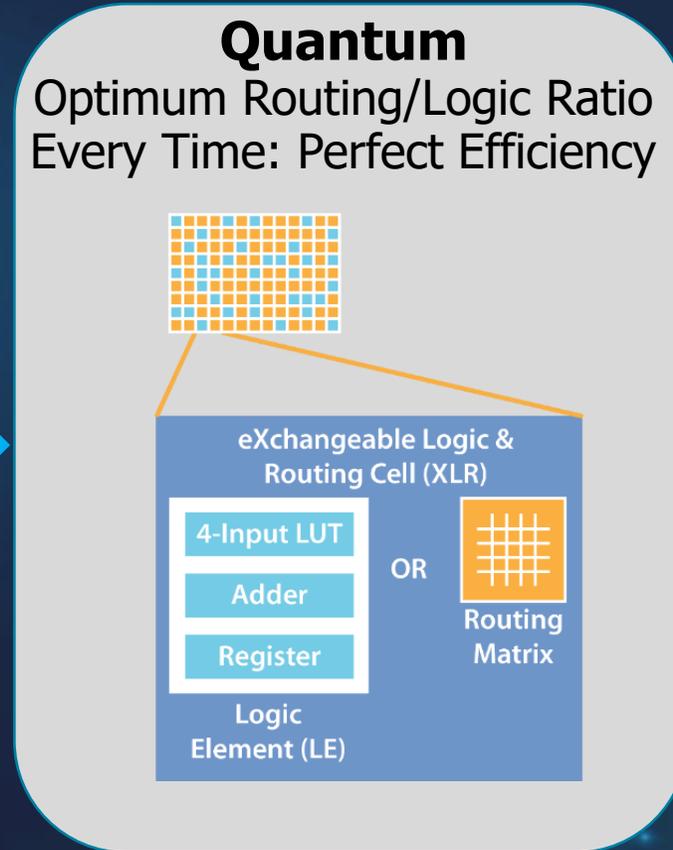
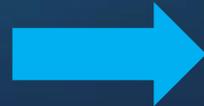
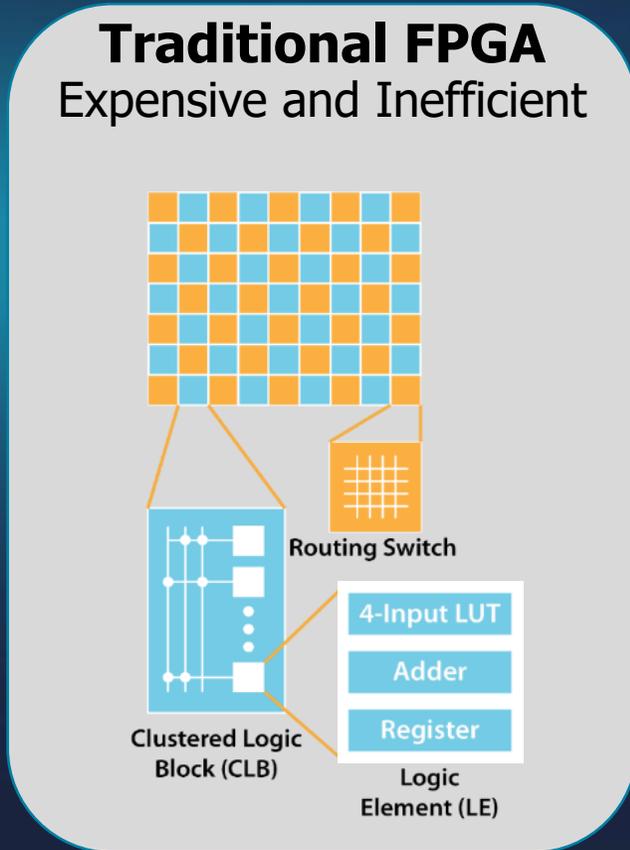
# Congested designs

- Congested designs are designs, which needs a lot of routing resources to connect the blocks together.
- Once a channel used all of the doorways, you can no longer access the remaining logic.



# Patent Protected FPGA Technology

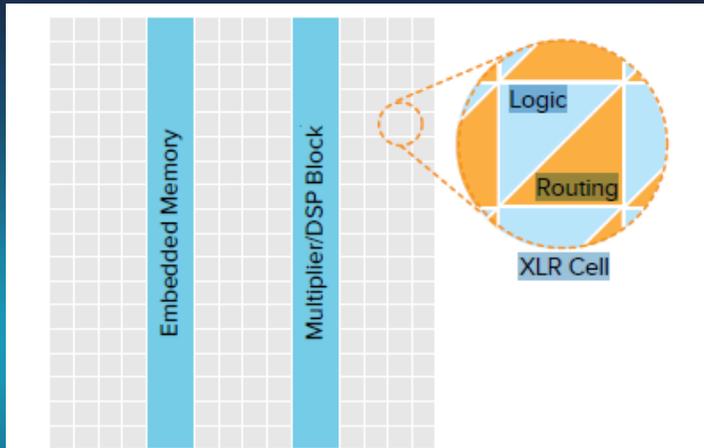
Erasing 40 Years of Inefficiency



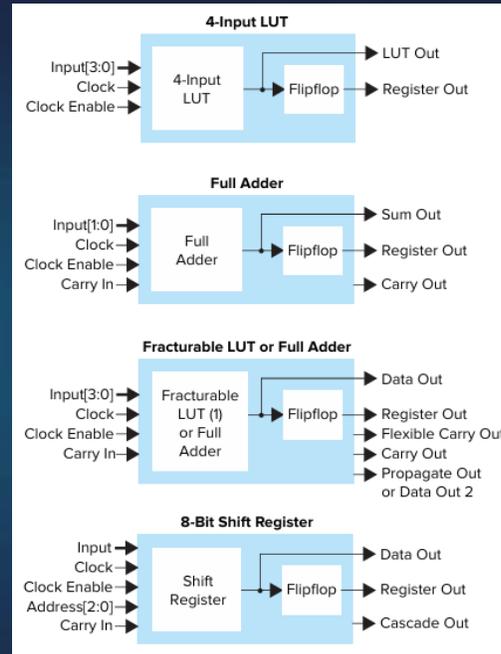
**EFINIX**®

- **High Performance**
- **Small Size**
- **Lower Power**
- **Cost Optimized**
- **Silicon process agnostic**

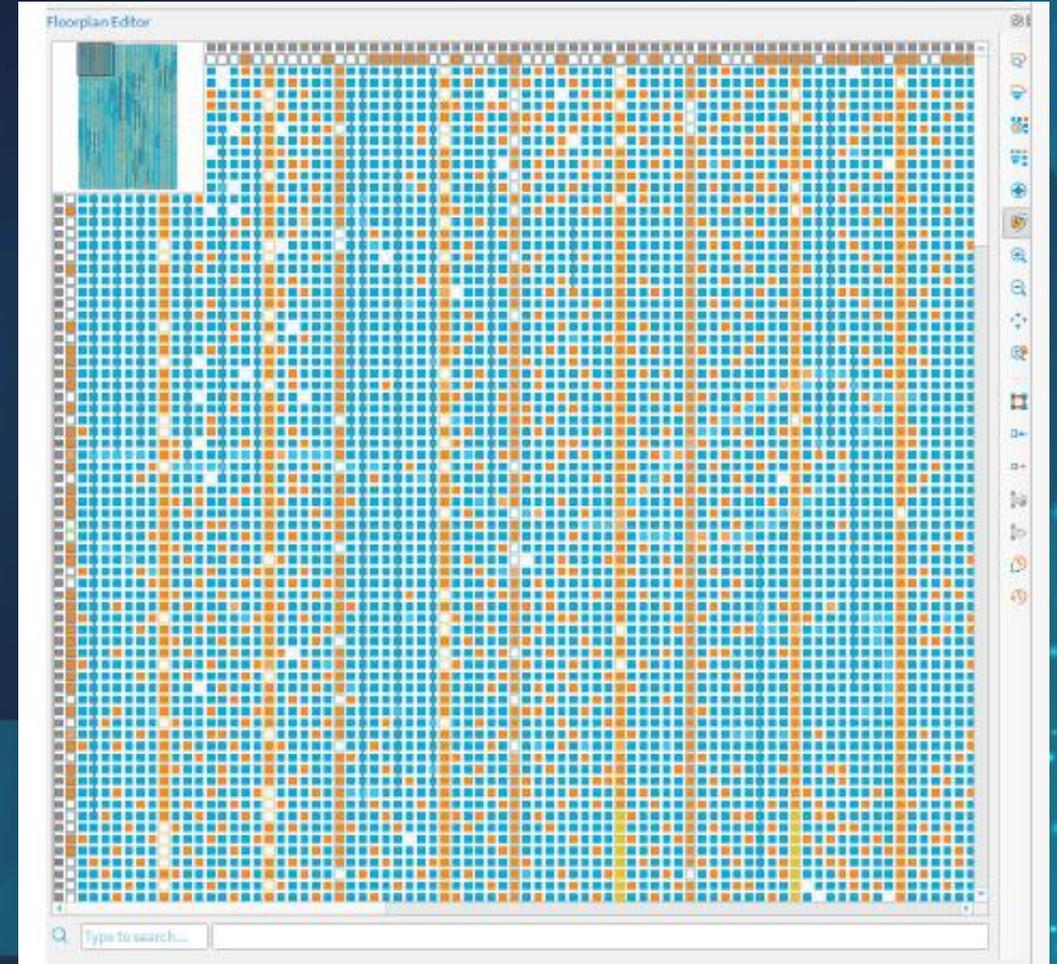
# eXchangeable Logic and Routing (XLR) Cells



Ability to use logic and routing at the same time



Logic Cell



8 times a 32 Bit RISC-V implemented into Ti60:

XLR: 56792/60800

# Product Portfolio



- Mid-Range 4K-120K LE
- Cost Optimized
- 1.5Gb MIPI D-PHY +CSI
- DDR3 Controller 1066Mbps
- Mask Programmable



- Mainstream FPGA 50K-325K LE
- Performance/Cost Optimized
- 2.0Gb MIPI D-PHY +CSI
- LPDDR4 Controller 2.4Gbps
- Enhanced DSP
- SERDES up to 12.5Gbps
- Quad RISC-V @800MHz



- Mid-High Range 35K-1M LE
- Performance Optimized
- 2.5Gb MIPI D-PHY +CSI
- LPDDR4/4X Controller 3.3Gbps
- Enhanced DSP
- SERDES up to 16Gbps
- Quad RISC-V @1GHz



- RTL to Bitstream Generation
- Simple and Intuitive GUI
- Floorplan Editor
- Timing Browser and STA
- Hardware Debugger

# Trion<sup>®</sup> FPGAs (Gen 1)

- Focus on **Consumer, Industrial Markets, Communications Markets** with varied applications
  - Traditional FPGA markets
  - Emerging edge AI computing markets
  - Applications: mobile, IoT, LED, automation, robotics, video, audio, sensing integration, display, computer vision, etc.
- 4K to 120K LEs on 40LL SMIC silicon process
- Traditional SRAM-based FPGA
  - Masked option for T20/T13/T8/T4 – boots internally vs. using a configuration device
- Optimized for low power
- Hard core blocks for DDR memory controllers (1066Mbps) and D-PHY v1.1 and CSI-2 v1.3
  - Up to 3 independent RX/TX interfaces, 4 lanes x 1.5 Gbps



Artificial intelligence (AI) and machine learning algorithms are everywhere, enabling new advances in areas like image and speech recognition and autonomous driving. But applications on the leading edge need a platform that can change as rapidly as they do.

Efinix<sup>®</sup> Trion<sup>™</sup> FPGAs are flexible, programmable platforms that can accelerate AI applications that rely on changing algorithms. Bring your Trion-accelerated product to market quickly today, and change it tomorrow to meet the next challenge.

See how Trion FPGAs are driving edge AI computing!

[www.efinixinc.com/drivingai](http://www.efinixinc.com/drivingai)



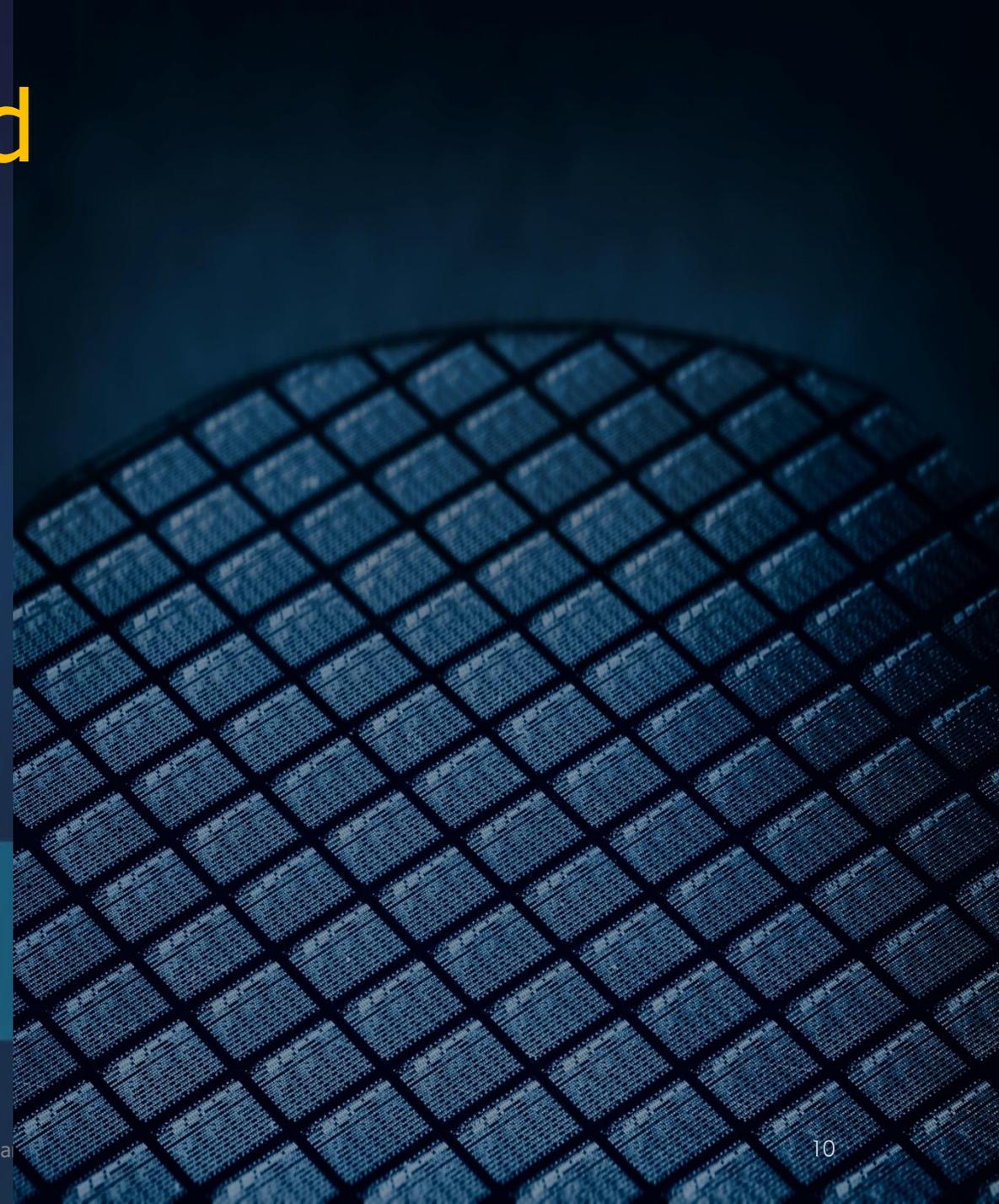
# Trion Family Table



Feature	T4	T8	T13	T20	T35	T55	T85	T120		
Logic Elements (LEs)	3,888	7,384	12,828	19,728	31,680	54,195	84,096	112,128		
Mask Programmable Memory	√	√	√	√	—	—	—	—		
Embedded RAM bits (kb)	77	77	727	1,044	1,475	2,765	4,055	5,407		
18 x 18 Multipliers	4	8	24	36	120	150	240	320		
	<b>Packages (GPIO/PLLs/LVDS PairsTX,RX/MIPI-CSI2 TX,RX/DDR)</b>									
49-ball FBGA (0.4 mm, 3x3 mm)	33	1 33	1 -							
80-ball WLCSP (0.4, 4.5x3.6mm)				33	5 - 1, 1 -					
81-ball FBGA (0.5, 5x5 mm)	55	1 55	1 -							
100-pin LQFP (0.5, 14x14 mm) (SIP)				65	4 4,4 - -	65	4 4,4 - -			
144-pin LQFP (0.5, 20x20 mm)		97	5 6, 6		97	5 6, 6 - -				
169-ball FBGA (0.65, 9x9 mm)				73	5 8,12 2, 2 -	73	5 8,12 2,2 -			
256-ball FBGA (0.8, 13x13 mm)*/**				195	5 13,13 - -	195	5 13,13 - -	191	7 10,18 - -	
324-ball FBGA (0.65, 12x12 mm)					130	7 20,26 2,2 x8,x16	130	7 20,26 2,2 x8,x16	130	7 20,26 2,2 x8,x16
400-ball FBGA (0.8 16x16 mm)					230	7 20,26 - x8,x16	230	7 20,26 - x8,x16		
484-ball FBGA (0.8, 18x18 mm)							256	8 40,40 - x16,x32	256	8 40,40 - x16,x32
576-ball FBGA (0.65, 16x16 mm)							278	8 52,52 3,3 x16,x32	278	8 52,52 3,3 x16,x32
SIP: 16Mb SPI flash integrated. ** subject to change	LVDS Pairs (TX, RX)			PLLs						
*: T20F256 not pincompatible with T35F256	MIPI Pairs (TX, RX)			DDR						

# Titanium Under the Hood

- TSMC 16nm Process
  - High Performance for the Most Demanding Applications
  - High Density and Low Power Consumption
- 2<sup>nd</sup> Generation Quantum Fabric
  - Optimized for Compute & Artificial Intelligence
- High Speed Interfaces
  - Designed for Video and Quantum Acceleration



# Titanium Family Table



			Ti35	Ti60	Ti85	Ti90	Ti120	Ti135	Ti165	Ti180	Ti240	Ti375	Ti550	Ti750	Ti1000
LE (k)			36	62	83	92	123	134	162	176	237	370	550	750	1000
10K RAM (Mb)			1,53	2,62	6,18	7,34	9,80	9,95	12,10	13,11	19,37	27,53	39,65	55,80	74,40
DSP			93	160	300	359	478	486	590	640	946	1344	1936	2736	3648
PLLs			4	4	12	10	10	12	12	10	12	12	12	12	12
HVIO			34	34	166	80	80	166	181	80	181	181	200	200	200
HSIO			146	146	140	232	232	140	235	232	235	235	320	320	320
MIPI DPHY 1.5G, support CSI-			Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
MIPI DPHY x4 2.5Gbps Hard IP			-	-	X2	X4	X4	X2	X3	X4	X3	X3	X3	X3	X3
LPDDR4/X (> 3Gbps)			-	-	X32	X32	X32	X32	2 X32	X32	2 X32	2 X32	2x72	2x72	2x72
RISC-V hardwired					x			x	x		x	x	x	x	x
16 Gbps Serdes			-	-	X8	-	-	X8	X16	-	X16	X16	X16	X16	X16
25.8 Gbps Serdes			-	-	-	-	-	-	-	-	-	-	X8	X8	X8
PCIe Gen4 (16G) hard controller			-	-	1x PCIe Gen4x4			1x PCIe Gen4x4	2x PCIe Gen4x4		2x PCIe Gen4x4	2x PCIe Gen4x4	2x PCIe Gen4x8	2x PCIe Gen4x8	2x PCIe Gen4x8
<b>Packages (HSIO/HVIO/LPDDR4/MIPI /SERDES)</b>															
W64	0.4mm	3.5x3.4mm	-	34/0											
F100 (SIP)	0.5mm	5.5x5.5mm	61/0	61/0											
F100	0.5mm	5.5x5.5mm	61/0	61/0											
F225	0.65mm	10x10mm	140/23	140/23											
F256	0.8mm	13x13mm	142/27	142/27											
J361	0.65mm	13x13mm	-	-		110/20/16/2/0	110/20/16/2/0			110/20/16/2/0					
G400	0.8mm	16x16mm				200/74/0/0/0	200/74/0/0/0			200/74/0/0/0					
J484 (SIP)	0.65mm	15x15mm	-	-						190/54/0/2/0					
J484	0.8mm	18x18mm	-	-		116/27/32/4/0	116/27/32/4/0			116/27/32/4/0					
G529	0.8mm	19x19mm	-	-		210/48/32/0/0	210/48/32/0/0			210/48/32/0/0					
C529	0.8mm	19x19mm	-	-					176/50/32/0/0		176/50/32/0/0	176/50/32/0/0			
N441	0.5mm	11x11mm			86/18/16/1/8			86/18/16/1/8							
N576**	0.65mm	16x16mm			100/43/32/2/8			100/43/32/2/8							
N676**	0.8mm	22x22mm	-	-	139/84/32/2/8			139/84/32/2/8							
N676	0.65mm	18x18mm							140/84/32/2/8		130/63/32/2/12	130/63/32/2/12			
N484	0.8mm	18x18mm	-	-	85/21/32/1/8			85/21/32/1/8	85/20/32/1/8		85/20/32/1/8	85/20/32/1/8			
N900	0.8mm	25x25mm	-	-					167/50/32x2/2RX/16		167/50/32x2/2RX/16	167/50/32x2/2RX/16			
N1156	1.0mm	35x35mm	-	-					234/103/32x2/3/16		234/103/32x2/3/16	234/103/32x2/3/16	x	x	x



\*\* subject to change, just in the discussion  
 F100 (SIP) :16 MbFlash + 256Mbit HyperRAM  
 J484 (SIP) : 2Gb LPDDR4X

Available  
 Available soon  
 and Proprietary

# Cern collaboration

## DRD 7.6 a/b framework

- quantum FPGA on-detector modules using interposer technology (Ti60)

# Ti60F100 SIP

- FPGA with 60K LE, 2.6Mb Memory, 160 DSP Blocks
- BGA 100 Package (5.5x5.5mm, 0.5mm pitch)
- SPI flash 16Mb
- HyperRAM PSRAM up to 6.4Gbps (400Mbps x 16), (256Mb)
  - 500Mbps available soon !
- MIPI-CSI/DSI up to 1.5Gbps support.
  - 2x8 MIPI
  - 2x4 MIPI
- LVDS support up to 1.5Gbps
- VCC: 0.95/0.85V



256Mb HyperRam  
@500Mbps

16Mb Spi Flash

# Ti180 SIP Devices

- Ti180J484D1
- BGA484 package (15x15mm, 0.65mm pitch)
- LPDDR4x 2Gb x16 @2.5 Gbps in package
- 2x2.5G MIPI x4
- Preliminary datasheet : December 2024
- Samples and Dev, Kit: Q1'2025

# Advantage

- Advantages compared with Ti180 standalone FPGA



\*Stacked way in real

Package Size ↓ 30%

Simplify PCB layout

Low Power System

#High Speed IO ↑ 74

#High Voltage IO ↑ 27

## Ti180J484D1 Standalone FPGA

Features	Ti180D1	Ti180
LE	176256	176256
10K RAM (M bits)	13,11	13,11
DSP	640	640
PLLs	10	10
HVIO	54	27
HSIO	190	116
LPDDR4/x	x16	x32
MIPI 2.5G	2RX/2TX	4RX/4TX

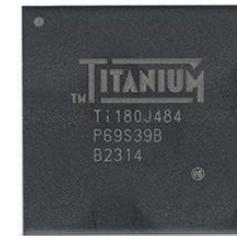
Package	J484D1	J484
Pitch	0.65mm	0.8mm
Size	15x15mm	18x18mm

# Ti90/120/180 Variants

Smallest Size	
J361	0.65mm, 13mm x 13mm HVIO:20, HSIO: 110, MIPI: 2 ports, LPDDR4/4x (x16): 48Gbps
I/O Rich	
G400	0.8mm, 16mm x 16mm HVIO: 74, HSIO: 200, MIPI: 0, LPDDR4/4x:0
Rich Hardcore IP	
J484 L484	0.8mm, 18mm x 18mm HVIO: 27, HSIO: 116, MIPI: 4 ports, LPDDR4/4x (x32): 96Gbps
High Performance	
G529	0.8mm, 19mm x 19mm HVIO: 48, HSIO: 210, MIPI: 0, LPDDR4/4x (x32): 105.6Gbps



Ti180 J361  
13x13 mm



Ti180 J484  
18x18 mm



Ti180 G529  
19x19 mm

Note: G400 and J484 support automotive grade

# Titanium Ti375 Highlight

## Quantum™ compute fabric

- TSMC 16nm process
- High performance, Low power fabric
- 0.95V and 0.85V (LP mode) support
- High DSP compute capability
- High Embedded Memory resource

## 3300-LPDDR4/4x Hard IP

- x32-bit LPDDR4/4x @ 3300Mbps
- LPDDR4x reduce I/O voltage by 50% for both memory & controller (1.1V to 0.6V)
- Harden DDR PHY and Controller IP, optimum performance and power

## Security

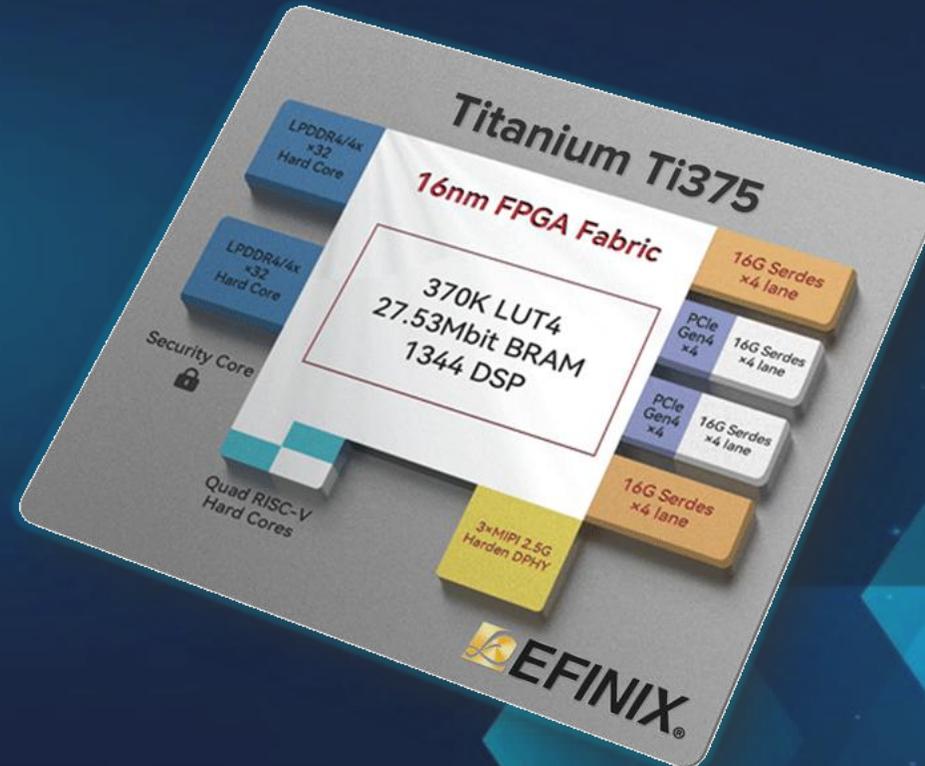
- AES-GCM Bitstream Encryption
- AES-GCM Symmetric Authentication
- RSA-4096 Asymmetric Authentication

## Qualification

- AEC-Q100

## Quad Core Risc-V RV32 SoC

- Quad Core RV32-IMACFD
- MMU, FPU, Custom Instruction support



## Quad 16Gbps High Speed Serdes

- Support x1, x2 and x4 configurations
- Support PCIe 4.0, 10G-KR, SGMII, PHY-only mode

## PCIe Gen4x4 Controller Hard IP

- Compliant with PCIe 4.0, 3.2, 2.1, and 1.1 Spec
- Support x1, x2 and x4 configurations
- Configure as Root Port (RP), or End Point (EP)
- Single Root IO Virtualization (SRIOV)

## 2.5Gbps MIPI-DPHY Hard IP

- 3 MIPI-DPHY 2.5Gbps x4 lanes Hard IP instances (RX & TX)
- CSI-2, DSI soft IP

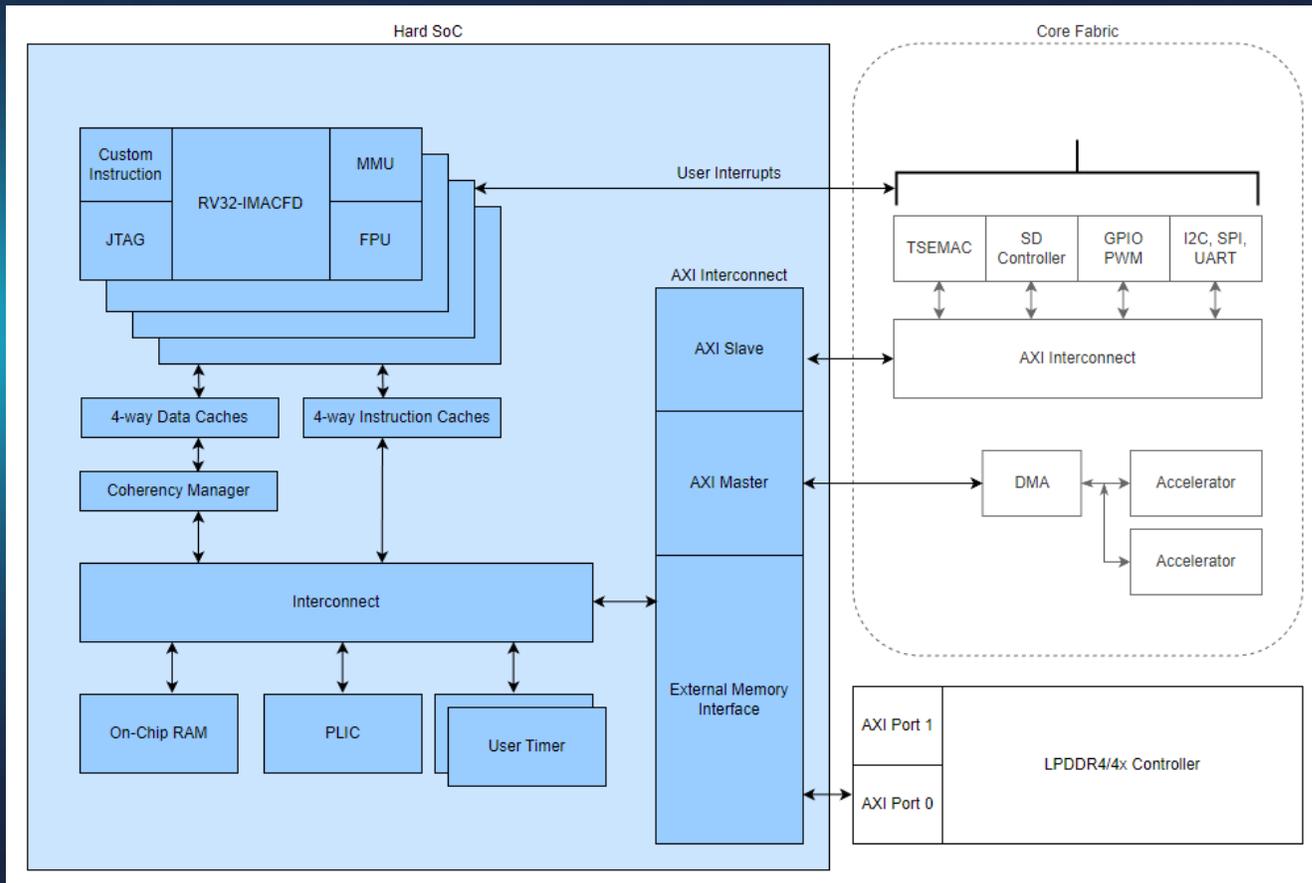
## High Voltage IO

- 3.3V, 2.5V, 1.8V capable

## High Speed IO

- LVDS 1.5Gbps
- MIPI-DPHY 1.5Gbps

# Titanium Quad Core RV32 SoC



- Quad Core RV32 Hard SoC
- CPU:
  - 6-stages pipeline in-order architecture
  - Instruction: IMACFD
  - Cache: I\$ & D\$, 4-ways 16KB each
  - MMU, FPU, Branch Predictor supports
  - Custom Instruction supports
- SoC:
  - 16KB on Chip RAM
  - Hard Wired 256b AXI4 External Memory to LPDDR4
  - 128b AXI Master @ 250MHz
  - 32b AXI Slave @ 250Mhz
  - 24 User Interrupts
  - CLINT timer, User timer, PLIC
- Target @1.0GHz CPU Fmax @ 450mW typical (4 cores)
- Linux & RTOS ready
- One design environment with Efinix' Sapphire SoC

# Titanium Ti135 Highlight

## Quantum™ compute fabric

- TSMC 16nm process
- High performance, Low power fabric
- 0.95V and 0.85V (LP mode) support
- High DSP compute capability
- High Embedded Memory resource

## 3300-LPDDR4/4x Hard IP

- x32-bit LPDDR4/4x @ 3300Mbps
- LPDDR4x reduce I/O voltage by 50% for both memory & controller (1.1V to 0.6V)
- Harden DDR PHY and Controller IP, optimum performance and power

## Security

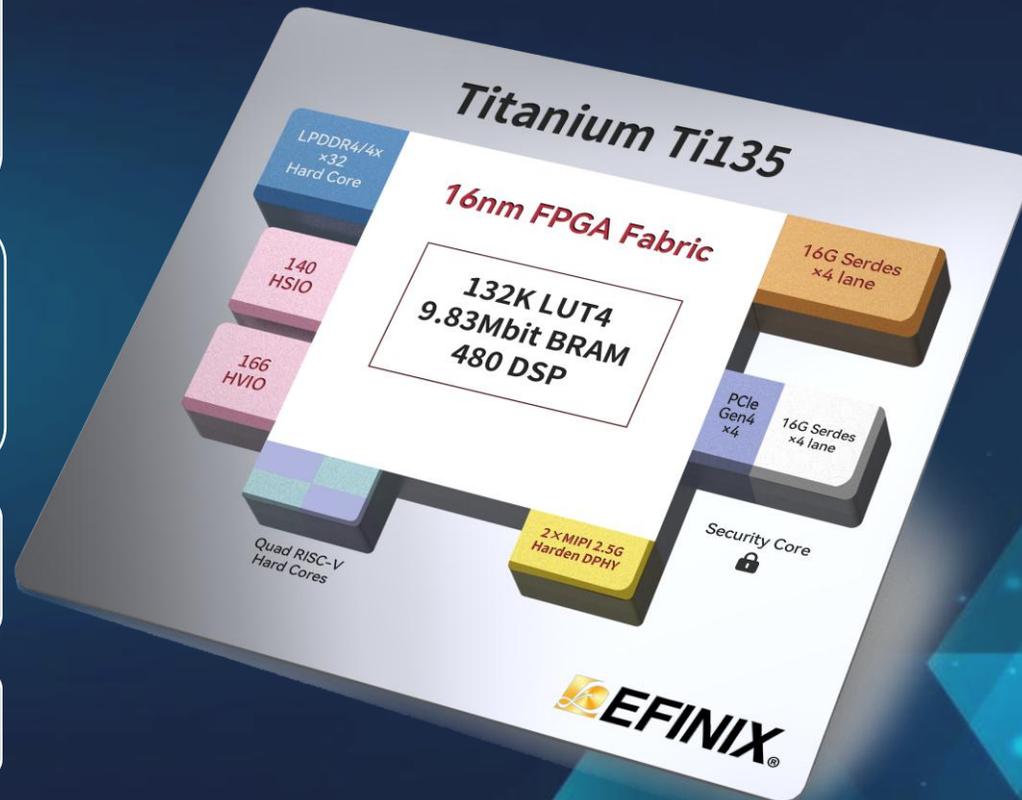
- AES-GCM Bitstream Encryption
- AES-GCM Symmetric Authentication
- RSA-4096 Asymmetric Authentication

## Qualification

- AEC-Q100

## Quad Core Risc-V RV32 SoC

- Quad Core RV32-IMACFD
- MMU, FPU, Custom Instruction support



## 2x Quad 16Gbps High Speed Serdes

- Support x1, x2 and x4 configurations
- Support PCIe 4.0, 10G-KR, SGMII, PHY-only mode

## PCIe Gen4x4 Controller Hard IP

- Compliant with PCIe 4.0, 3.2, 2.1, and 1.1 Spec
- Support x1, x2 and x4 configurations
- Configure as Root Port (RP), or End Point (EP)
- Single Root IO Virtualization (SRIOV)

## 2.5Gbps MIPI-DPHY Hard IP

- 2 MIPI-DPHY 2.5Gbps x4 lanes Hard IP instances (RX & TX)
- CSI-2, DSI soft IP

## High Voltage IO

- 3.3V, 2.5V, 1.8V capable

## High Speed IO

- LVDS 1.5Gbps
- MIPI-DPHY 1.5Gbps

## PLL

- Dynamic Reconfigure PLL
- Fractional PLL

# A Complete Product Portfolio



## General FPGA

IO Rich, Wide Range Selection, MIPI DPHY  
CSI, DDR



## Value for Mainstream Markets

Performance, Low Power, 12Gbps SerDes, LPDDR4 & MIPI  
DPHY 2Gbps



## High Performance & Low Power

Low Power, Size, 3.3Gbps LPDDR4/4x &  
MIPI DPHY 2.5Gbps



## Serdes Series

## Ultimate Compute & Connectivity

16/25Gbps Multi-Protocol SerDes, PCIE Gen4  
Controller, Quad Core RISC-V CPU

# New Family: Topaz



Topaz			Tz50	Tz110	Tz170	Tz75	Tz100	Tz200	Tz325
Logic Elements (LE)			52160	120584	161008	75520	101440	215360	326080
10K RAM (Mb)			2,4	6,41	11,14	5,34	6,32	15,77	19,22
DSP			140	320	544	264	312	840	1008
PLLs			4	10	10	12	12	12	12
GPIO			34	80	80	166	166	181	181
HSIO			146	232	232	140	140	235	235
MIPI DPHY 1.3G, support CSI-2/DSI			Yes	Yes	Yes	Yes	Yes	Yes	Yes
LPDDR4 (hard controller)			-	X32	X32	1x32	1x32	2x32	2x32
MIPI DPHY x4 2Gbps Hard IP			-	X4	X4	X2	X2	X3	X3
12.5/10.3 Gbps Serdes (-3/-2)			-	-	-	X8	X8	X16	X16
PCIe Gen3 (8G) hard controller			-	-	-	1x Gen3x4	1x Gen3x4	2x Gen3x4	2x Gen3x4
Harden Quad-Core Risc-V CPU			-	-	-	Yes	Yes	Yes	Yes
Package			HVIO/HSIO/MIPI/LPDDR4/SERDES						
F100	0.5mm	5.5x5.5mm	0,61,0,0						
F225	0.65mm	10x10mm	23,140,0,0						
F256	0.8mm	13x13mm	27,142,0,0						
J361	0.65mm	13x13mm		20,110,2,x16,0	20,110,2,x16,0				
G400	0.8mm	16x16mm		74,200,0,0,0	74,200,0,0,0				
J484	0.8mm	18x18mm		27,116,4,x32,0	27,116,4,x32,0				
N441	0.5mm	11x11mm				18,86,1,16,8	18,86,1,16,8		
N576	0.65mm	16x16mm				43,100,2,x32,8	43,100,2,x32,8		
N676	0.8mm	22x22mm				84,140,2,x32,8	84,140,2,x32,8		
N484	0.8mm	18x18mm				21,85,1,x32,8	21,85,1,x32,8	20,85,1,x32,8	20,85,1,x32,8
C529	0.8mm	19x19mm						51,176,1,x32,0	51,176,1,x32,0
N676	0.65mm	18x18mm						63,130,2,2x32,12	63,130,2,2x32,12



# Efinix Low Power FPGAs



	Trion	Topaz	Titanium
LE (k)	4-120	50-325	35-1000
MIPI CSI 2	1.5Gbps	HSIO: 1.3Gbps/Hard: 2Gbps	HSIO: 1.5Gbps/Hard: 2.5Gbps
MIPI DSI	NA	HSIO: 1.3Gbps/Hard: 2Gbps	HSIO: 1.5Gbps/Hard: 2.5Gbps
LVDS	800Mbps	1300 Mbps	1500Mbps
DDR Memory	DDR3 1066 Mbps	LPDDR4 2.4Gbps	LPDDR4/X up to 3.3Gbps
RISC-V	Soft : up to 120MHz	Soft up tp 250MHz/Hard Quad: 800MHz	Soft up tp 350MHz/Hard Quad: 1000MHz
SERDES	NA	up to 12.5Gbps	up to 16Gbps
PCI-E	NA	up to GEN3x4	up to GEN4x4
10GE	NA	soft IP	soft IP

# Automotive Ready Devices



AEC-Q100 (Grade 3) application

$T_j = -40 - 105^{\circ}\text{C}$

Speed Grade = Q4



T13F256

T20F256

T13F169

T20F169

AEC-Q100 (Grade 2) Application

$T_j = -40 - 125^{\circ}\text{C}$

Speed Grade = Q3



Ti60F225

Ti180J484

Ti120J484

Ti90J484



High Performance, Low Power  
Quantum Compute Fabric in TSMC 16nm

# Titanium Ti375/240/165/135/85



16Gbps PCIE Gen4 and  
Multi Protocol Serdes



Embedded Hardened  
Quad-Core Risc-V CPU



MIPI DPHY 2.5G Hard IP  
All HSIO support MIPI DPHY 1.5G



High Performance, Low Power  
LPDDR4/4x offering

# Benefit of Quantum architecture: Trion

Ta	25Deg. C										
AF	12.50%										
	LUT (k)	Reg. (k)	Frequency (MHz)	Memory (Mbit)	Mult	MIPI RX	DDR	Typ. Stb (mW)	Typ total (mW)	WC total (mW)	LP WC total (mW)
T8	7	3	10	0.05	4	0	0	0.205	2.7	2.9	2.9
T20	18	13	100	0.5	30	0	0	38	164	172	144
T35	30	20	100	0.5	30	x4 @1.5Gbps	LPDDR3x16/1066Mbps	45	440	464	400
T120	100	70	100	2.5	100	x4 @1.5Gbps	LPDDR3x16/1066Mbps	75	1007	1061	902

LP: Low Power (1.1V vs 1.2V)

- Utilization >90%
- All XLR from the datasheet are accessible, no reduction because of routing as routing is using additional XLRs which are not accessible for logic.

# Benefit of Quantum architecture: Titanium

Ta	25Deg. C												
AF	12,50%												
Device	LUT (k)	Reg. (k)	Frequency (MHz)	Memory (Mbit)	Mult	PCI-E	Hardwired QUAD RISC-V	MIPI RX	DDR	Typ. Stb (mW)	Typ total (mW)	WC total (mW)	LP WC total (mW)
Ti60	50	30	200	1	100	0	0	0	0	52	225	269	183
Ti180	160	100	200	10	500	0	0	x4 @2.5Gbps	LPDDR4x/x16/3Gbps	80	1520	1607	1362
Ti135*	100	70	200	9	400	x4 Gen4	Quad @0.9GHz	x4 @2.5Gbps	LPDDR4x/x16/3Gbps	40	3140	4004	3015
Ti375*	320	200	200	20	1000	x4 Gen4	Quad @0.9GHz	x4 @2.5Gbps	LPDDR4x/x16/3Gbps	94	4800	6463	4083

LP: Low Power (0.85V vs 0.95V)

\*: preliminary data

- 60K LE in a 3.5x3.4mm package
- All XLR cells are available, calculate 5-10% for routing.
- QUAD Risc-V @1GHz: 400mW
- LPDDR4x/x16/@3Gbps: 650mW





# SoftIP/ RISC-V<sup>®</sup> SOC offering

# Continue Innovation

## Sapphire SoC

- Soft Processor (Performance)
- RV32 with IMAFDC extension
- 100-400Mhz System Clock
- Quad Core
- Multi-way Instruction and Data Cache
- MMU, Linux Capable
- Hardware FPU
- Custom Instruction

## Sapphire Lite

Efinity 2023.2

- Soft Processor (Area)
- RV32 with IM extension
- 100-200Mhz System Clock
- Single Core
- Instruction and Data Cache
- **4KLE resource consumption**

## Sapphire High Performance

Ti375, Ti240,  
Ti165, Ti135, Ti85

- Hard Processor (High Performance)
- RV32 with IMAFDC extension
- **>1GHz System Clock**
- Quad Core
- Multi-way Instruction and Data Cache
- MMU, Linux Capable
- Hardware FPU
- Custom Instruction
- **~500mW CPU Hard IP power**

Same Embedded Software Development, IDE, Tool Chain, Driver



Risc-V IDE



Debugger



Linux OS



RTOS



Zephyr OS

Ethernet  
Linux/FreeRTOS  
Solution Stack

SD Card  
Storage  
Solution Stack

and more..

# Comparison Hard VS Soft Sapphire

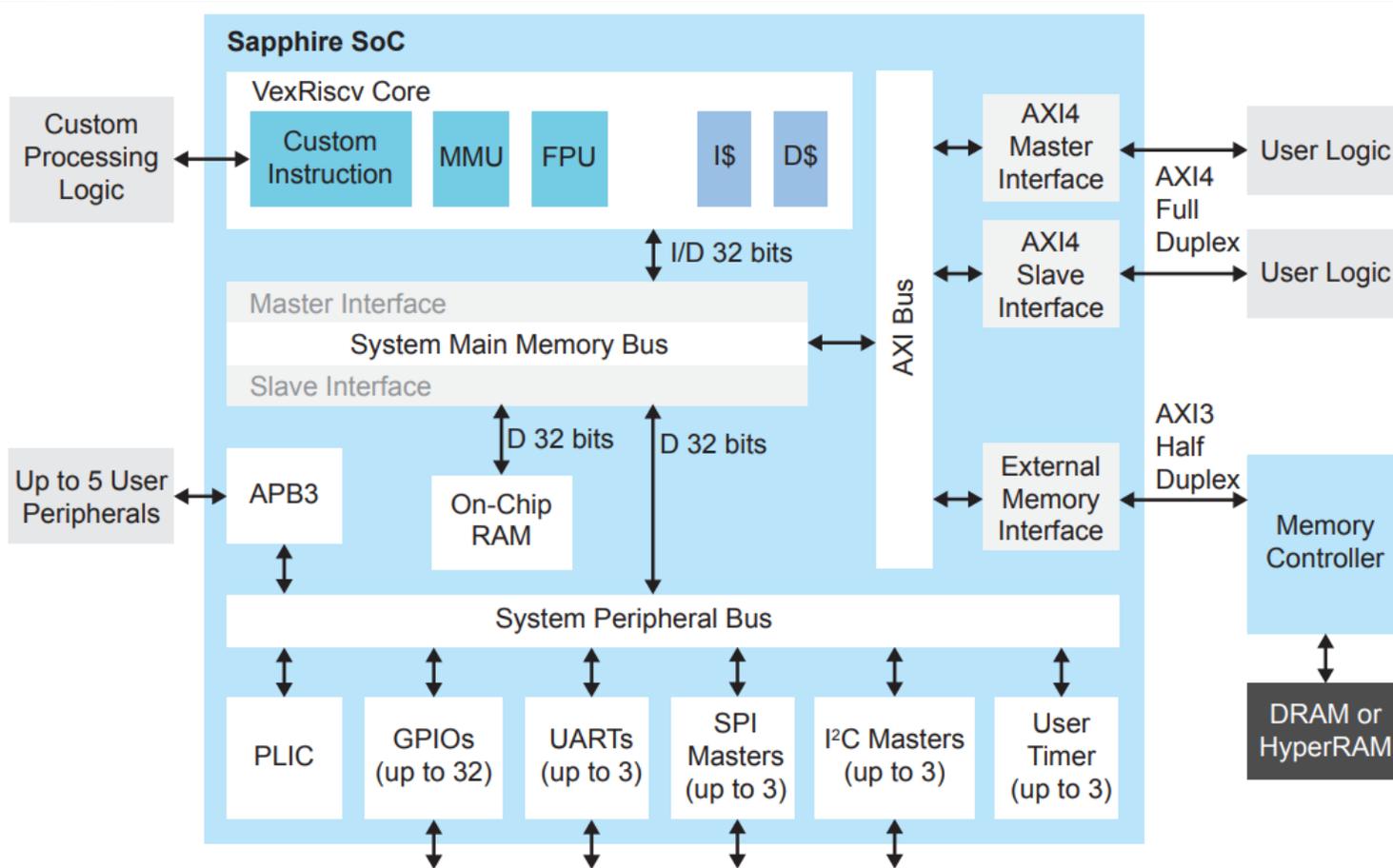
## Hard Sapphire

- 128-bit internal bus
- Improves data path latency between CPU and periphery
- Static branch predictor
- Unblocked operation for custom instruction
- Dedicated FPU for each core
- 8 Hardware breakpoints for debug module
- Data coherency between CPU and DMA channel (AXI Master)
- Additional write buffer to improve write performance to external memory

## Soft Sapphire

- Max 64-bit internal bus
- Higher latency due to pipelining, trade-off for fmax
- No branch predictor
- Stall CPU pipeline until get the result from custom ALU
- Shared FPU for multi-core configuration
- Up to 4 hardware breakpoints
- No data coherency between CPU and DMA channel (AXI master)
- No write buffer introduced in SoC

# Sapphire



- New:
  - LINUX MMU
  - FPU
  - Custom Instructions

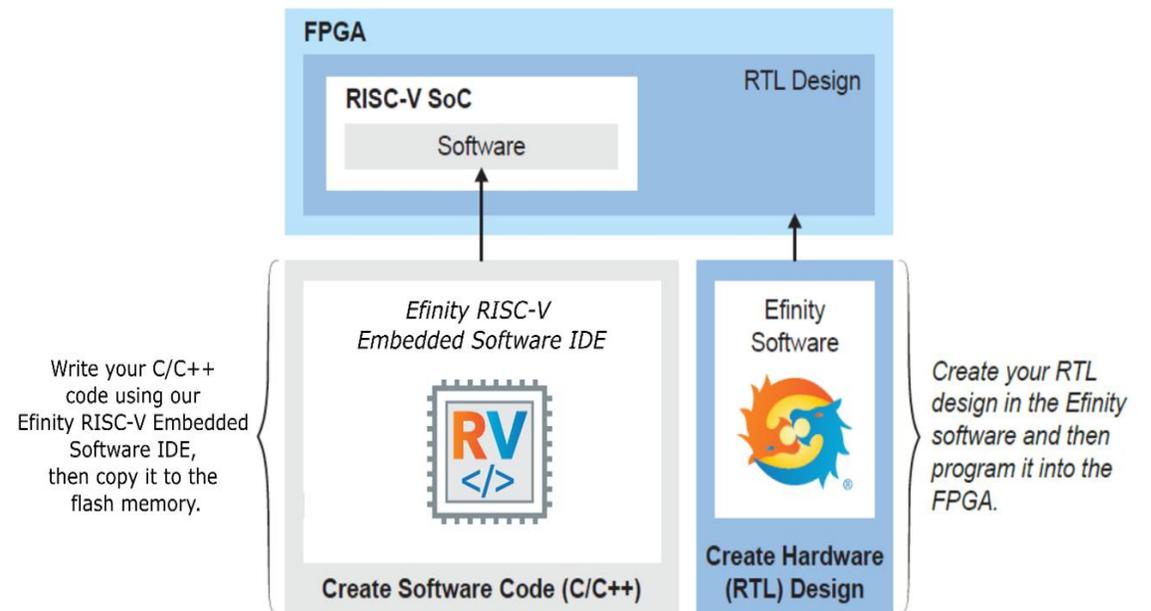
The screenshot shows a configuration tool interface with a sidebar listing hardware components and a main panel with configuration options. The main panel includes the following settings:

- Option: Standard
- Core Number: 1
- Frequency (MHz): 100
- Peripheral Clock:  Use separate clock domains for the peripherals and CPU.
- Cache:  Include a cache controller.
- Custom Instruction:  Include the custom instructions interface.
- Linux Memory Management Unit:  Include the memory management unit (MMU) with sv32 page-based virtual memory.
- Floating-point Unit:  Include the floating point unit with F and D instructions set extension.
- Atomic Extension:  Include the atomic instructions set extension.
- Compressed Extension:  Include the compressed instructions set extension.

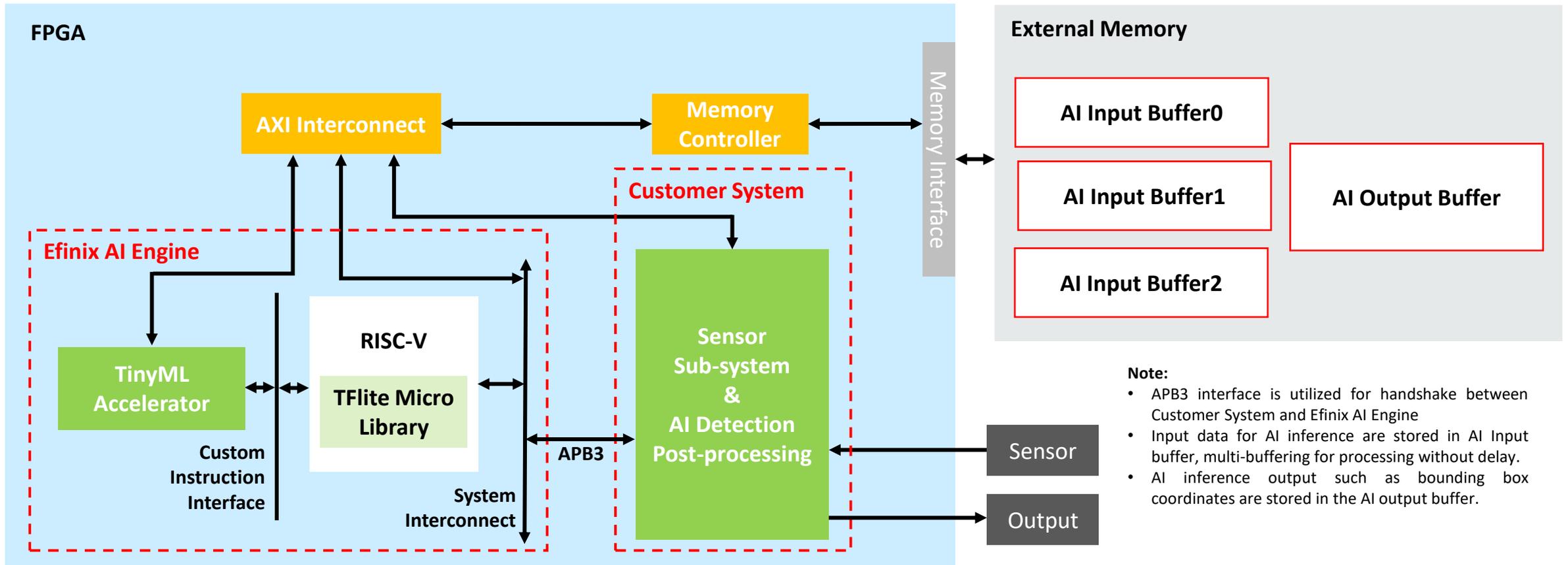
At the bottom right, there are buttons for "Show Confirmation Box", "Generate", and "Close".

# Required Software and Tools

- Efinity<sup>®</sup> software
- Pre-compiled, open-source SDK
- Eclipse IDE for managing projects and software with Ashling GUI
- RISC-V GCC compiler and GDB debugger
- OpenOCD debugger for debugging applications
  - Support of Lauterbach Tracer
- Windows build tools (Windows)
- Available from our web page
  - <https://www.efinixinc.com/products-riscv.html>



# AI: Ease of Integration



# AI: TinyML Implementation

Follow the typical implementation ways

- Module training
- Quantization/Converter
- TinyML Accelerator
- AI inference on FPGA



# AI: Differentiation Advantages

## ➤ Custom AI Acceleration

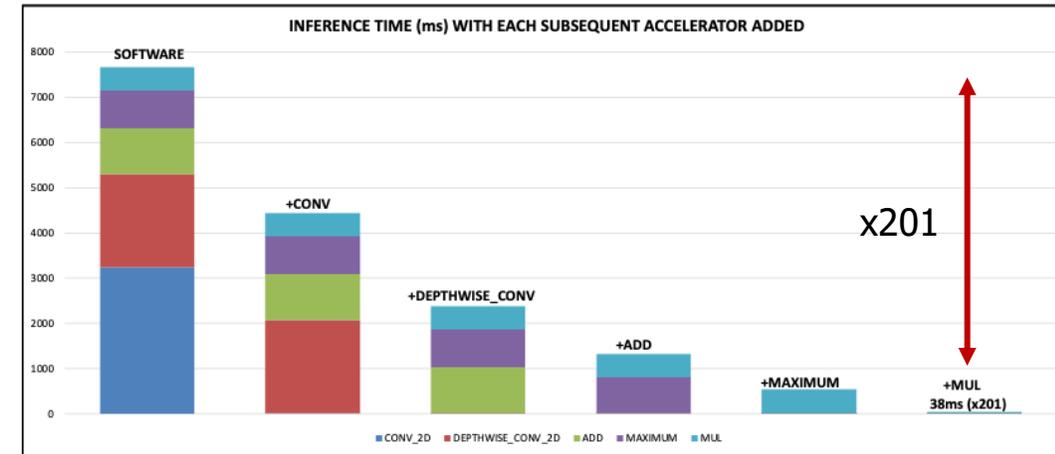
- Customizable TinyML accelerator using GUI-based Generator
- Resource estimator to facilitate design space exploration

## ➤ Fast Prototyping

- Single platform that facilitates end-to-end AI design flow
- Fast Go-to-market

## ➤ Efinix 16nm Titanium FPGAs

- Low Power + Small Form Factor
- High Performance & Scalable Density



Layer/Module	LUtEs	FFs	ADDs	RAM Blocks	DSP Blocks
1 CONV_DEPTHW	12516	8870	5323	41	48
2 ADD	1904	2674	747	0	8
3 MUL	2416	2168	695	0	7
4 MIN_MAX	926	936	139	0	0
5 TINYML_CACHE	880	488	172	10	0
6 COMMON	3065	1073	116	26	0
7 TINYML ACCELERATOR	21707	16209	7192	77	63

Hardware Definition File  
Generated hardware definition file : output/mediatek\_face\_landmark/defines.v...  
Include the file under : source/tinyml  
End File Generation

Software Definition File  
Generated software definition file : output/mediatek\_face\_landmark/define.cc ...  
Generated software definition file : output/mediatek\_face\_landmark/define.h ...  
Include the file under : embedded\_sw/SuppIveSC/software/standalone/application\_name/src/model  
End File Generation

Software Model File  
Generated model file : output/mediatek\_face\_landmark/mediatek\_face\_landmark\_model\_data...  
Generated model file : output/mediatek\_face\_landmark/mediatek\_face\_landmark\_model\_data.h...  
Include the file under : embedded\_sw/SuppIveSC/software/standalone/application\_name/src/model  
End File Generation

NOTES:  
1. Efinix TinyML platform supports .tflite model with full integer quantization.  
2. LITE accelerator is a lightweight accelerator with less resource usage.  
3. STANDARD accelerator is a high performance accelerator with more resource usage.  
4. TinyML cache is an optional feature to speed-up data access of STANDARD mode accelerator.  
5. Resource Estimator estimates resource usage of TinyML accelerator based on configured parameter setting for Efinix Titanium FPGAs. Open .tflite model file to get started.

Model File : mediatek\_face\_landmark.tflite

Open Generate





# Development Kits

# Development Kits

Trion T120 BGA576 Development Kit



Featuring T120 FPGA with hardened MIPI CSI-2 and DDR DRAM

Trion T120 BGA324 Development Kit



Featuring T120 FPGA with hardened MIPI CSI-2 and DDR DRAM

Trion T20 MIPI Development Kit



Featuring T20 FPGA with hardened MIPI CSI-2 and D-PHY

Trion T20 BGA256 Development Kit



Featuring the T20 BGA256 FPGA

Trion T8 BGA81 Development Kit



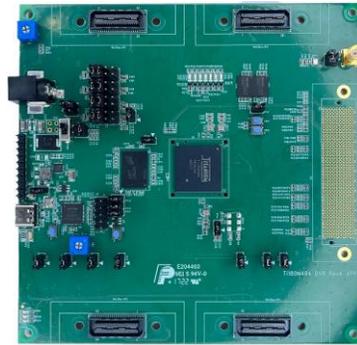
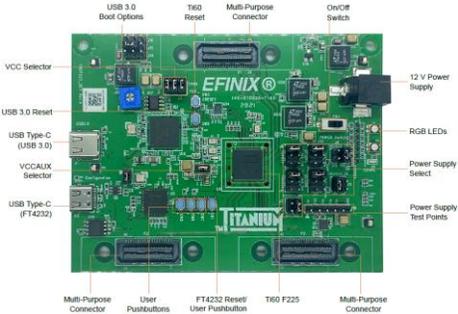
Featuring the T8 BGA81 FPGA

Xyloni Development Kit



Thumb-sized USB board for hobbyists and makers

# Titanium Development Kits



Ti60F225C-DK  
available

Ti180J484C-DK  
available

Ti375C529C-DK  
available

Ti375C1156C-DK  
available

## Daughter Cards



EFX\_DC\_GPIO\_B  
LVDS expansion



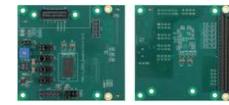
EFX\_TI60\_2x30\_IFB  
Dual MIPI to DSI



EFX\_DC\_CAM\_FPC15\_B  
Raspberry PI Con



EFINIX\_IFB\_PICAMX2  
Dual Raspberry PI Con



EFX\_FMC\_DDR3\_GBIO  
FMC DDR3 and GPIO



EFX\_GPIO\_FL\_DC\_C  
FMC to QSE

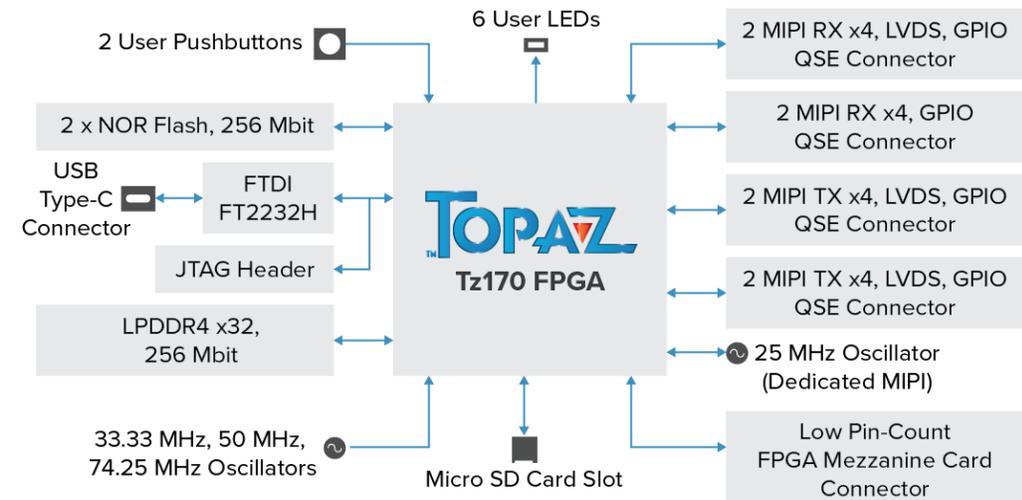


EFX\_RGMII  
Ethernet card

# Topaz: Tz170J484C-DK

## Main Features:

- Tz170 FPGA in a 484-ball FineLine BGA package
- 2x 256Mb SPI NOR flash memories
- Four MIPI, LVDS, and GPIO high-speed connectors to attach daughter cards
- FMC LPC connector
- Micro-SD card slot
- USB Type-C connector for programming the flash or Tz170 FPGA using the Efinity® software
- 6 User LEDs
- 2 User pushbutton switches
- 33.33 MHz, 50 MHz, and 74.25 MHz oscillators for PLL input
- 12.0 V power supply connector
- Resale Price: \$400
- Ordering Code: **Tz170J484C-DK**





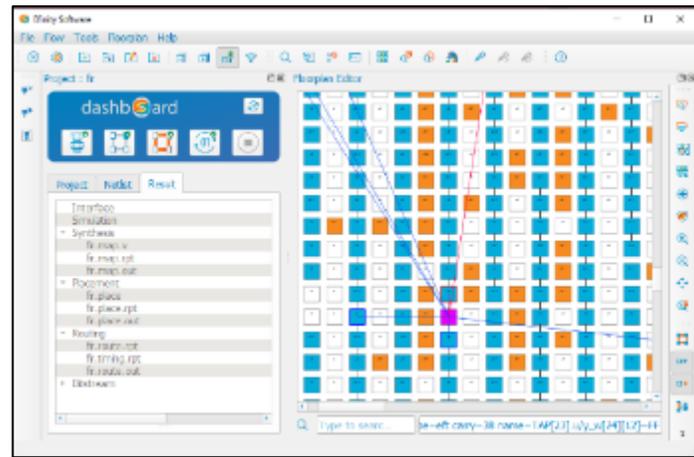
Software Efinity

# Efinity<sup>®</sup> Integrated Development Suite

- Standard RTL-to-bitstream FPGA development tool **(free of charge)**
- Core and interface concept enables system integration

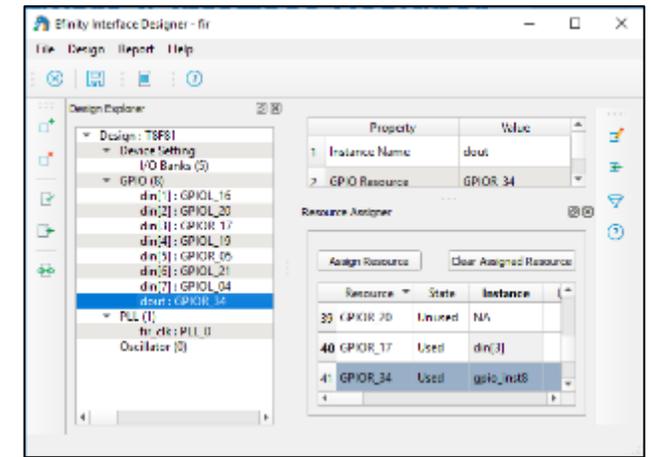
## Core Designer

FPGA Core Fabric  
(Synthesis, Place and Route)

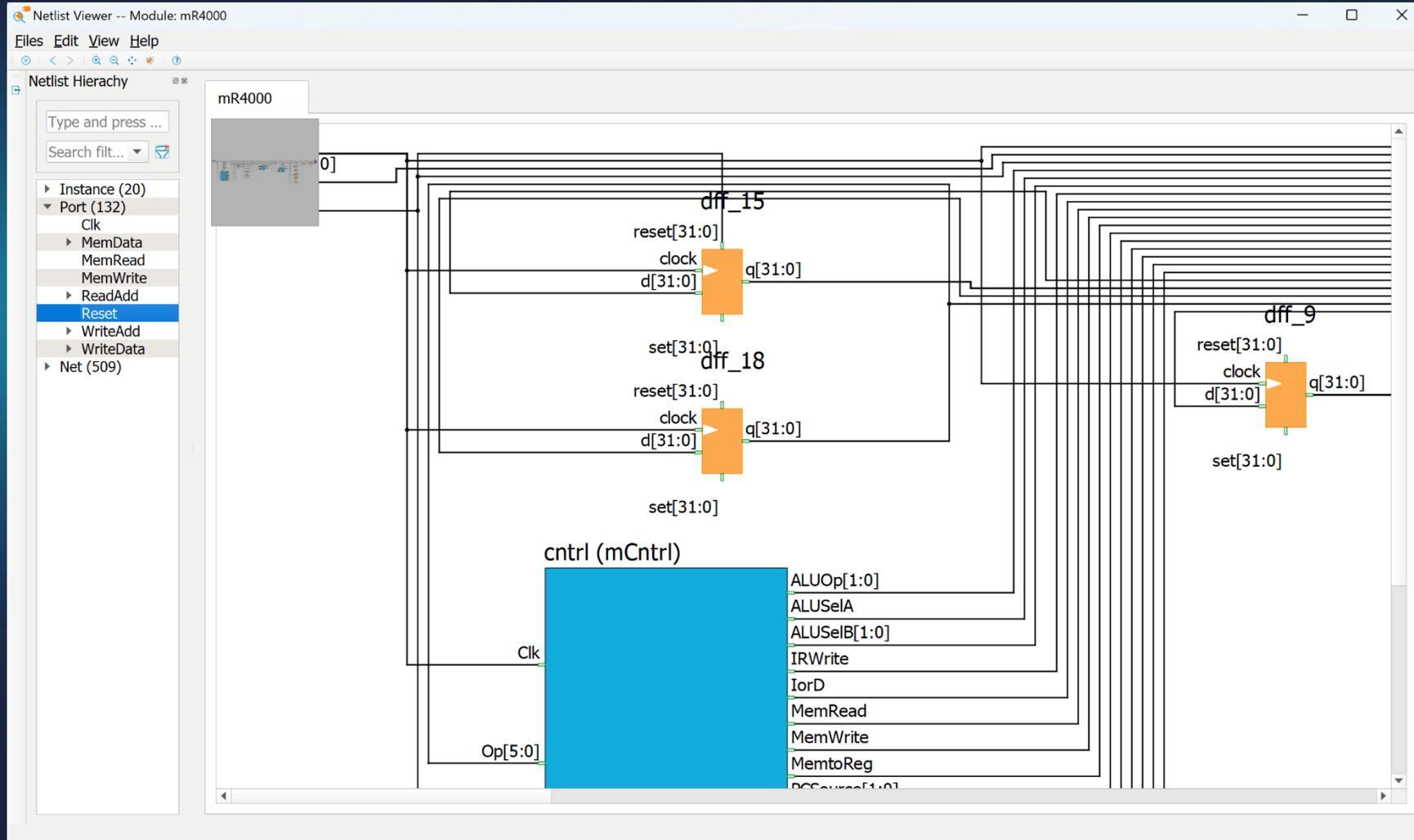


## Interface Designer

Subsystems  
(I/O, DDR, MIPI, etc.)



# Netlist Viewer



# IP Manager



IP Catalog

Search

- Installed IP
  - Efinix
    - AXI Infrastructures
      - AXI Data FIFO
      - AXI Interconnect
      - AXI4-Stream Switch
    - Arithmetic
      - CORDIC
      - Divider
      - Integer Square Root
    - Bridges and Adaptors
      - APB Interconnect
      - APB3 to AXI4 Lite converter
      - Data Pipeline
      - Direct Memory Access
    - Ethernet
      - 10G Ethernet Mac
      - Triple Speed Ethernet MAC
    - Foundation IP
      - PLL Dynamic Reconfiguration
      - Trion PLL Auto-reset
    - MIPI
      - MIPI 2.5G CSI-2 RX Controller
      - MIPI 2.5G CSI-2 TX Controller
      - MIPI BIDIR DPHY RX
      - MIPI BIDIR DPHY TX
      - MIPI CSI-2 RX Controller
      - MIPI CSI-2 TX Controller
      - MIPI DPHY RX
      - MIPI DPHY TX
      - MIPI DSI RX Controller
      - MIPI DSI TX Controller
    - Memory
      - BRAM Wrapper
      - FIFO
    - Memory Controllers
      - ASMI SPI Flash Controller
      - DDR Hard Memory Controller - Calibration and Reset
      - DDR Hard Memory Controller-Reset
      - DDR3 Soft Controller
      - HyperRAM Controller
      - JTAG SPI Flash Loader
      - SD Host Controller
      - SDRAM Controller
      - Trion DDR Calibration and Debug IP
    - Processors and Peripherals
      - Sapphire High Performance SoC
      - Sapphire SoC
    - Serial Interface Protocols
      - I2C
      - UART

+ Add    Next>>    Close

IP Configuration

Module Name:

efx\_i2c\_controller 5.0

General    Deliverables    Summary

8-bits I2C Slave Address (decimal, bit0 is ignored)

I2C Data Transfer Speed

I2C Controller Mode

Data Width

Core Clock Frequency (MHz)

SDA/SCL Spike Filtering Cycle

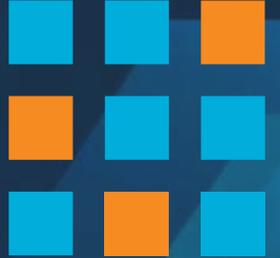
General    Deliverables    Summary

Generate these deliverables:

- Source
- Example Design (T20F256\_devkit)
- Example Design (TI60F225\_devkit)
- Testbench

Show Confirmation Box    Generate    Close

# Floorplan Viewer



Floorplan

Cell Browser

Type regex to filter...  Regex

Leaf Cells

- (37,70) ALUOp[0]~FF
- (32,62) ALUOp[1]~FF
- (37,61) ALUSelA~FF
- (32,67) ALUSelB[0]~FF
- (53,65) AUX\_ADD\_CI\_alu/...
- (219,165) Clk
- (101,145) GND
- (71,89) Instruction[0]~FF
- (82,47) Instruction[10]~FF
- (82,58) Instruction[11]~FF
- (19,61) Instruction[12]~FF
- (82,75) Instruction[13]~FF
- (68,119) Instruction[14]~FF
- (71,84) Instruction[15]~FF
- (31,114) Instruction[16]~FF
- (31,118) Instruction[17]~FF
- (71,105) Instruction[18]~FF
- (101,95) Instruction[19]~FF
- (37,60) Instruction[1]~FF

Inspector

Property	Value
1 Coordinate	(71, 89)
2 Name	Instruction[0]~FF
3 Type	eft
4 Route ...	2

Type to search... Block: (71,89) type=eft routethru=2 name=Instruction[0]~FF

Legend

Filter

- Always Apply
- Block Name
- Block Type
- Routing
- Carry Chain

# SERDES access: PCI-E

The screenshot displays the Efinix Interface Designer software interface, showing the configuration of a PCI Express (PCI-E) SerDes access. The interface is divided into several panes:

- Design Explorer:** Shows the project hierarchy, including Design: T1135N484, Device Setting, I/O Banks (8), Configuration, Clock/Control Configuration (4), GPIO (0), PLL (0), Oscillator (0), LVDS / SLVS TX (0), LVDS / SLVS RX (0), Bidirectional LVDS / SLVS (0), MIPI TX Lane (0), MIPI RX Lane (0), MIPI DPHY TX (0), MIPI DPHY RX (0), JTAG User Tap (0), DDR (0), PLL SSC (0), PCI Express (1), and various Ethernet and PMA Direct instances.
- Block Summary:** A table listing properties and values for the 'pcie\_inst1' instance.
- Block Editor:** Shows the configuration for the 'pcie\_inst1' block, including Instance Name, PCIe Resource, Generation (Gen3 (8.0 Gbps)), Link Width (x4), Mode, Endpoint, Link Width (x4), Generation (Gen3 (8.0 Gbps)), Maximum Payload Size (512 bytes), SRIS Enable (false), Reference Clock (External), Reference Clock Frequency (100.000), Reference Clock Source (CMN\_REFCLK0), External Reference Clock (CMN\_REFCLK0), Enable 50 Ω to ground on-die termination for REFCLK0 (true), Reference clock from on-board crystal (true), Function, Subsystem Vendor ID (0x1f7a), Total Physical Functions (4), Vendor ID (0x1f7a), Physical Function 0, BAR0 Aperture (4 KB), BAR0 Control (32 bit non-prefetchable memory), BAR1 Control (Disabled), BAR2 Control (Disabled), and BAR3 Control (Disabled).
- PCI Express Reset:** Shows the configuration for the PCI Express Reset block, including Resource (Unknown), Instance (Unknown), Hot Reset Output Pin Name (pcie\_inst1\_HOT\_RESET\_OUT), Link Down Reset Pin Name (pcie\_inst1\_LINK\_DOWN\_RESET\_OUT), Reset Acknowledge Pin Name (pcie\_inst1\_RESET\_ACK), and Reset Request Pin Name (pcie\_inst1\_RESET\_REQ).
- Subsystem Vendor ID:** Shows the configuration for the Subsystem Vendor ID block, including Vendor ID (0x1f7a), Total Physical Functions (4), Physical Function 0, BAR0 Aperture (4 KB), BAR0 Control (32 bit non-prefetchable memory), BAR1 Aperture (4 KB), BAR1 Control (Disabled), BAR2 Aperture (4 KB), BAR2 Control (Disabled), and BAR3 Aperture.
- AXI:** Shows the configuration for the AXI block, including Enable AXI Master Interface (checked), Enable AXI Slave Interface (checked), AXI Clock Pin Name, Invert AXI Clock Pin (unchecked), AXI Reset (Active-Low) Pin Name (pcie\_inst1\_USER\_AXI\_RESET\_N), Master/Slave selection, and Read/Write Address/Response Channels.

# SERDES access: Ethernet 10/5GE

The screenshot displays the Efinix Interface Designer software interface for configuring a SERDES block. The main window is divided into several panes:

- Design Explorer:** Shows the project hierarchy for 'Design: T1135N484', including Device Setting, I/O Banks (8), Configuration, and various peripheral blocks like PLL, Oscillator, LVDS, MIPI, and PCI Express.
- Block Summary:** A table listing properties and their values for the selected block.
- Block Editor:** Provides a detailed view of the block's configuration, including checkboxes for 'Enable Auto Negotiation (AN) Clause 37', 'Enable Forward Error Correction (FEC)', and 'Invert RX/TX Polarity'. A speed dropdown menu is currently set to 10Gbps.
- Clock and Reset Panel:** Configures the interface clock input connection type (rdk), pin names (eth10g\_inst1\_PCS\_RST\_N\_RX, eth10g\_inst1\_PCS\_RST\_N\_TX, eth10g\_inst1\_PHY\_RESET\_N), and reset pins.
- Common Instance Name Panel:** Sets the instance name to 'cmn\_inst2', reference clock frequency to 156.250 MHz, and source to 'External'. It also shows the external clock resource as 'CMN\_REFCLK0' and has the 'Enable 50 Ω to ground on-die termination for REFCLK0' checkbox checked.

Property	Value
1 Instance Name	xgmil_inst1
2 I/O Resource	Q0_LN0
3 Control Register	
4 Enable Auto Negotiation (AN) Clause 37	true
5 Enable Forward Error Correction (FEC)	false
6 Invert RX Polarity	false
7 Invert TX Polarity	false
8 Speed	10 Gbps
9 USXGMII AN Ordered set code	0x3
10 Clock and Reset	
11 Interface Clock Input Connection Type	rdk
12 Control	
13 Enable KR Base	true
14 Config	
15 Common Instance Name	cmn_inst1
16 Reference Clock	
17 Reference Clock Frequency (MHz)	156.250
18 Reference Clock Source	External
19 External Reference Clock	CMN_REFCLK0
20 Enable 50 Ω to ground on-die termination for REFCLK0	true
21 Pins	
22 Clock and Reset	
23 Interface Clock Input Pin Name	
24 PCS Receive Reset Pin Name	xgmil_inst1_PCS_RST_N_RX
25 PCS Transmit Reset Pin Name	xgmil_inst1_PCS_RST_N_TX

# SERDES access: Ethernet 1.25/2.5G

The screenshot displays the Efinix Interface Designer software interface for a device named 'byte\_enable\_test'. The interface is divided into several panels:

- Design Explorer:** Shows a hierarchical tree of components. Under 'Device Setting', 'I/O Banks (8)' is expanded to show 'Clock/Control Configuration (4)'. Within this, 'SGMII (0)' is selected, and its 'Control Register' is expanded to show 'sgmii\_inst1'.
- Block Summary:** A table listing properties and their values for the selected block.
- Block Editor:** A configuration window for the 'sgmii\_inst1' block, showing various settings.

Property	Value
1 Instance Name	sgmii_inst1
2 SGMII Resource	
3 Control Register	
4 Enable Activity Status for LED	false
5 Enable SGMII Auto Negotiation (AN)	true
6 Speed	10/100/1000 Mbps
7 Clock And Reset	
8 Interface Clock Input Connection Type	rdclk
9 Interface Clock X2 Input Connection Type	rdclk
10 Config	
11 Common Instance Name	cmn_inst2
12 Remove 1 Preamble Byte for Even Number of Idles	false
13 Reference Clock	
14 Reference Clock Frequency (MHz)	156.25
15 Reference Clock Source	External
16 External Reference Clock	CMN_REFCLK0
17 Enable 50 Ω to ground on-die termination for REFCLK0	true
18 Pin	
19 Clock And Reset	
20 Interface Clock Input Pin Name	
21 Interface Clock X2 Input Pin Name	
22 PCS Receive Reset Pin Name	sgmii_inst1_PCS_RST_N_RX
23 PCS Transmit Reset Pin Name	sgmii_inst1_PCS_RST_N_TX
24 PHY Lane Reset Pin Name	sgmii_inst1_PHY_RESET_N
25 Control	

The Block Editor shows the following configuration for the 'sgmii\_inst1' block:

- Enable Activity Status for LED
- Enable SGMII Auto Negotiation (AN)
- Speed: 10/100/1000 Mbps (selected), 2.5 Gbps

# SERDES access: PMA direct

The screenshot displays the Efinix Interface Designer software interface, showing the configuration of a SerDes block for PMA direct access. The interface is divided into several panes:

- Design Explorer:** Shows the project hierarchy, including I/O Banks, Configuration, and various SerDes blocks like pma\_direct\_inst1.
- Block Summary:** A table listing properties and values for the pma\_direct\_inst1 block.
- Block Editor:** A detailed configuration window for the pma\_direct\_inst1 block, showing various tabs like Base, Control Register, Pins, and Common Properties.
- Control Register:** A window for configuring the Control Register, showing fields for Instance Name, PMA Direct Resource, Data Rate, SerDes Width, Mode, Bonding Mode, Tx equalization mode, and Deemphasis.
- Common Properties:** A window for configuring common properties, showing fields for Interface Transmit Clock Pin Name, Interface Receive Clock Pin Name, Reference Clock Frequency, and Reference Clock Pin Name.

Property	Value
1 Instance Name	pma_direct_inst1
2 PMA Direct Resource	
3 Control Register	
4 Data Rate (Gbps)	5.00000
5 SerDes Width (Bits)	40
6 Mode	TX FIFO, RX FIFO
7 Bonding Mode	x1
8 Tx equalization mode	Deemphasis
9 Deemphasis	Off
10 Clock and Reset	
11 Transmit Clock Input Connection Type	rclk
12 Receive Clock Input Connection Type	rclk
13 Config	
14 Common Instance Name	cmn_inst3
15 Reference Clock	
16 Reference Clock Frequency (MHz)	156.25
17 Reference Clock Source	External
18 External Reference Clock	CMN_REFCLK0
19 Enable 50 $\Omega$ to ground on-die termination for REFCLK	true
20 APB	
21 Enable Advanced Peripheral Bus	true
22 Clock and Reset	
23 Enable PHY Quad Reset Pin	false
24 Pins	
25 Clock and Reset	

# Package Planner



Package Planner - r4000

File View Help

Package View

### 225-ball FBGA Pinout Diagram

Top View Device Name: Ti60F225

View Configuration

Report Pin information

Pin Number: A2  
Pin Name: GPIOA\_N\_18  
Pin Type: HSIO or Multi-Function  
Signal Name: N/A  
Direction: N/A  
I/O Bank: 1B  
I/O Bank Voltage: 1.8 V  
I/O Standard: N/A  
Pull Type: N/A  
Block Type: HSIO  
Block Instance: N/A  
Resource Name: GPIOA\_PN\_18, GPIOA\_N\_18  
MIPI Rx Group: I2  
Function: User IO/ PLL\_CLKIN

# Hardware Debugger



The screenshot displays the Efinity Debugger interface with the following components:

- Program Configuration:** USB Target: Titanium Ti60F225 Development Kit; USB Info: ID: 0403:6011; Bitstream: ...ing\_for\_new\_customer/Tutorial\_larger/outflow/Tutorial\_larger.bit; Device Status: Last Updated: Thu Jun 13 24 16:07:18; Debugging: 0x10660a79.
- Core Status:** Idle (highlighted in green), Waiting for Trigger, Post-Trigger, Full.
- Capture Status:** Segment 0 of 1, Segment sample 0 of 1024, Total sample 0 of 1024.
- Waveform Path:** ...g\Flow\_Training\_for\_new\_customer\Tutorial\_larger\la0\_waveform.vcd.
- Trigger Setup:** Trigger Mode: Basic Only; Trigger Condition: Global 'AND'; Trigger Table:

Name	Operator	Radix	Value	Port
counter_ins...	==	Bin	XXXXXXXXXXXXXXXXXXXXXXXXXXXX0000000	probe0[31:0]
- Console:** Shows a list of signals including stopn, resetn, and counter\_inst/cnt[31:0] through [6:0].
- Waveform:** A timing diagram showing signals at 8CC4AA00 through 8CC4AA05 over a 5 ns period.

# Efinity Transceiver Debugger

The screenshot displays the Efinity Transceiver Debugger application. The interface is divided into several sections:

- Program:** Contains configuration fields for USB Target (Ti375N1156-Serdes-CEM-EngBrd15), USB Info (ID: 0403:6010 S/N FT9VBB9P), Bitstream, Device Status (Last Updated: Mon Jun 24 24 13:02:01), and Debugging (0x006a0a79).
- Console:** Shows a log of system events, including disconnection from a URL, board profile loading, and device ID validation.
- Eye Diagram Plot:** A central plot showing signal quality. The plot is labeled "Eye Diagram Plot" and has a color scale from 0 to 1000. The horizontal axis is labeled "Steps" with values -40, 0, and 40. The vertical axis is labeled "Steps" with values -60 and 60. Below the plot, it indicates "Horizontal Open: 46 Steps" and "Vertical Open: 85 Steps".
- Configuration:** A section titled "Eye Diagram Plot Configuration" with a table of settings:

Parameter	Value
1 Selected Lane	3
2 Vertical Offset Value	60
3 Vertical Offset Step	1
4 Horizontal Offset Value	40
5 Horizontal Offset Step	1

# ISO26262/ ICE61508



The manufacturer may use the mark:



Revision 1.0 August 4, 2023  
Surveillance Audit Due  
September 1, 2026

## Certificate / Certificat Zertifikat / 合格証

EFI 2207092 C001

*exida* hereby confirms that the:

**Efinity® IDE and Toolchain v2023.1**

**Efinix Technology (M) Sdn. Bhd.  
Penang - Malaysia**

Has been assessed per the relevant requirements of:  
**IEC 61508:2010 and ISO 26262:2018**

and meets requirements providing a level of integrity to:  
**SIL 4 / ASIL D Qualified**

### Tool Functions:

The Efinity® IDE and Toolchain suite is an integrated development environment designed for Efinix FPGA development. Using Efinity, customers can develop, compile and test their FPGA design from RTL source code all the way down to bitstream programming on FPGA development boards.

### Application Restrictions:

The tools of the Efinity® IDE and Toolchain must be used per the defined use cases, and all requirements specified for the tool users (conditions and assumptions of use) shall be fulfilled, as described in the Functional Safety Manual for each tool.

Efinity® IDE and  
Toolchain

## Certificate / Certificat / Zertifikat / 合格証

EFI 2207092 C001

### SIL 4 / ASIL D Tool Qualification:

The Efinity® IDE and Toolchain have met the requirements for support tools up to Safety Integrity Level (SIL) 4 of IEC 61508-3 (section 7.4.4). The product has also met the requirements for confidence in use of software tools of Automotive Safety Integrity Level (ASIL) D of ISO 26262-8 (Section 11). These are intended to achieve sufficient integrity against systematic errors of design by the manufacturer.

### Tool Confidence Level (TCL)

Several use cases were defined for each Efinity® IDE tool. A software tool evaluation according to ISO 26262-8, clause 11 determined a required tool confidence level of TCL1 for all tools and use cases, without the need for software tool qualification. Individual tools or the complete tool chain can be used in the development of FPGAs with allocated safety requirements up to ASIL D.

Tool users must confirm the validity of the pre-determined TCL1 in their own design environment, and confirm that all tools are used per the defined use cases and that all conditions and assumptions of use (CoU and AoU) are fulfilled, as specified in the tool functional safety manuals. Otherwise, tool users must perform their own detailed software tool evaluation and possibly software tool qualification.

The following documents are a mandatory part of the certification:

### *exida* Assessment Report:

- EFI 22-07-092 R011 V1R1 61508 26262 Tool Assessment Report - Efinix IDE

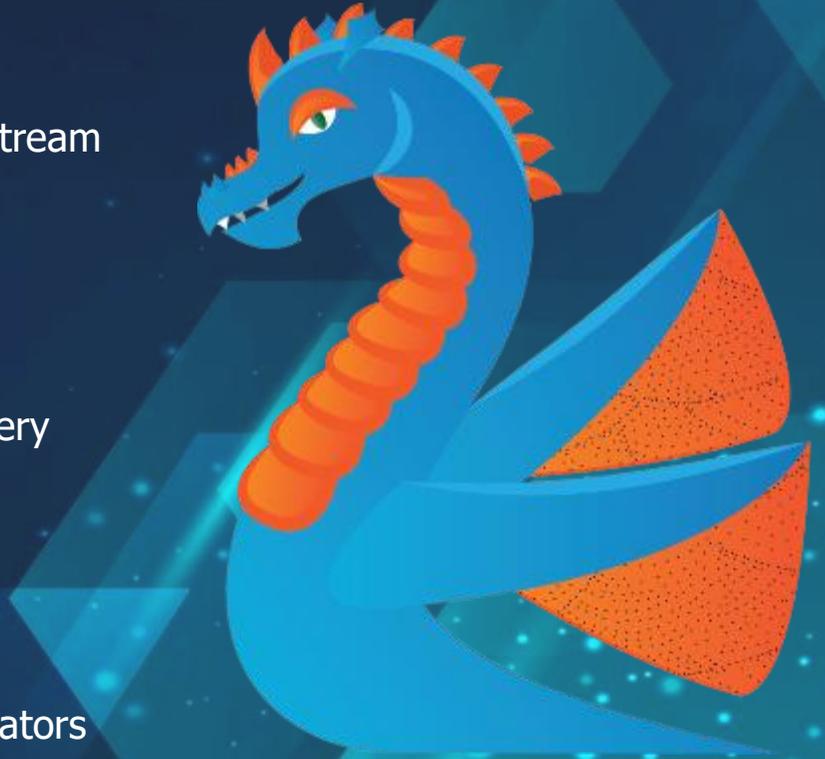
### Efinix Functional Safety Manuals:

- Efinity\_IDE Functional Safety Manual v3 or later
- Interface\_Designer Functional Safety Manual v2 or later
- IP\_Manager Functional Safety Manual v2 or later
- Code\_Editor Functional Safety Manual v2 or later
- Synthesis Functional Safety Manual v2 or later
- PhR Functional Safety Manual v2 or later
- Bitgen Functional Safety Manual v2 or later
- Programmer Functional Safety Manual v2 or later
- Timing\_Engine Functional Safety Manual v2 or later
- Debugger Functional Safety Manual v2 or later



# Efinity Features

- Project management to keep your design files organized
  - Support for Verilog HDL , System Verilog and VHDL languages (1993,2008,2019)
  - Graphical views of design hierarchy, result files, and reports
- VHDL LIBRARY support
- Easy to use dashboard to run through the flow (synthesis, placement, routing, bitstream generation) automatically or manually
- IP Manager to configure IP cores
- Support for Python scripting and command line tool flow
- Interface Designer to constrain logic and assign pins to blocks in the device periphery
- Floorplan Editor to browse through your design's logic and routing placement
- Timing Browser and static timing analysis to measure your design's performance
  - Tcl Command Console to perform timing analysis
- Supports simulation flows using the ModelSim, Aldec, NCSim, or free iVerilog simulators
- GUI and command-line Programmer
- Efinity Debugger with Virtual I/O and Logic Analyzer debug cores



# System Needs

Product	Model	Memory
Trion	T4, T8, T13, T20, T35	8 GB
	T55, T85, T120	16 GB
Titanium	Ti35, Ti60	8 GB
	Ti85, T190, Ti120, Ti135, Ti180, Ti165, Ti240, Ti375	16 GB
Topaz	Tz50	8 GB
	Tz110, Tz170	16 GB

- Minimum requirements
  - Computer with a 64 bit operating system, dual-core processor, and 8 GB RAM
- Linux environments
  - Operating system: Ubuntu x86-64 v18.04 or later, Red Hat Enterprise x86-64 v8.0 or later
  - Linux X11 windowing system (for Efinity® GUI)
  - Udev device manager for Efinix USB programming cable
  - Open-source Java 64-bit runtime environment; required for configuring the Sapphire RISC-V SoC in the IP Manager; available from: <https://developers.redhat.com/products/openjdk/download> (OpenJDK 8 or 11) – <http://jdk.java.net/16/> (OpenJDK 16)
- Windows environments
  - Windows 10 or later, 64 bit
  - Microsoft Visual C++ 2019 x64 runtime library (or latest version)
  - Open-source Java 64-bit runtime environment; required for configuring the Sapphire RISC-V SoC in the IP Manager; available from: – <https://www.java.com/en/download/manual.jsp> (Java 8)
- GTKwave 3.3.117



Thanks !