Unleashing >100G Performance:
High-Speed UDP/TCP Hardware Stacks for FPGAs by CAST

Calliope-Louisa Sotiropoulou, PhD
Sales Engineering Manager
FPGA Developers Conference 2025, CERN

www.cast-inc.com

About CAST

CAST
www.cast-inc.com

A successful, low-risk Silicon IP vendor

- ► One of the first IP vendors in the market
  - Founded in **1993**
- ► Quality standards and business practices refined and evolved over the three decades of our operation
- ► Dedicated to customer success
  - Have helped hundreds of customers ship billions of product units
- ► A global team with offices in the US and Europe and Sales/Support Partners in the Middle East and Asia
- ► IP Cores for different applications:
  - Communications
  - Data Centers
  - Automotive
  - Video, Image codecs
  - Data compression
  - Peripherals

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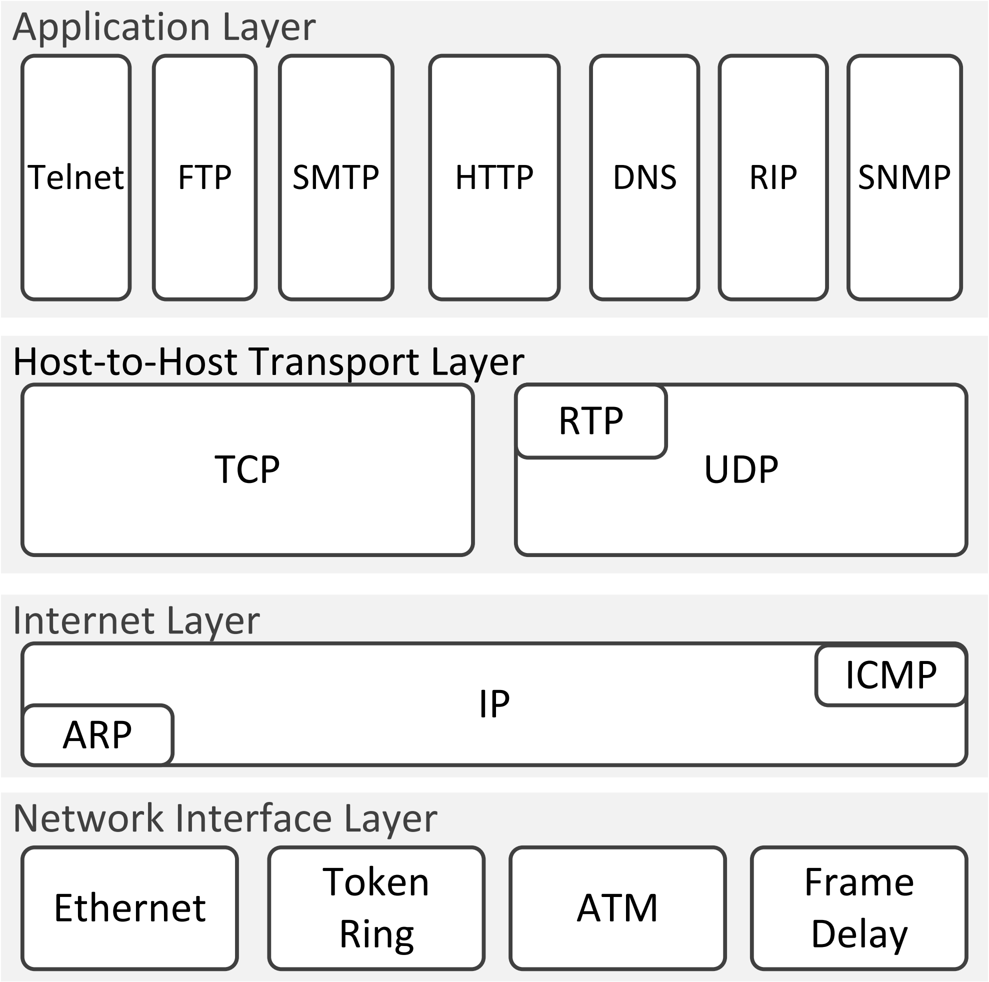
Introduction: UDP and TCP

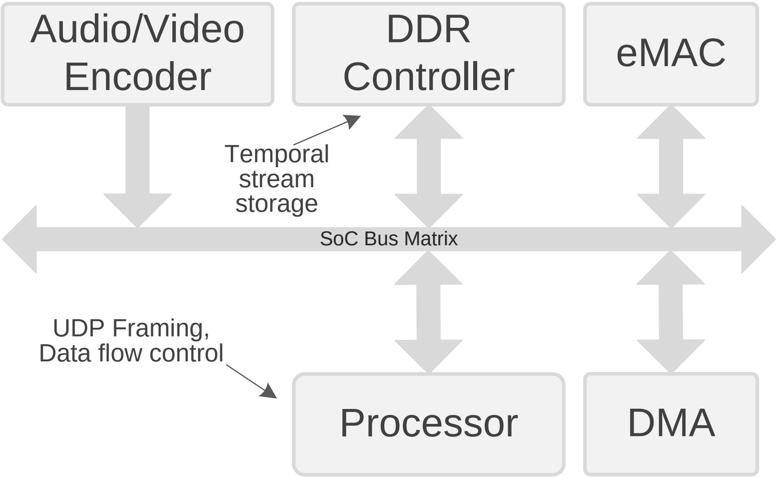


UDP	TCP
Connectionless No requirements for opening, maintaining, or terminating a connection	**Connection-Oriented** Data can be exchanged only after a connection has been established
Broadcasting-Capable	**No Broadcasting**
Best Effort – Unreliable No handshaking or retransmission	**Guaranteed Delivery - Reliable** Handshaking, retransmission
No Flow Control	**Flow Control**
Less Complex & Faster than TCP	**More Complex & Slower than UDP**
8 Bytes Header	**20 Bytes Header**
Used for Video & Audio streaming, VoIP, DNS, radar ...	Used for HTTP(S), FTP, POP, SMTP ...

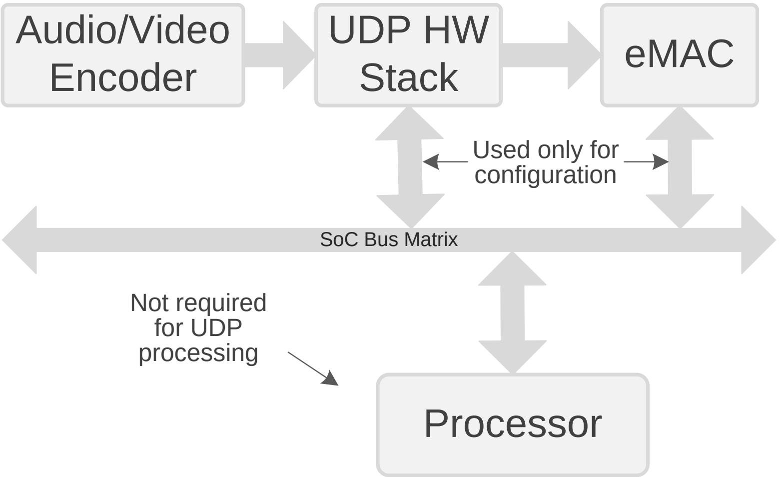
Why use a hardware stack?

UDP Application Example

- ▶ Without a HW Stack
  - Several GIPS on uP
  - Several million of accesses on the SoC bus and memory
  - Bus, memory, and processor arbitration is an issue



- ▶ With a HW Stack
  - Processor is no longer required for UDP/IP packet processing
  - Lower design complexity
  - Lower power

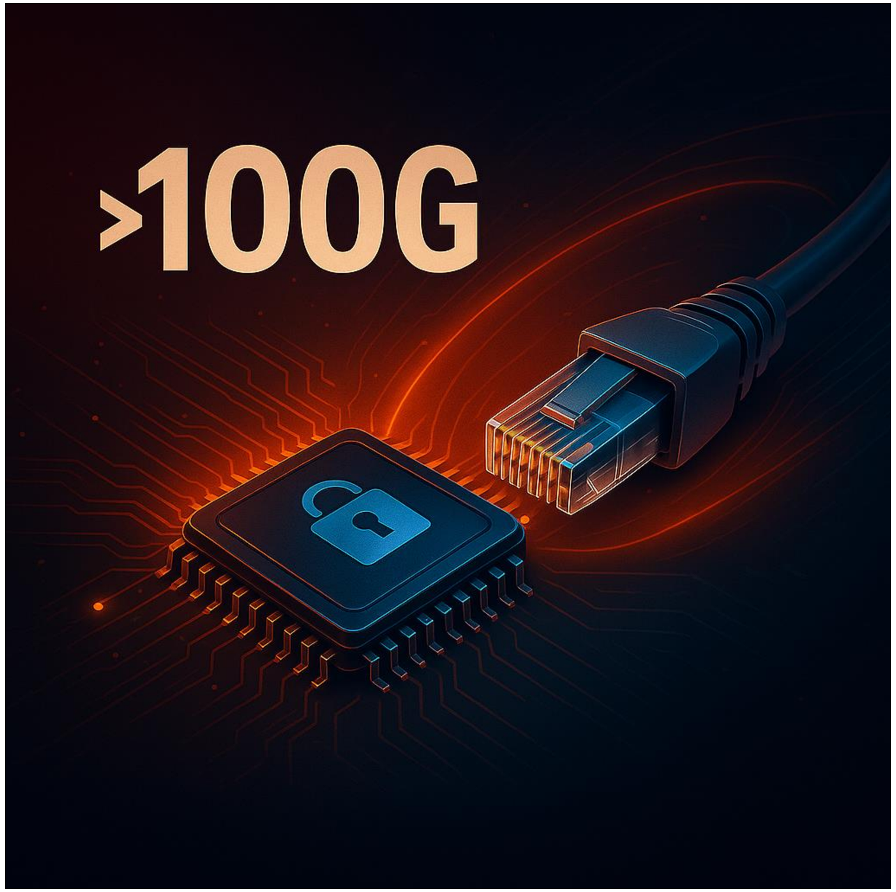


Why >100G HW Stacks?

- High-bandwidth demands in data acquisition, HPC, scientific computing, data centers

- Real-time requirements push beyond traditional software networking
  - Handling networking through software is no longer an option because it simply cannot keep up

- Hardware stacks:
  - Deterministic, scalable, efficient, offer predictable and stable data flow, critical for streaming and control systems



Performance at 100G and beyond…

- What are the key metrics that define the performance of a HW Stack?

  - Latency: Time it takes for data to travel through the stack from input to output
    - Lower latency = faster response and real-time behavior

  - Throughput: The amount of data the stack can process per unit time (e.g. Gbps)
    - High throughput = better utilization of link capacity, important for >100G systems

Performance at 100G and beyond…

- Traditional software stacks struggle at >100G due to OS overhead, memory copies, and unpredictable latencies

- The latency is SW can be as high as 50µsec or more

- HW Stacks (both UDP and TCP) enable predictable, line-rate networking

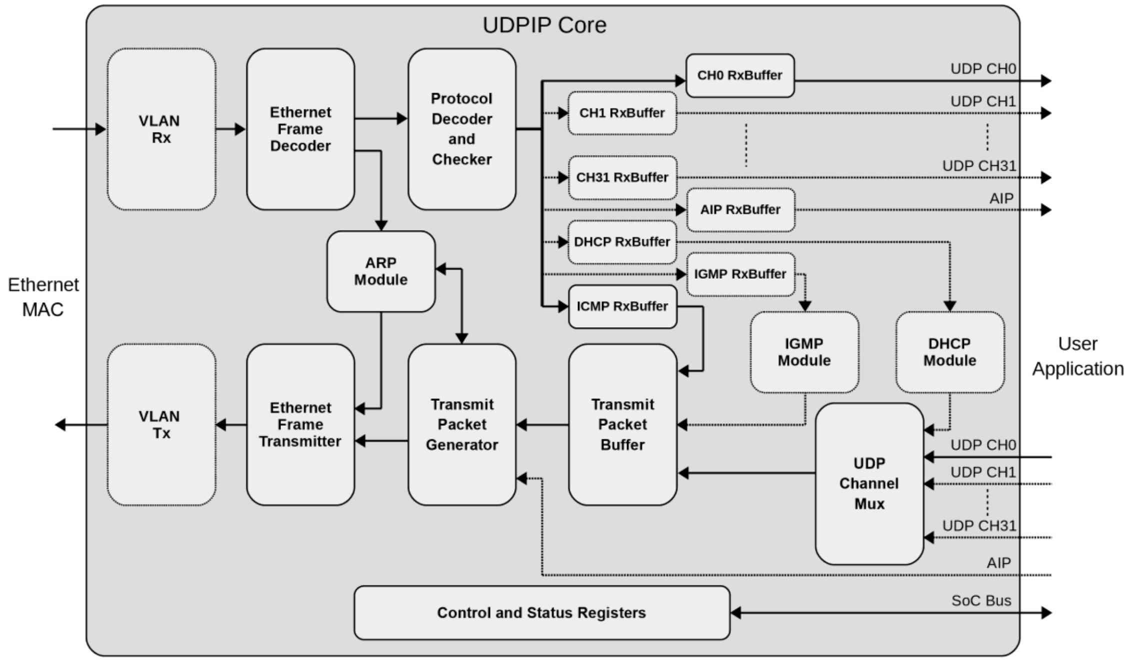
Hardware Stack Architecture

- Fully hardware-based (no embedded CPU or microcontroller) →100% RTL code

- Deep pipelining, internal parallelism – throughput increases by increasing the bus size and the clock speed

- Protocol acceleration: segmentation, checksum, reassembly

UDPIP 100G IP – Basic Characteristics

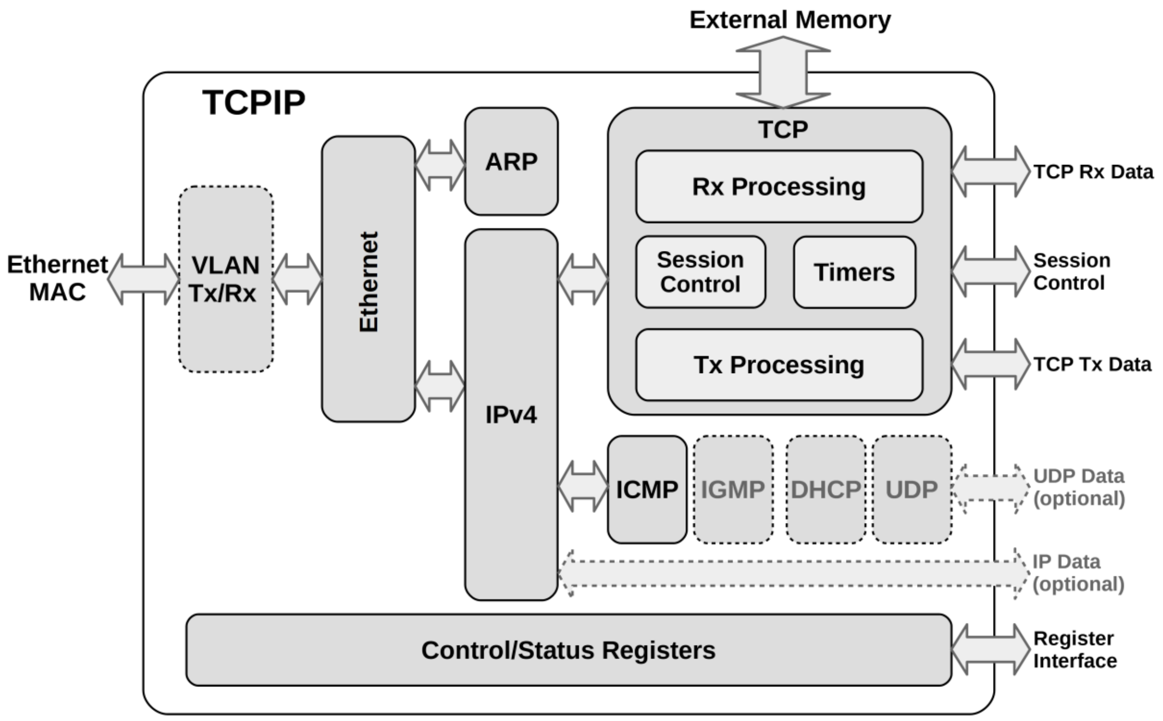


- ►Full protocol offloading
- ►Implements transport, internet, and link layers
- ►Up to 32 Tx Channels
- ►Up to 32 Rx Channels
- ►512bit bus
- ►Needs a clock of >250MHz
- ►Separate clock domains for data and control
- ►Jumbo frames up to 64kB

UDPIP 100G IP – Resources

- Basic Configuration required: Number of Rx/Tx channels and size of Rx/Tx buffers
- A basic configuration with **1Rx/1Tx** channels and **32kB** buffering is as small as **~10,000 LUTs** and **28 RAMB36**
- The same configuration with **16Rx/16Tx** channels and **32kB** buffering has a size of **~27,000 LUTs** and **133 RAMB36**
- It is important to note that the core doesn’t grow linearly with the number of channels

TCPIP 100G IP – Basic Characteristics



- ▶ Full protocol offloading
- ▶ Handles up to 32k sessions
- ▶ Simultaneous Client and Server support
- ▶ Port and IP address filtering for incoming connection requests
- ▶ Optional support of UDP

TCPIP 100G IP – Resources

- Basic Configuration required: Maximum number of sessions, max number of servers and ports

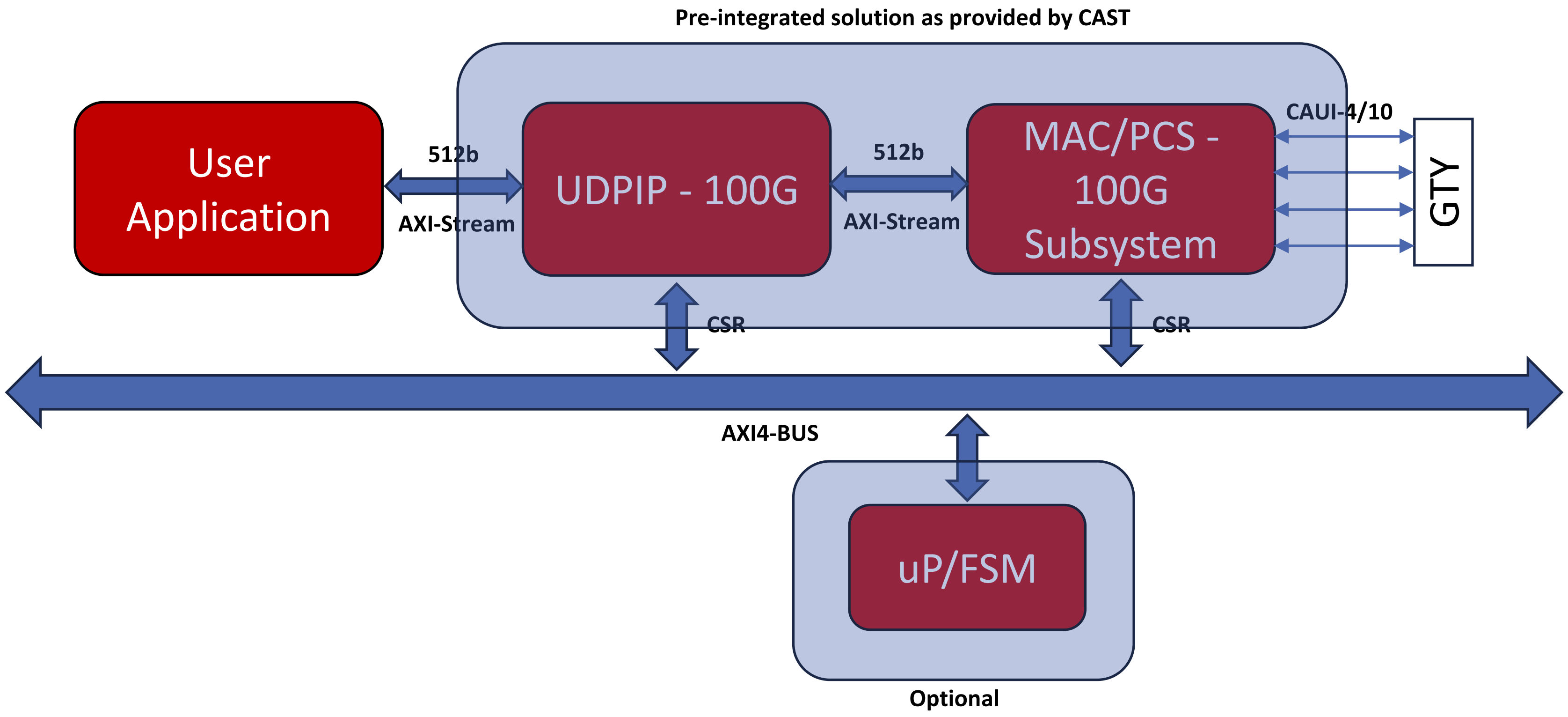
- A basic configuration with **16 sessions** and **8 servers** has a size **smaller than 50,000 LUTs** and **~20 RAMB36** (+ size of desired UDP configuration)

- A configuration with **16k sessions** and **8k servers** has a size of **~50,000 LUTs** and **~980 RAMB36** (+ size of desired UDP configuration)

- The number of sessions and servers has a small impact on the logic size but significant impact on the required memory

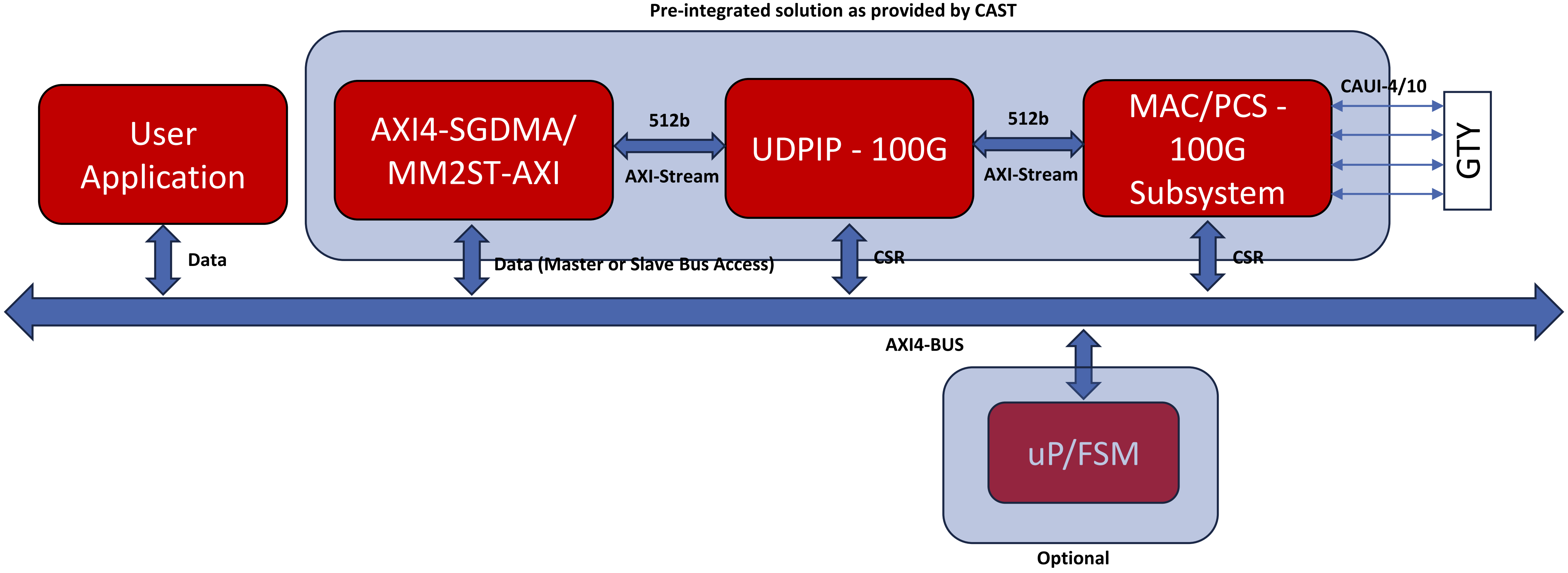
Integration into FPGA Design

- ▶AMD Ultrascale+ UDPIP-100G Example:



Integration into FPGA Design

► AMD Ultrascale+ UDPIP-100G Example:



Processing Latency

- It can be structured based on the layer of the protocol:

  - MAC layer latency – the Ethernet MAC IP core processing latency for the ethernet frame receive and transmit directions. The latency is MAC vendor dependent and needs to be checked in the MAC user’s guide.

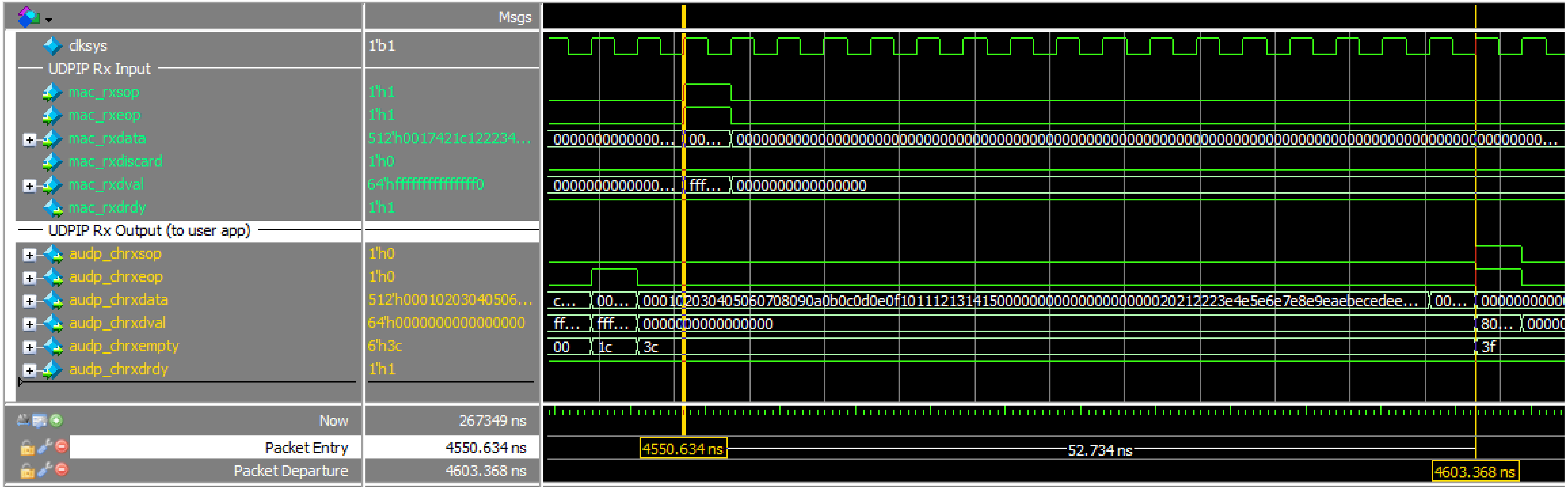
  - UDP/IP latency – the latency of the UDPIP core introduced while processing the received packets (Rx Latency) and generating transmit packets from the data sent by the user application (Tx Latency)

  - ARP Latency – this latency comes in play in case the network device needs to resolve an unknown MAC address for the destination IP address

UDPIP-100G Rx Latency

- ►Measured at the MAC boundary and UDP Rx channel output to the user application
  - The UDPIP core stores and checks the UDP packet for errors before the data is sent to the user application (store-and-forward)
- ►It is the time between the End-of-packet received from MAC until the moment the Start-of-packet is passed to the user application
  - The measurement must be done without any affects from the user application data backpressure (ready signal)
- ►The latency of the UDPIP Rx datapath is 17 clksys cycles. For a system clock at 322.265625MHz, the latency is 52.734ns

UDPIP-100G Rx Latency

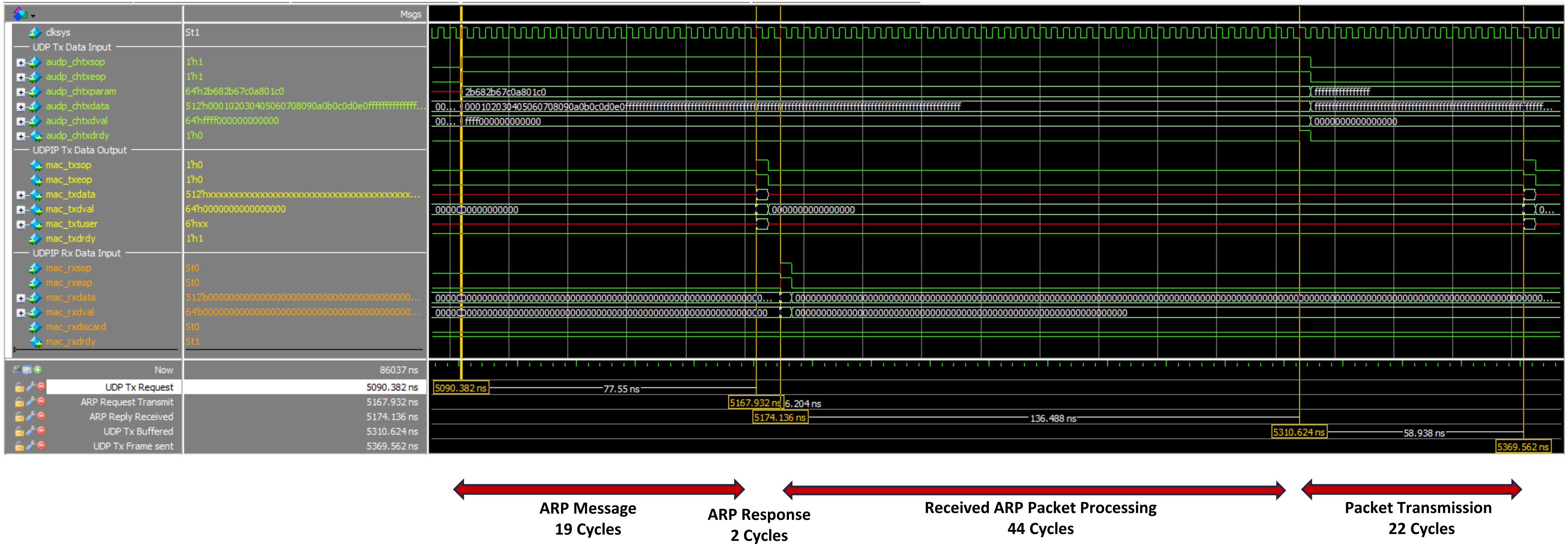


UDPIP-100G Tx Latency with ARP Delay

The Tx latency is affected by:

- ARP protocol - the presence of the target IP address in ARP cache greatly reduces the transmit latency
  - In case the IP address is not in the cache the core must perform the ARP packet transmission and receiving before it can proceed with the UDP packet forming and transmission
- UDP payload size - the core buffers the full data payload due to the checksum computation and only then the core can proceed with the UDP packet transmission
- Channel arbitration - the packet transmission is arbitered by round-robin arbiter. In case there are more channels transmitting data at the same time then the channel latency may increase by waiting for a finished transmission at a different channel.

UDPIP-100G Tx Latency with ARP Delay



Hardware Stacks from CAST

Complete, efficient, easy to integrate for ASIC and FPGA

	VLAN	IPv4	ICMP	ARP	DHCP	IGMP	UDP	TCP	UDP Sockets	TCP Sessions	Speed (Gbps)	Availability
UDPIP-1G	✓	✓	✓	✓	✓	✓	✓	✗	Unlimited	N/A	1	Now
UDPIP-10G/25G	✓	✓	✓	✓	✓	✓	✓	✗	Unlimited	N/A	10/25	Now
UDPIP-40G/50G	✓	✓	✓	✓	✓	✓	✓	✗	Unlimited	N/A	40/50	Now
UDPIP-100G	✓	✓	✓	✓	✓	✓	✓	✗	Unlimited	N/A	100	Now
TCPIP-1G/10G	✓	✓	✓	✓	✓	✓	✓	✓	Unlimited	32k	1/10	Now
TCPIP-25/40/50G	✓	✓	✓	✓	✓	✓	✓	✓	Unlimited	32k	25/40/50	Coming soon
TCPIP-100G	✓	✓	✓	✓	✓	✓	✓	✓	Unlimited	32k	100	Coming soon

Conclusions

- >100G Networking Requires Hardware Solutions: Software stacks are no longer sufficient for modern data rate and latency demands.

- HW Stacks Deliver Deterministic Performance: Fully hardware-based UDP and TCP/IP cores offer low-latency, high-throughput communication ideal for scientific, industrial, and data center applications.

- Efficient Resource Utilization: Scalable architectures provide flexibility from minimal to highly parallel configurations without linear resource growth.

- CAST HW Stacks: Ready for Real-World Deployment: Seamless integration into FPGA designs, production proven UDP and TCPIP solutions

Thank you!

Contact CAST:
info@cast-inc.com
sales@cast-inc.com

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