

# 2nd FPGA Developers' Forum (FDF) meeting



**Tuesday 20 May 2025 - Friday 23 May 2025**

**CERN**

## **Scientific Programme**

## **Sharable HDL cores**

HDL modules that are shared under any licence to be used in any FPGA design.

## **Algorithm implementation in HDL and HLS**

Implementations of algorithms both in HDL or HLS.

For example: peak finding, clustering, neural networks, boosted decision trees, transforms, etc.

## **Solutions to everyday digital design problems**

Have you encountered some common problem, and you solved it in a way that you would like to share?

For example: fast memory access, multiple transceiver configuration, clock domain crossing methods, super logic region crossing, NoC, etc.

## **HDL development tools**

Tools to help HDL development that are shared under any licence.

For example: code management on version control systems, continuous integration, register mapping, package generations, etc.

## **HDL verification and simulation tools**

Tools to help HDL verification or simulation, that are shared under any licence.