Session Program

20–23 May 2025

2nd FPGA Developers' Forum (FDF) meeting

Sharable HDL cores

CERN, 500/1-001 - Main Auditorium

Tuesday 20 May

15:40

Sharable HDL cores

Session | **Location:** CERN, 500/1-001 - Main Auditorium

15:40–16:15 **Open Logic – open-source FPGA Standard Library**

Speaker
Oliver Bründler

16:15–16:45 **TBD**

Speaker
Calliope-Louisa Sotiropoulou

16:45–17:10

The PandABlocks framework for flexible run-time configuration of Zynq SoCs

Speaker
Glenn Christian

17:10–17:40

NDK: An open-source framework for high-speed network applications on FPGAs

Speakers
Daniel Kondys, Radek Iša

17:40–18:10

Error-Redundant Implementation of Commercial IP Cores: A Practical Example

Speaker
Mr Philipp Jacobsohn

18:10