Session Program

20–23 May 2025

2nd FPGA Developers' Forum (FDF) meeting

Algorithm Implementation

CERN, 500/1-001 - Main Auditorium

Wednesday 21 May

09:00

Algorithm Implementation: 1

Session | **Location:** CERN, 500/1-001 - Main Auditorium

09:00–09:30

Exploring Linearity and Temperature Stability in Time-to-Digital Converters

Speaker
Gian-Luca Brazerol

09:30–09:50

Implementation of Time to Digital Converter on FPGA for high-resolution-performance in Particle Therapy applications

Speaker
Mr ARASH AMINI BARDPAREH

09:50–10:20

A low latency Gated Recurrent Unit Implementation for the AMD Versal AI Engine

Speaker
Michail Sapkas

10:20–10:50 **TBD**

10:50

11:20

Algorithm Implementation: 2

Session | **Location:** CERN, 500/1-001 - Main Auditorium

11:20–11:50 **Distributed Arithmetic for Real-time Neural Networks on FPGAs**

Speaker
Chang Sun

11:50–12:20

Chisel4ml: Generating Fast Implementations of Deeply Quantized Neural Networks using Chisel Generators

Speaker
Jure Vreča

12:20–12:50 **A Reconfigurable FPGA-Based ML Library for Kernel Methods**

Speaker
Yousef Alnaser

12:50

14:00

Algorithm Implementation: 3

Session | **Location:** CERN, 500/1-001 - Main Auditorium

14:00–14:20

Accelerating Transformer Neural Networks on FPGAs for High Energy Physics Experiments

Speaker
Filip Wojcicki

14:20–14:40

FPGA Implementation of Next-Generation Reservoir Computing for predicting dynamical systems

Speaker
João Folhadela

14:40