

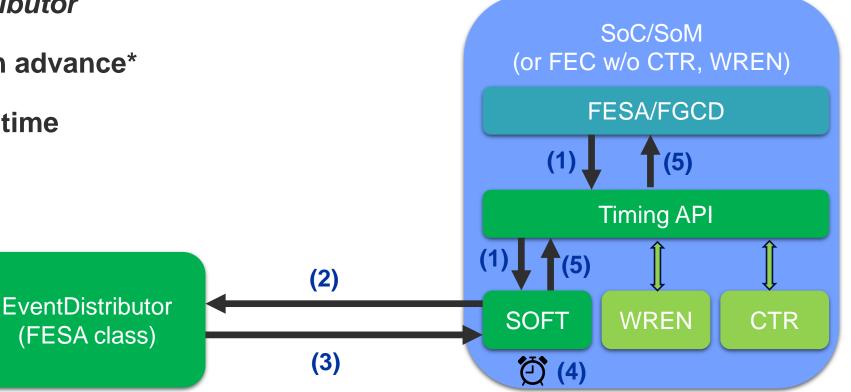
Timing on SoC/SoM, without CTR

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Timing on SoC, without a CTR/WREN

- **1. FESA subscribes to a Central Timing event**
- 2. Subscribe to EventDistributor
- 3. Notify about the event in advance*
- 4. Wait until the event due time
- 5. Trigger the event



*) Not possible for all events, see next slide



Timing on SoC: Asynchronous Events

• Scheduled events can be sent in advance

- LIC (LEI, PSB, CPS, SPS) cycles are scheduled 2-3 sec in advance
 - All regular events can be sent out ~1 sec in advance
- LHC uses event tables, mostly started by Java applications (typically sequencer)
 - Can send the events immediately but with postponed due time (to be seen if by 1 sec or less)

Asynchronous events can't be sent in advance

- Triggered by TTL pulses:
 - SPS: SX.AWK-10HZ-CT, SX.AWK-1HZ-CT, AWAKE Ej (SEX.F-W180-CT, ...), SX.BIS-OPEN-CT
 - LHC: HX.DUMPED1-CT, HX.DUMPED2-CT, HX.PM1-CT, HX.BINST1-CT, HX.BINST2-CT
- Safe Machine Parameter (SMP) messages, distributed at 10Hz
 - Beam energy, intensity, safe machine flags, beta*, ...
- Asynchronous events would still work but with the interrupt some milliseconds after event due time
 - With a noticeable jitter (publication by FESA, CMW transmission over TN, reception)



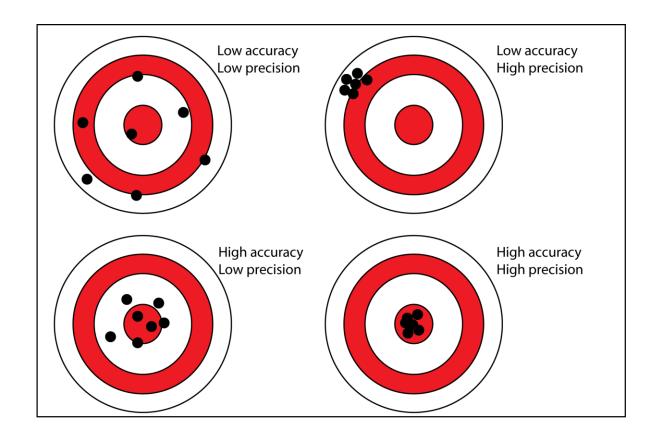
Timing on SoC: LTIM?

- LTIM == Local Timing
 - Local triggers (pulses, interrupts) generated on the FEC by the timing receiver module
 - Typically, Central Timing event (CTIM) + delay [clock ticks]
 - But supports more advanced scenarios e.g. started or stopped by external signals (TTL)
 - Clock: 1KHz, 1MHz, 10MHz, 40MHz, 1GHz, LTIM, ext. TTL pulses (e.g. RF bunch or revolution)
 - Single triggers, trigger trains
- Without the receiver module, a VERY simplified version (subset of functionality)
 - Clock: 1KHz, 1MHz
 - Single interrupts, interrupt trains (N interrupts equally spaced in time)
 - CTIM + delay [ms/us]



Timing on SoC: Accuracy and Precision

- Accuracy (as good as on the OS):
 - NTP: sub-millisecond
 - PTP: sub-microsecond
 - To be measured
- Precision:
 - Plan A: system call (clock_nanosleep)
 - Expecting between tens and hundreds of microseconds
 - Plan B (if need be): dedicated kernel module
 - To be measured







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