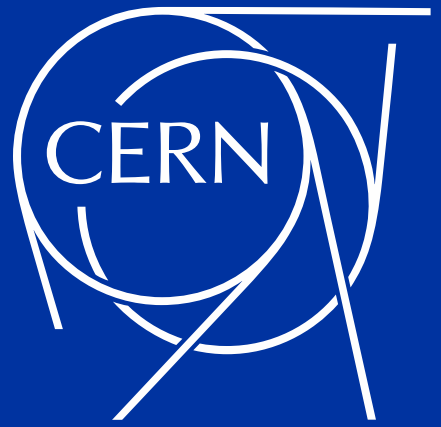


ATS SoC Framework Project
ECF #14: SoC/SoM projects and timing

Irene Degl'Innocenti, Manoel Barros Marin

31/10/2024

Introduction to ATS SoC Framework Project

- **Development of a System-on-Chip framework to simplify access to the technology, reduce redundant developments, standardise integration in the accelerator controls.**
  - Target: ATS projects using Zynq UltraScale+ MPSoC with deployment in LS3 (BI, EPC, ABT, CEM)
  - Simplify development: SoC Base project and platform management solutions
  - Standardise integration of stand-alone SoCs: FEC-like model
  - EDMS: Project Mandate
- **Based on the Project Proposal of the CTTB ATS SoC Taskforce**
  - Survey on SoC applications in the sector
  - Intermediate reporting at 34th CTTB (24/11/2023): indico
  - Final reporting at 37th CTTB (23/02/2024): indico
  - Project proposal document available on EDMS on 31/05/2024
  - Documentation: ATS SoC Framework Wiki

Timing on SoC: from the survey

Machine timing:

- Required for FESA on SoC (FEC-like model)
- SW Applications do not require full WR capabilities: light implementation?
- Real-time actions in programmable logic
  - TTL inputs, Beam Synchronous Timing (BST)

UTC Timing:

- Required on the Processing System of the SoC for Linux;
- NTP precision for most SoC applications, no generic development foreseen for the SoC project
- Exception: FGC4 (EPC) requiring PTP precision (see Adrian's and Valerio's presentation)
  - Their development to be followed up by the project

SoC Project status: workunit and milestone plan definition

- Milestone plan
- Resources requests
- Coordination
- Keeping stakeholders informed

- Test procedures
- Beta version delivery
- Final version delivery
- Maintenance proposal
- Documentation

Workunits

- **WU1 – SoC Base Project**
- **WU2 – SoC platform management**
- **WU3 – FESA and timing**
- **WU4 – OS and sysadmin**

- Holder: Alen Arias Vazquez (CEM)
- Synergy with **DI/OT project**
- Build scripts, diagnostics libraries, etc.

Workunits

- **WU1 – SoC Base Project**
- **WU2 – SoC platform management**
- **WU3 – FESA and timing**
- **WU4 – OS and sysadmin**

- Holder: Steen Jensen (BI)
- Remote console and reset, IP repository, EDGE

Workunits

- **WU1 – SoC Base Project**
- **WU2 – SoC platform management**
- **WU3 – FESA and timing**
- **WU4 – OS and sysadmin**

- Holder: Greg Kruk (CSS)
- FESA on SoC
  - CMW integration
  - **Timing class** (see Greg's presentation)

Workunits

- **WU1 – SoC Base Project**
- **WU2 – SoC platform management**
- **WU3 – FESA and timing**
- **WU4 – OS and sysadmin**

- Holder: Ioan Kozsar (CEM)
- Linux distribution image (FECOS), booting

SoM Project

SoM Project Mandate

- The ATS SoM Project is mandated by the CTSB to **deliver a System on Module** (SoM) part suitable for use by the majority of stakeholders within the ATS *(full synergy with SoC project!).*
- The SoM will be an **Open Hardware development** following the specification established by the CTTB SoM Taskforce.
- The SoM project is complete once **pre-series quantities of the SoM are delivered** and validated at CERN and responsibility for maintenance has been taken over. This is foreseen to be achieved in 2026.

ATS SoM Project Mandate: https://edms.cern.ch/document/3156343
CTTB SoM Taskforce specifications: https://edms.cern.ch/document/3156345
Detailed information: Update on the CERN ATS System-on-Module

Status

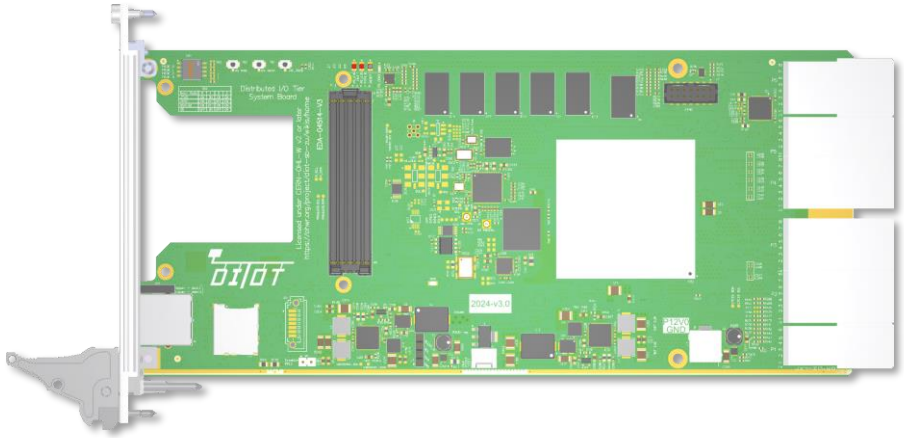
- ATS Technical Specification by SoM Taskforce in circulation for Approval (EDMS 3156345)
- Contract Technical Specification has been Released (EDMS 3157099)
- Department Request is Approved (DRQ 10494653) for Proto and Pre-series
- Call for tender already launched

Contact

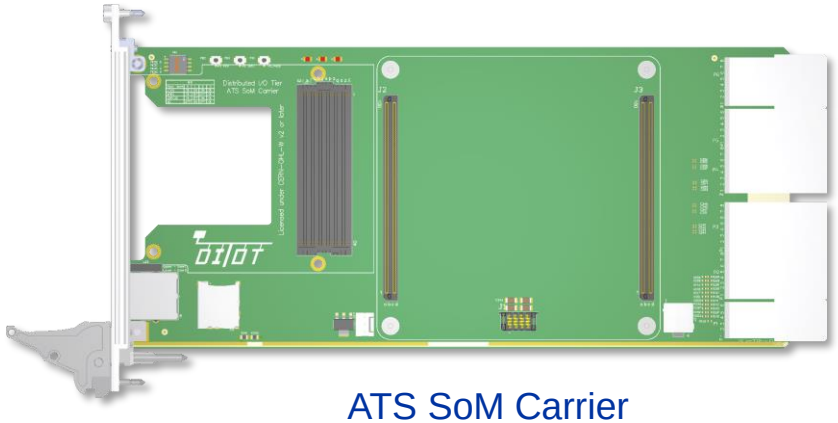
- Project Leader: David Nisbet (David.Nisbet@cern.ch)
- Technical Coordinator: Manoel Barros Marin (manoel.barros.marin@cern.ch)

SoM Project

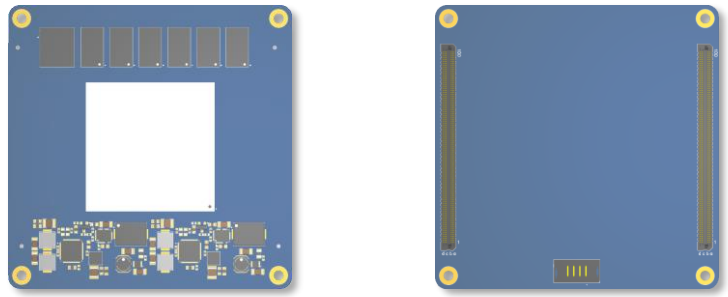
Compatibility with DI/OT



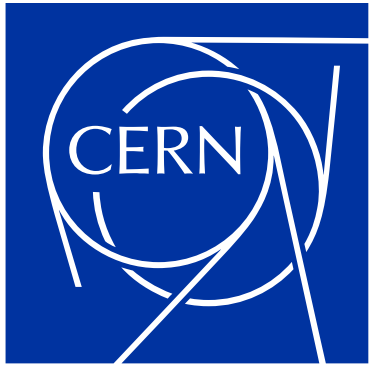
DI/OT System Board v3 (EDA-04514-V3)



ATS SoM Carrier



ATS SoM



SoC Framework Project: EDMS
Read about: ATS SoC Wiki

home.cern

Project mandate

Mandate:

The ATS System-on-Chip (SoC) Framework project is mandated by the CTSB to deliver a framework composed of project examples and references, libraries, tools and standardised solutions to integrate SoCs in the accelerator control system.

The project is established through the CTTB, based on the current and foreseen SoC applications in ATS and the future needs.

The SoC Framework project will be complete once the whole framework is delivered and validated and the responsibility for maintenance has been taken over. This is foreseen to be achieved by mid 2026.

Project mandate

The project is responsible for:

- Defining the milestone plan;
- Defining appropriate workunits, workunit holders, participants, and their deliverables;
- Defining and requesting suitable resources (budget and workforce) from groups throughout the ATS sector;
- Keeping all stakeholders informed;
- Coordinating the parallel developments across the groups involved;
- Delivering the various parts of the framework and granting the users the possibility to test and integrate them in their systems in time for their reliable commissioning;
- Ensuring the final SoC framework can be smoothly transferred to a long-term support.

Project mandate

Deliverables:

- Milestone plan, project structure including workunit definition;
- Workunit holders and workunit resources;

STATUS

- Long-term maintenance and long-term support plan;
- Delivery of beta-versions and operational versions of the various components in line with the detailed schedule outlined in the project milestone plan;
- Procedures for early-stage testing and trouble-shooting as the individual components are developed;
- Delivery of the whole framework by Q2 2026;
- Delivery of documentation for all components.

Reporting:

- The project will report regularly to the CTTB and may periodically report to the CTSB.

No.	Milestone
1	DI/OT build system for HDL and SW improved and generalised.
2	Reference hardware design extracted from the DI/OT System Board
3	Proposal and development of remote power cycle and console
4	Timing Front-End library for reception of events via CMW/RDA
5	Provide distribution image for DI/OT
6	Validate FECOS boot sequence for DI/OT
7	Booting with fail-safe image
8	Adoption of application-specific device tree overlays or alternative
9	Beta version of the FESA framework
10	Debian packages for GW/SW updates
10a	Extend Controls Configuration Service (CCS) to integrate SoCs
11	DI/OT library plug-ins for custom sensors and diagnostic parameters
12	Integration with COSMOS
13	Common IP repository set up
14	PTP support on SoC
15	Pro version of FESA framework and dependencies validated (full integration tests) for SoC
16	Proposal and development of tools/methods for SoC operational troubleshooting
17	Remote logging for DI/OT
18	Timing Front-End library and FESA supporting SoC LTIMs
19	Integration with remote CSS access tools
20	Provide distribution image for “hosted” SoCs
21	Validate FECOS boot sequence for “hosted” SoCs
22	Application of SoC framework to “hosted” SoCs
23	Scaling remote logging for “hosted” SoCs
24	EDGE driver for memory map and IRQ proof of concept
25	Integration of Post Mortem libraries