



ÖAW



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RD50 HV-CMOS Meeting

DESY Test Beam Oct. 2024

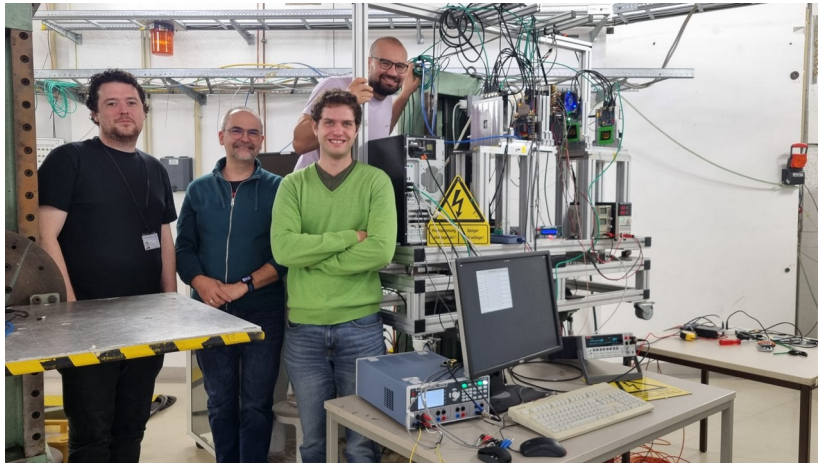
First results

Bernhard Pils



Setup

- Telescope: 6 *Adenium* planes
- Telepix2 as ROI trigger
 - Input to TLU
- Operated with 4.2 GeV electrons
- Improved cooling setup (Thanks to Sam and Christian!) able to go down to $\sim -15^{\circ}\text{C}$
 - Operated all samples at this temperature
- Samples in luggage:
 - Non-Irradiated W8 (W8-0E0)
 - W3-1E14
 - W3-3E14
 - W8-1E15
 - W3-1E16



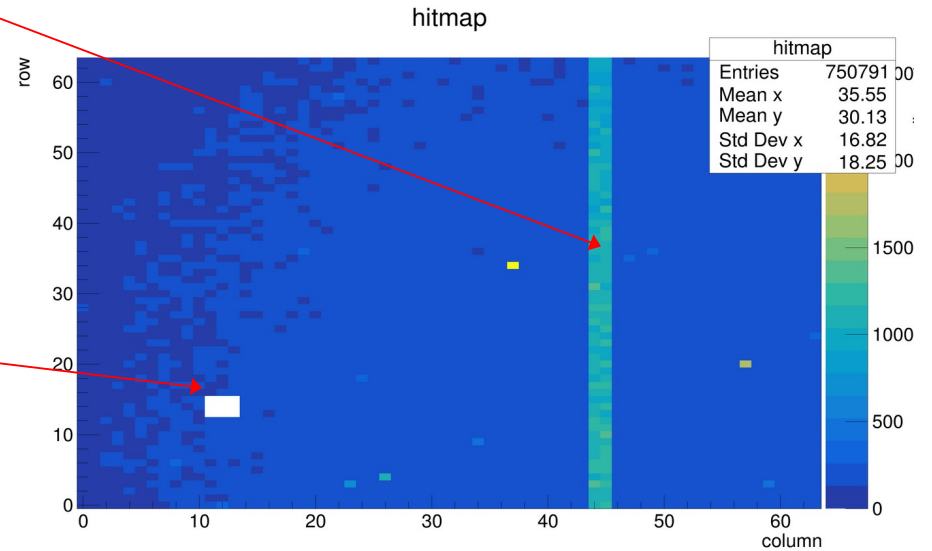
What got measured?

- Each sample measured with „standard“ settings
 - $V_{\text{Bias}} = 190\text{V}$
 - $V_{\text{Thr}} = 1.1\text{V}$
- Best settings
 - Minimized threshold (as low as possible without noise)
 - Maximized Bias voltage
- Bias Voltage Scans (at safe threshold)
 - Going from 0V → 500V in 10V steps
- **All done for both biasing schemes (backside and topside)**

Analysis is not done yet!
You are about to see **very preliminary** plots
This is a first glance, do not present elsewhere

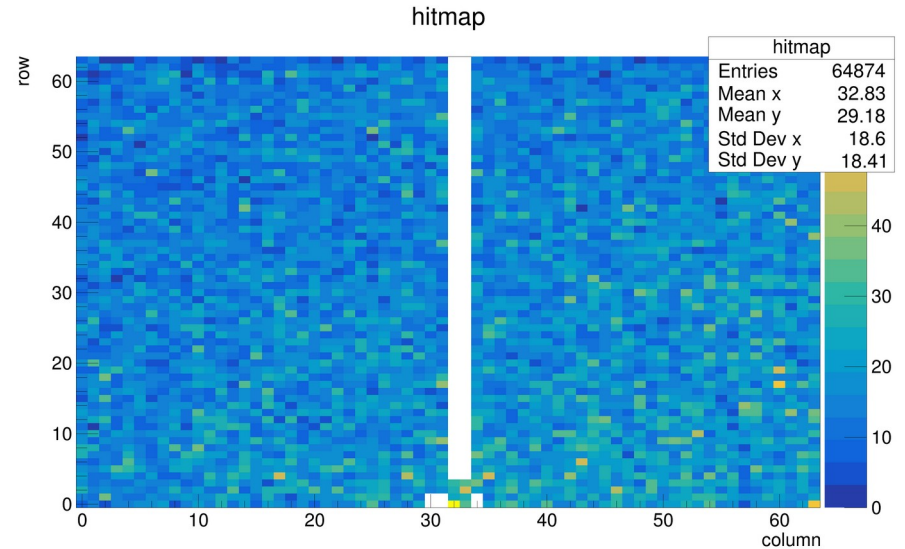
General problems 3E14

- One „damaged“ double column (columns #44 + #45 → double column #22)
- 1 noisy pixel
 - Masked during data taking



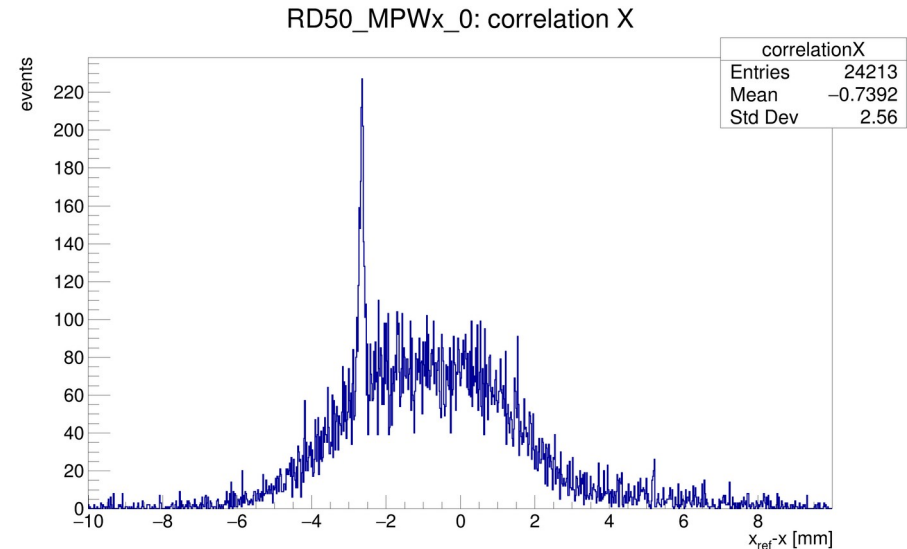
General problems 1E15

- 1 dead double column (#16)
 - Reason for (upcoming) masking
- TS-overflow not counting → had to use TLU timestamp → No proper timing analysis possible
- Died at $V_{\text{Bias}} = 600\text{V}$ at the testbeam



General problems 1E16

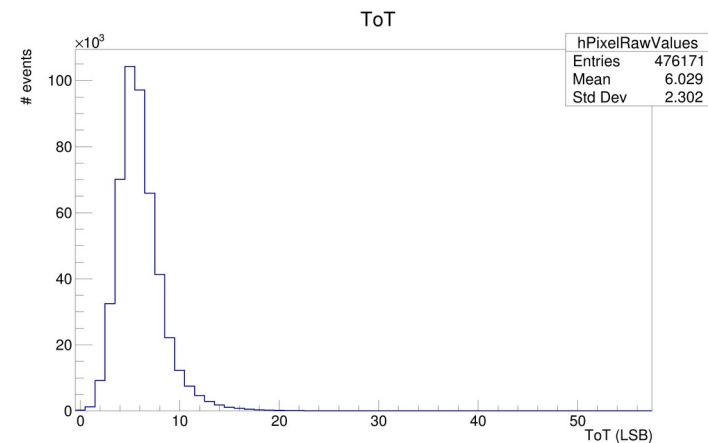
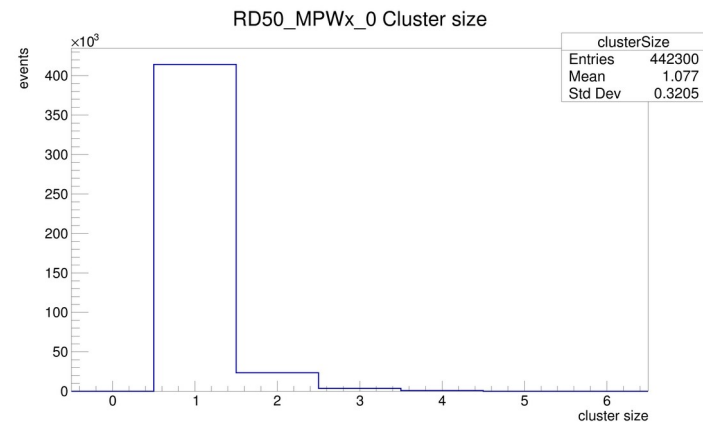
- Is talking to I2C and delivering data (a little bit)
- Increased noise
- Correlations observed
- Track based characterization difficult (not managed to so far)



Standard Settings (1)

Coloring: Biasing Topside Backside

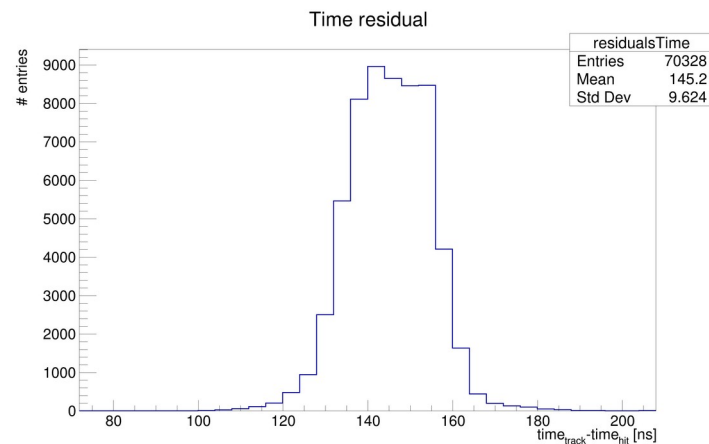
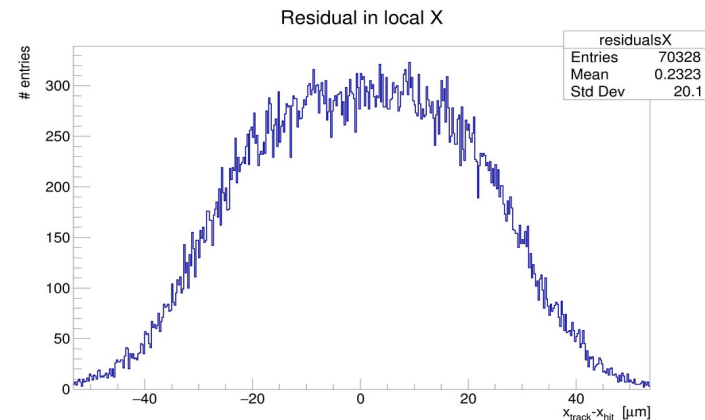
DUT	ClusterSize	ToT	
W8-0E0	1.07	6.02	Fishy
W3-1E14	1.15	13.62	
W3-1E14	1.16	13.78	
W3-3E14	1.12	4.99	
W3-3E14	1.12	4.97	
W8-1E15	1.04	2.09	
W3-1E16	1.36	73.68	



Standard Settings (2)

Coloring: Biasing **Topside** Backside

DUT	σ X-Residuals [μm]	σ T-Residuals [ns]
W8-0E0	20.51	11.05
W3-1E14	20.79	10.04
W3-1E14	TODO	
W3-3E14	19.14	11.23
W3-3E14	19.2	10.68
W8-1E15	21.51	-
W3-1E16	-	-



Standard Settings (3)

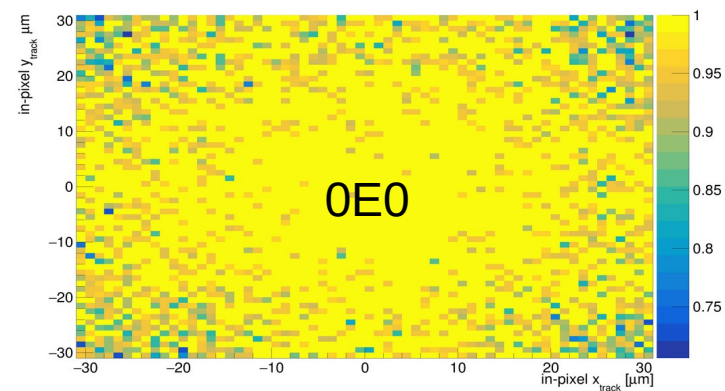
Coloring: Biasing

Topside

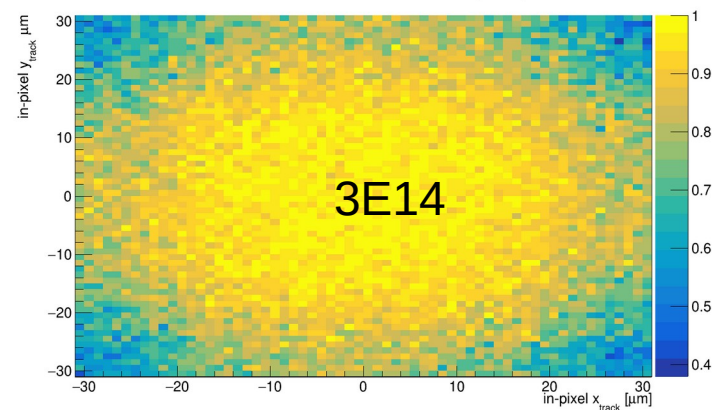
Backside

DUT	Efficiency [%]	
W8-0E0	97.5%	Fishy
W3-1E14	99.5%	
W3-1E14	TODO	
W3-3E14	84.7%	
W3-3E14	85.5%	
W8-1E15	8.9%	
W3-1E16	-	

RD50_MPWx_0 Pixel efficiency map



RD50_MPWx_0 Pixel efficiency map



Minimizing thresholds

DUT	V_{Thr}	V_{Bias}	Efficiency	Comment
0E0	960mV	190V	99.9%	Lower V_{Thr} at higher V_{Bias} done in April
1E14	1.02V	190V	99.8%	
3E14	950mV	190V	97.9%	No masking of hurt double column
1E15	970mV	190V	51.3%	No masking of broken double column, we'll see HV is key anyways
1E16	1.05V	300V	-	You already know the problem

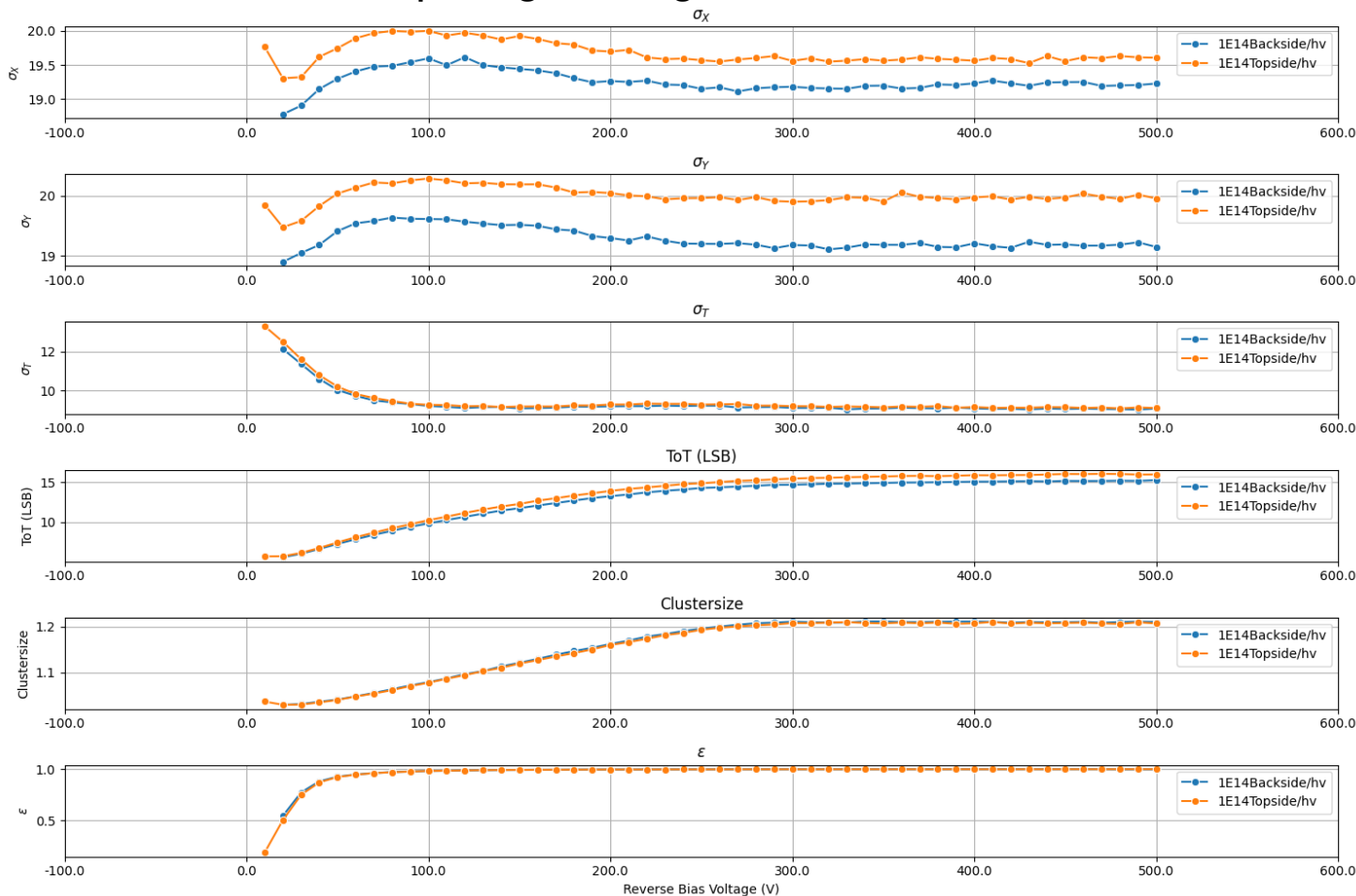
- Minimum thresholds were not always usable for higher bias voltages
- Higher leakage current → higher noise

Comparing biasing schemes 1E14

Differences
observed

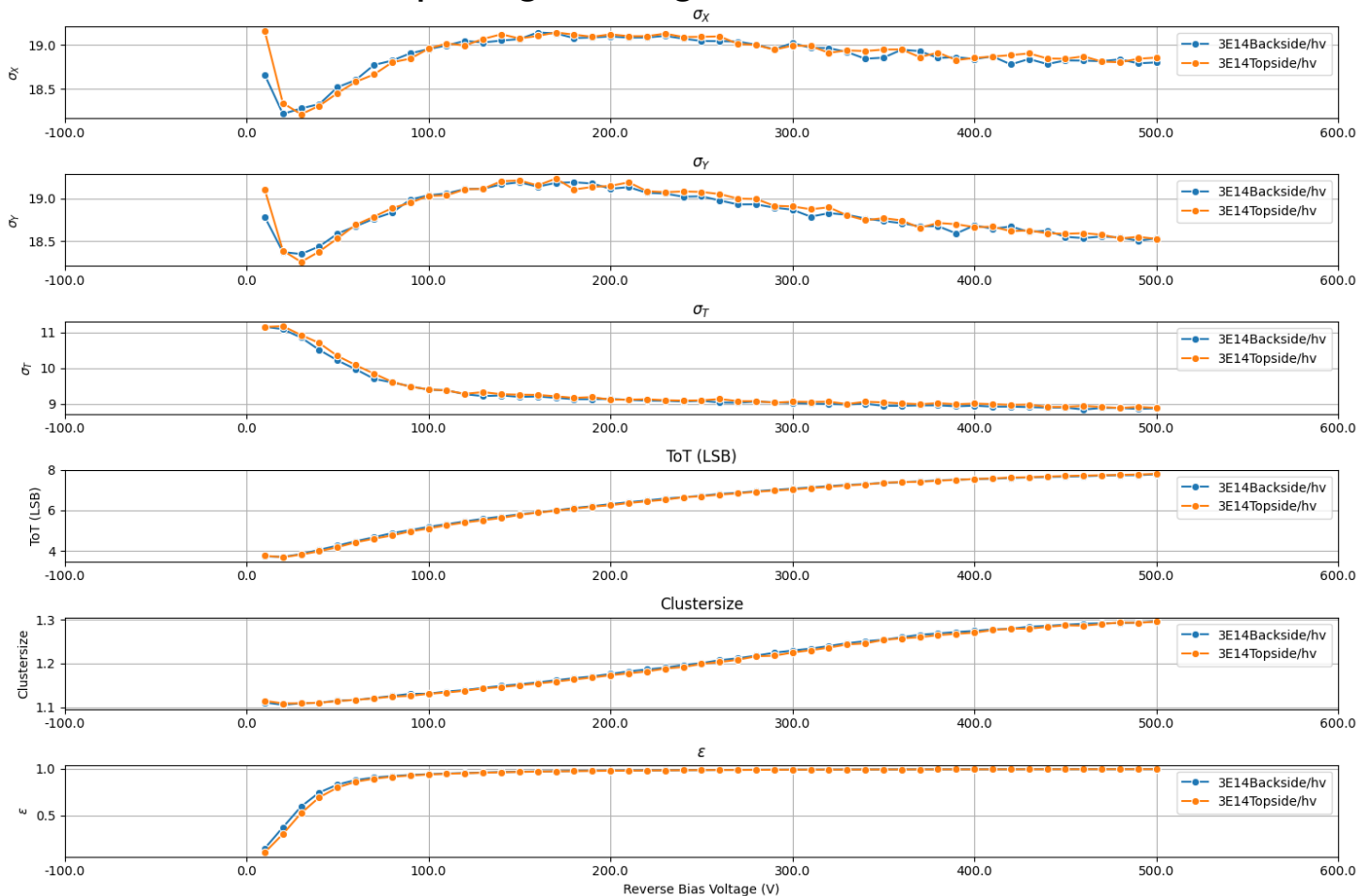
Reason
unclear (atm)

No noteworthy differences encountered

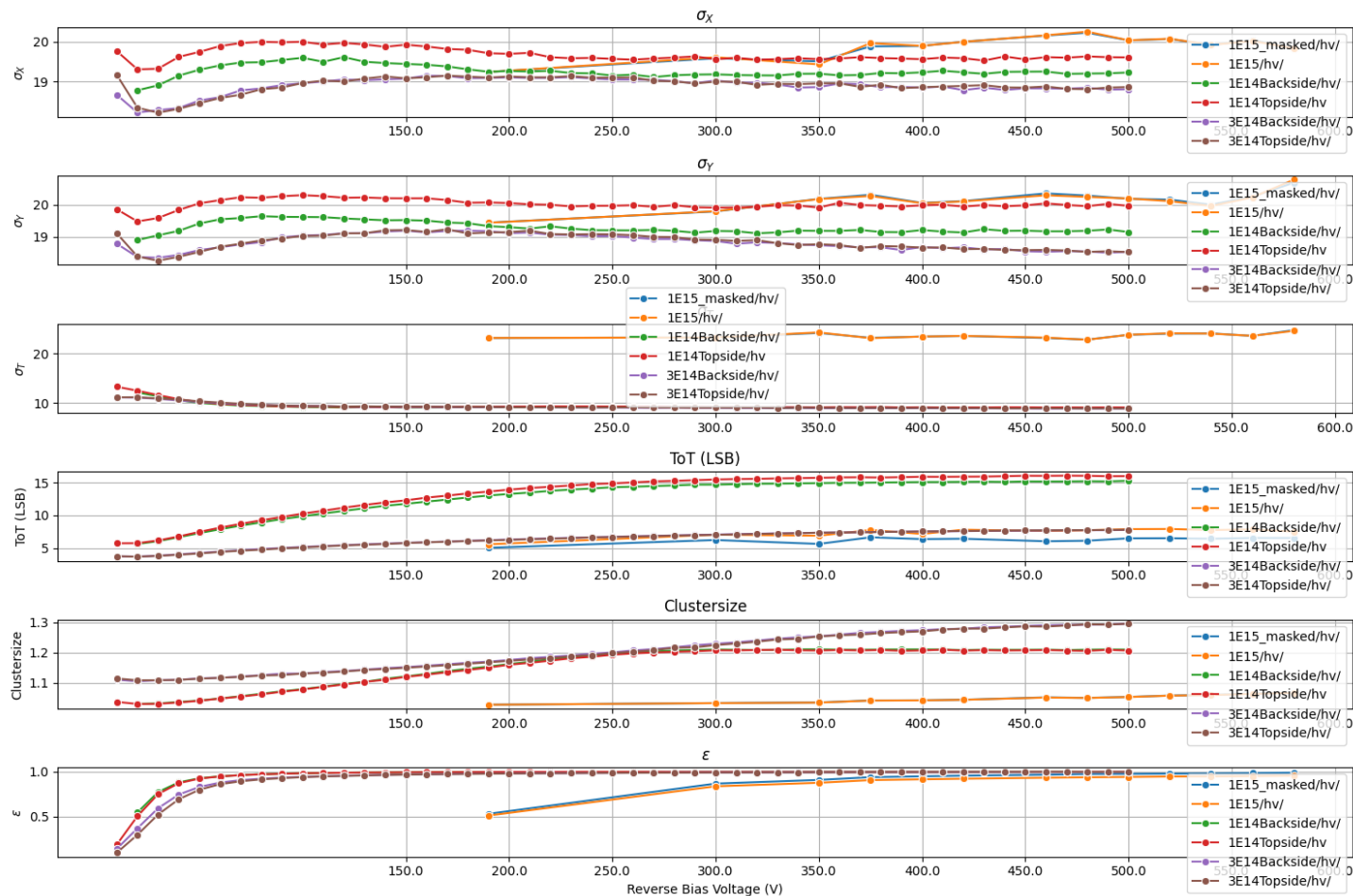


Comparing biasing schemes 3E14

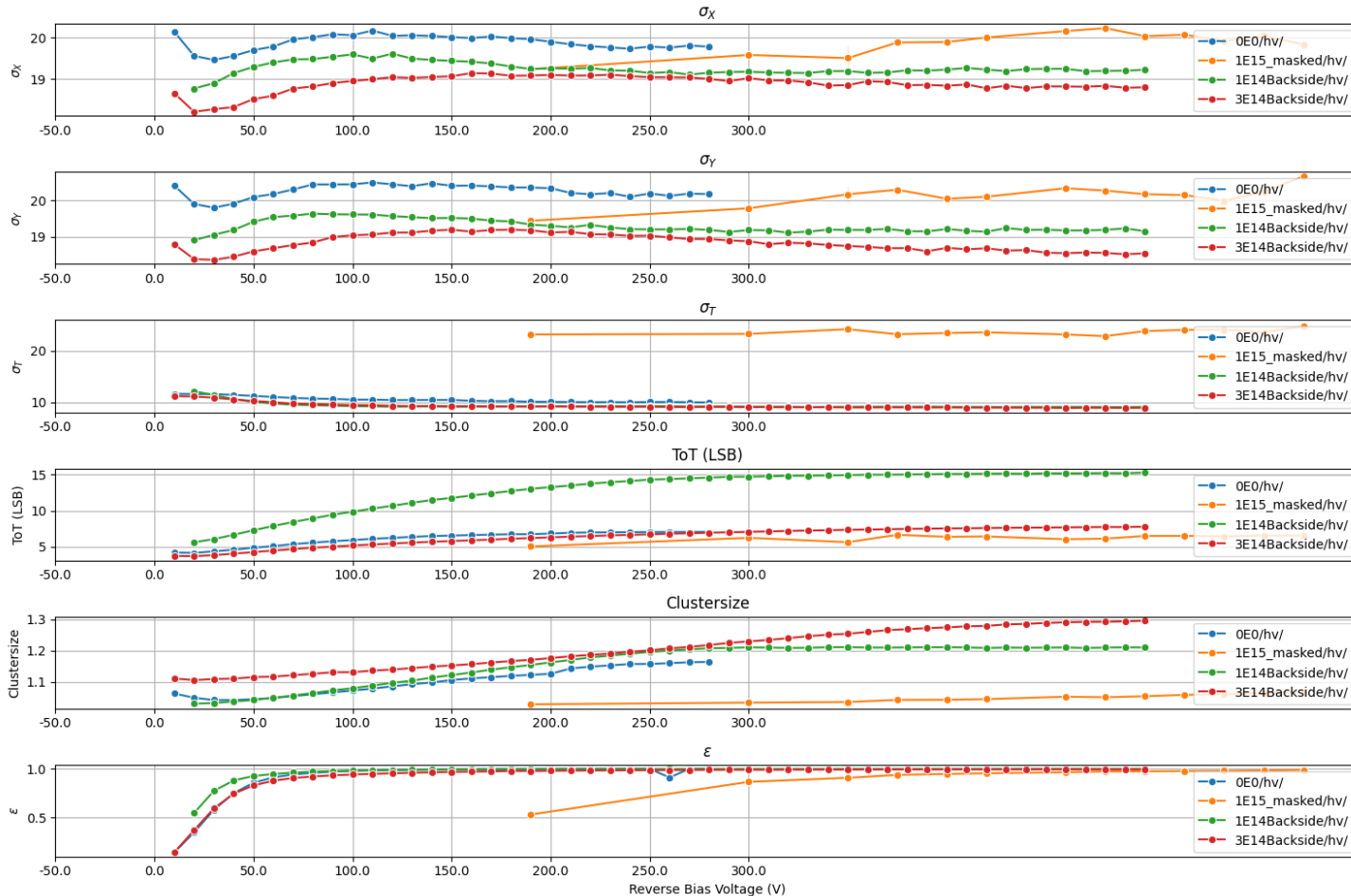
No noteworthy differences encountered



The entire testbeam in 1 figure



Just fluences



Spatial resolution effects:
3E14 better 1E14 better 1E15
Not understood yet

Timing resolution of 1E15 invalid
(see "Problems")

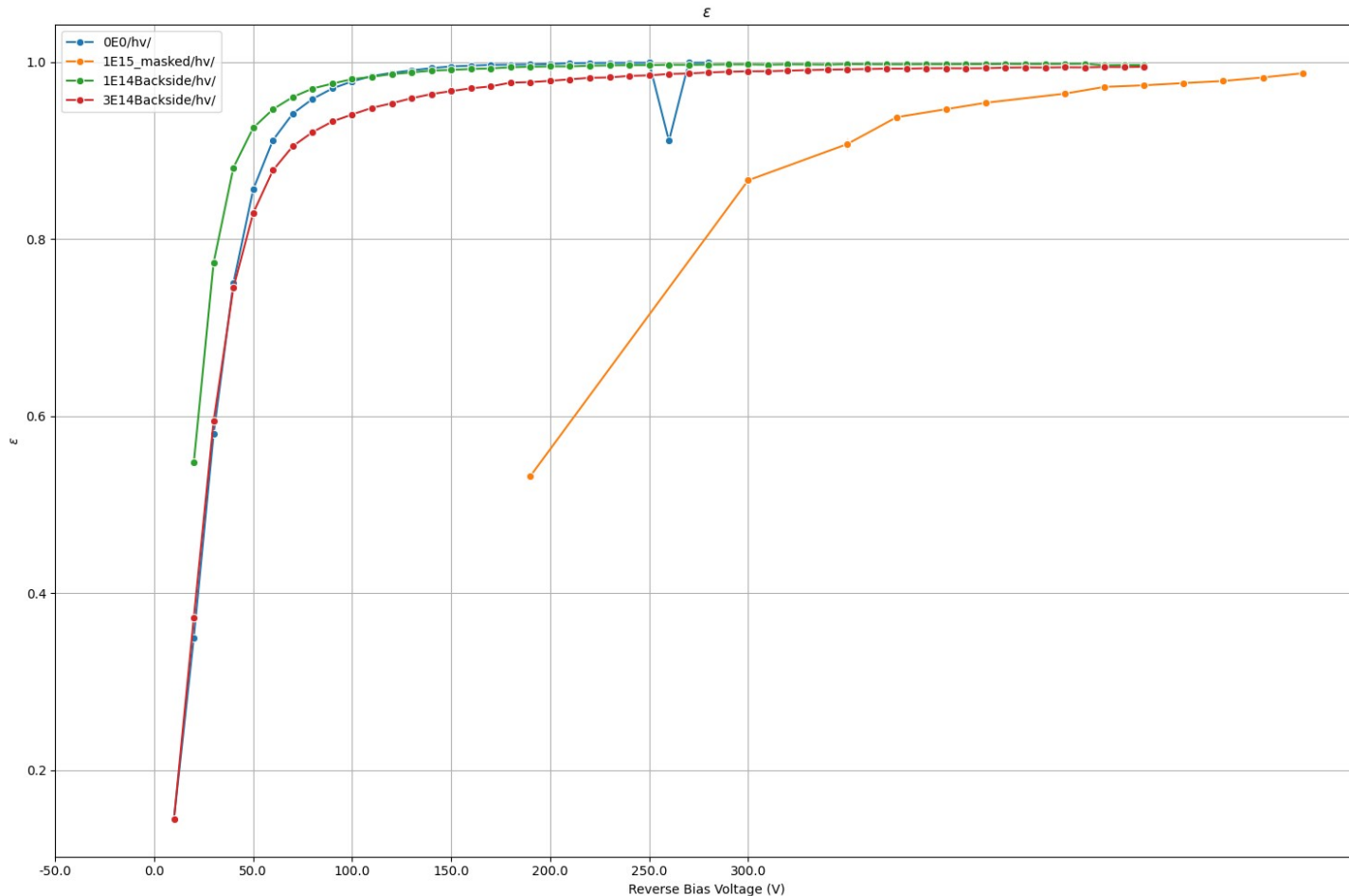
Significant ToT drop
from 1E14 → 3E14

3E14 → 1E15 not
so much more

Significant cluster size
drop at 1E15
3E14 > 1 E14??

Larger fluence →
larger bias needed

Just Efficiencies

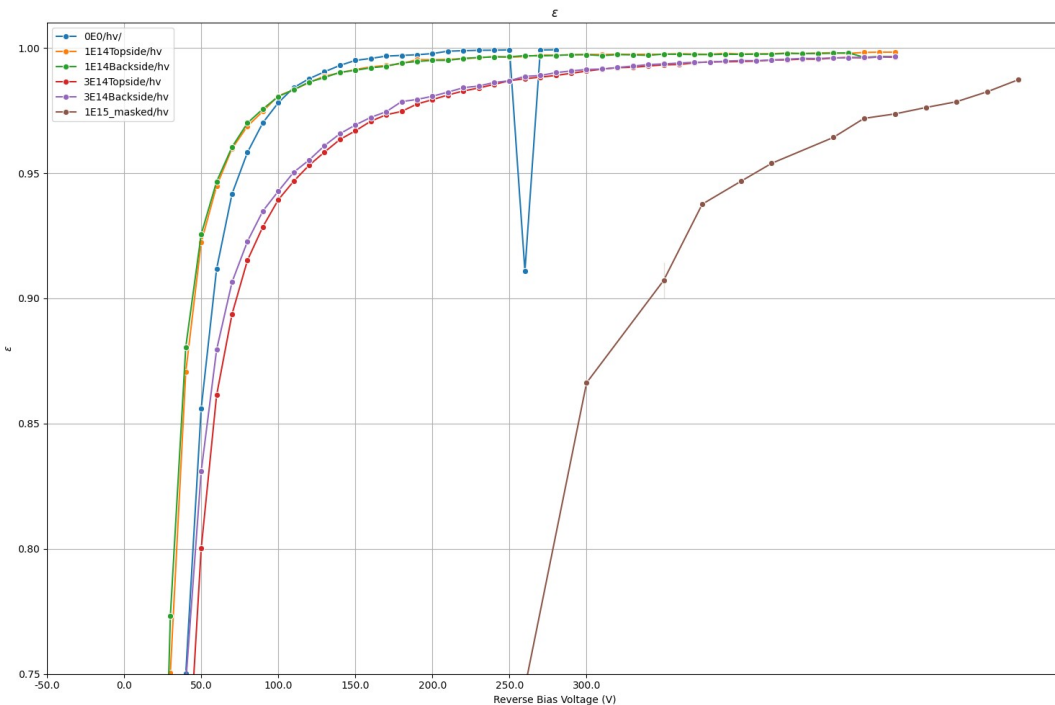


Fewer points for 1E15 due to its destruction :(

DUT	V _{Thr}
0E0	1.0V
1E14	1.1V
3E14	950mV
1E15	970mV

Used threshold as low as possible without noise

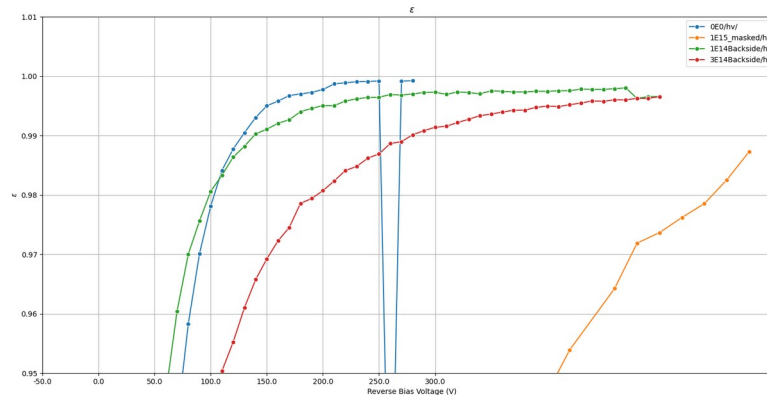
Biasing Schemes revisited



- Only minimal differences between top and backside biasing
- Minimal but backside seems to be better at lower bias voltages

Best Efficiencies

DUT / Fluence	Biasing	V _{Thr}	V _{Bias}	Efficiency	Comment
0E0	Top	1.1V	210V	99.9%	
1E14	Top	1.05V	600V	99.9%	Lower V _{Thr} available
3E14	Back	950mV	500V	99.6%	Masked noisy pixel but not the hurt double column
1E15	Top	970mV	580V	95.4% / 98.7%	Full / Masked
1E16	Back	1.05V	300V	-	



Summary

- **1E14 and 3E14 achieving full efficiency**
 - Higher bias voltages needed though (The HV-CMOS approach works)
 - Biasing scheme top- vs. backside not showing major differences
- **1E15 still performing good**
 - If it did not die, we would have achieved full efficiency
 - Backside biasing was not possible (W8)
- **1E16 is basically not working anymore**

ToDo

- Clean up some plots
- Why is unirradiated sample behaving so bad? Investigate!
- VNFB scans
- Mask pixels which were masked in the config
- More stuff will definitely come up

- Future testbeam?
- New samples (multiple per fluence) in range $5E14 \rightarrow 5E15$ (all backside processed) needed